

Freescale Semiconductor Application Note

Document Number: AN4095

CodeWarrior Build Tools Options for Optimal Performance on the Power Architecture® e200 Core

by Mark Anderson Senior Compiler Engineer CodeWarrior Tools

1 Introduction

This document provides two sets of options in the CodeWarrior tools to produce optimal code generation for the Power Architecture e200 core. One set optimizes for speed; another set optimizes for size.

For more information on the build tools, refer to the following compiler documents:

- *CW C-C++Notes 4.x.txt*
- CW Embedded PPC Notes 4.0.x.txt
- CodeWarrior Development Studio for Power Architecture Processors Build Tools Reference.

2 Optimization for Speed

Compiler (mwcceppc) options

-proc Zen -fp spfp_only -vle -ppc_asm_to_vle -char
unsigned -sym dwarf-2,full -wchar_t off -enum min -
04 -opt speed -inline auto,smart -ipa program -
<pre>use_lmw_stmw on -use_isel on -flag no-switch_tables</pre>
-flag switch_op -lang c99 -flag c9x_alias_by_type -
sdata 71 -sdata2 127 -prefix
ansi_prefix.PPCEABI.bare.h -schedule on -
spe_vector

Contents

1. Introduction	
2. Optimization for Speed	
3. Optimization for Size	:





Optimization for Size

Linker (mwldeppc) options

```
-proc Zen -fp spfp_only -lRuntime.PPCEABI.V.SP.UC.a -lMSL_C.PPCEABI.bare.V.SP.UC.a -lMSL_C++.PPCEABI.bare.V.SP.UC.a -sym dwarf-2,full -code_merging all,aggressive -far_near_addressing -vle_enhance_merging -vle_bl_opt -char unsigned -sdata 71 -sdata2 127 -map
```

TIP Experiment with the values of the -sdata and -sdata2 options. The compiler and linker need to have the same thresholds. Make them as large as possible until link errors are generated saying that the small data errors have overflowed. The threshold for *sdata* is independent of the threshold for *sdata2*. The default is 8 for each. If there is lots of small data, this value may need to be lowered to less than 8. One way to determine the optimal threshold is to look at *.data*, *.bss* and *.rodata* sections in the link map file. Ideally, only CodeWarrior library data is in these sections. If any application code in these sections, try to make the thresholds match the largest application data. If a link error is generated saying that relocation 109 does not match the section of an object and the object is in a library, bump down the threshold or rebuild the library with larger thresholds that match the application small data thresholds. If no link error is generated, it is OK if library and application thresholds do not match. *.rodata* corresponds to *sdata2* and *.data* and *.bss* corresponds to *sdataa*.

```
TIP Change -spe_vector to either
```

-spe_addl_vector Or

-spe2_vector

depending on processor support. For example z3 and some z6 processors, e.g. MPC5566 (Viper), support -spe_addl_vector

```
TIP Change -schedule on to either
```

-pragma "schedule z750" **Or**

-pragma "schedule z760"

if the targeted processor is in the z750 or z760 families.

TIP The option -ipa program generally produces the best code both when trying to obtain fastest speed or smallest size.

3 Optimization for Size

Compiler (mwcceppc) options

-proc Zen -fp spfp_only -vle -ppc_asm_to_vle -char unsigned -sym dwarf-2,full -enum min -04 - func_align 4 -opt space -inline auto,smart -ipa program -use_lmw_stmw on -Cpp_exceptions off -RTTI off -wchar_t off -bool off -use_isel on -flag no-switch_tables -flag switch_op -lang c99

CodeWarrior Build Tools Options for Optimal Performance on Power Architecture e200 Core Application Note

2 Freescale Semiconductor



-flag c9x_alias_by_type -sdata 32767 -sdata2 127 -prefix ansi_prefix.PPCEABI.bare.SZ.h -schedule on -spe_vector

Linker (mwldeppc) options

-proc Zen -fp spfp_only -lRuntime.PPCEABI.V.SP.UC.a -lMSL_C.PPCEABI.bare.SZ.V.SP.UC.a -lMSL_C++.PPCEABI.bare.SZ.V.SP.UC.a -sym dwarf-2,full -code_merging all,aggressive -far_near_addressing -vle_enhance_merging -vle_bl_opt -char unsigned -sdata 32767 -sdata2 127 -map

NOTE The tips in the previous Section 2, "Optimization for Speed" also apply to this section.

CodeWarrior Build Tools Options for Optimal Performance on Power Architecture e200 Core Application Note

Freescale Semiconductor 3



How to Reach Us:

Home Page: www.freescale.com

E-mail: support@freescale.com

US A/Europe or Locations Not Listed: Freescale Semiconductor Technical Information Center, CH370 1300 N. Alma School Road Chandler, Arizona 85224 +1-800-521-6274 or +1-480-768-2130 support@ freescale.com

Europe, Middle East, and Africa: Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064, Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

As ia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale, the Freescale logo, CodeWarrior and ColdFire are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. ColdFire+, Kinetis, Processor Expert, and Qorivva are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. ARM is the registered trademark of ARM Limited. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2011 Freescale Semiconductor, Inc. All rights reserved.

Document Number: AN4095

19 March 2010

