Document Number: AN3451
Rev. 0, 03/2007

M68HC08 SLIC vs. HCS08 SLIC

by: Michael Winge
MCD EMEA Application Engineer,
East Kilbride, Scotland

Contents

1 Introduction

Freescale Semiconductor's HCS08 family is the next step in the low-cost, high-performance evolution of the M68HC08 family.

This application note explains the differences between the M68HC08 SLIC and HCS08 SLIC. The SLIC is the Freescale slave local interconnect network (LIN) interface controller. It provides slave node connectivity on a LIN sub-bus. The LIN bus has been developed by the automotive industry as an open standard for a cost effective sub-bus system.

This application note does not describe specific device implementations such as register mapping and interrupt vector location. Programmers and designers should consult the specific HCS08 MCU data sheet for details.

2 SLIC Features

The M68HC08 and HCS08 SLICs support these features:

- Full LIN message buffering of identifier and 8 data bytes
- Automatic bit rate and LIN message frame synchronization
- No prior programming of bit rate required, 1–20 kbps LIN bus speed operation
- All LIN messages will be received (no message loss during synchronization)
- Input clock tolerance as high as ±50%, allowing internal oscillator to remain untrimmed
- Incoming break symbols always allowed to be 10 or more bit times without message loss
- Automatic software trimming of internal oscillator using LIN synchronization data
- Automatic processing and verification of LIN SYNCH BREAK and SYNCH BYTE
- Automatic checksum calculation and verification with error reporting
- Maximum of two interrupts per standard LIN message frame with no errors
- Full LIN error checking and reporting
- High-speed LIN capability up to 83.33 kbps to 120.00 kbps
- Configurable digital receive filter
- Streamlined interrupt servicing using a state vector register
- Switchable UART-like byte transfer mode for processing bytes one at a time without LIN message framing constraints
- Enhanced checksum (includes ID) generation and verification

3 Differences Between M68HC08 and HCS08 SLIC Modules

3.1 Register Differences

3.1.1 SLIC Memory Maps

M68HC08

Address	Use
0x0000+Offset	SLIC Control Register 1
0x0001+Offset	SLIC Control Register 2
0x0002+Offset	SLIC Status Register
0x0003+Offset	SLIC Prescaler Register
0x0004+Offset	SLIC Bit Time Register High
0x0005+Offset	SLIC Bit Time Register Low
0x0006+Offset	SLIC State Vector Register
0x0007+Offset	SLIC Data Length Code Register
0x0008+Offset	SLIC Identifier Register
0x0009+Offset	SLIC Data Register 7
…	…
0x0010+Offset	SLIC Data Register 0

HCS08

Address	Use
0x0000+Offset	SLIC Control Register 1
0x0001+Offset	SLIC Control Register 2
0x0002+Offset	SLIC Bit Time Register High
0x0003+Offset	SLIC Bit Time Register Low
0x0004+Offset	SLIC Status Register
0x0005+Offset	SLIC State Vector Register
0x0006+Offset	SLIC Data Length Code Register
0x0007+Offset	SLIC Identifier Register
0x0008+Offset	SLIC Data Register 0
…	…
0x000F+Offset	SLIC Data Register 7

Figure 1. Differences Between M68HC08 and HCS08 SLIC Memory Map

The HCS08 SLIC memory map has one fewer register than M68HC08 SLIC. The SLIC Prescaler (SLCP) register has been deleted from the HCS08 SLIC memory map. The Receive Filter Prescaler (RXFP) bits from the SLCP have been moved into the SLIC Control Register 2 (SLCC2), making the SLCP obsolete in the HCS08 SLIC. The SLIC Status (SLCS) register is now located after SLIC Bit Time Register Low (SLCBTL) and the order of the SLIC data registers has been reversed.

3.1.2 Changes in SLIC Control Register 1 (SLCC1)

M68HC08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	INITREQ	0	WAKETX	TXABRT	IMSG	SLCIE
Write:			INITREQ		WAKETX	TXABRT	IMSG	SLCIE
Reset:	0	0	1	0	0	0	0	0

HCS08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	INITREQ	BEDD	WAKETX	TXABRT	IMSG	SLCIE
Write:			INITREQ	BEDD	WAKETX	TXABRT	IMSG	SLCIE
Reset:	0	0	1	0	0	0	0	0

Figure 2. Changes in SLCC1

A new control bit has been added to the HCS08 SLCC1, the Bit Error Detection Disable (BEDD) bit. With the BEDD, the user can disable and enable the bit error detection circuitry.

3.1.3 Changes in SLIC Control Register 2 (SLCC2)

M68HC08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	SLCWCM	BTM	0	SLCE
Write:					SLCWCM	BTM		SLCE
Reset:	0	0	0	0	0	0	0	0

HCS08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	RXFP	RXFP	RXFP	SLCWCM	BTM	0	SLCE
Write:		RXFP	RXFP	RXFP	SLCWCM	BTM		SLCE
Reset:	0	1	0	0	0	0	0	0

Figure 3. Changes in SLCC2

The 3-bit wide RXFP has been added into the HCS08 SLCC2. In the M68HC08 SLIC, the RXFP bits are located in the SLIC Prescaler register (SLCP). The RXFP are only 2 bits wide.

The additional RXFP bit allows the HCS08 to operate at a higher bus frequency.

The RXFP bits define the highest count value of the 4-bit up/down counter, which is the total maximum filter delay. Any pulse lower than the maximum filter delay value will be rejected by the filter and ignored as noise.

3.1.4 SLIC Prescaler Register (SLCP)

	Bit 7	6	5	4	3	2	1	Bit 0	
Read:	RXFP		0	0	0	0	0	0	M68HC08
Write:									
Reset:	1	0	0	0	0	0	0	0	

Figure 4. SLIC Prescaler Register

The SLCP has been removed from the HCS08 SLIC memory map. For further details refer to Section 3.1.3, "Changes in SLIC Control Register 2 (SLCC2).

3.1.5 Changes in SLIC Bit Time Register (SLCBT)

	Bit 7	6	5	4	3	2	1	Bit 0	
Read:	0	0	0	BT12	BT11	BT10	BT9	BT8	M68HC08
Write:									HIGH
Reset:	0	0	0	0	0	0	0	0	

	Bit 7	6	5	4	3	2	1	Bit 0	
Read:	BT7	BT6	BT5	BT4	BT3	BT2	BT1	0	M68HC08
Write:									LOW
Reset:	0	0	0	0	0	0	0	0	

	Bit 7	6	5	4	3	2	1	Bit 0	
Read:	0	BT14	BT13	BT12	BT11	BT10	BT9	BT8	HCS08
Write:									HIGH
Reset:	0	0	0	0	0	0	0	0	

	Bit 7	6	5	4	3	2	1	Bit 0	
Read:	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0	HCS08
Write:									LOW
Reset:	0	0	0	0	0	0	0	0	

Figure 5. Changes in SLCBT

The M68HC08 SLIC bit time value is 13 bits wide. The HCS08 SLIC has a better bit-time resolution because the HCS08 SLIC bit time value is 15 bits wide. Increasing the resolution of the SLCBT allows the HCS08 SLIC module to run at higher bus speeds than the HC08 SLIC, resulting in more accurate bit time measurement in LIN mode or a more accurate bit time generation in BTM mode.

3.1.5.1 Bit Time Calculation Comparisons

The examples listed below compare the bit time calculations when the baud rate is 1000 bps and 19200 bps for SLIC system clock speeds of 20 MHz or 4 MHz.

- Bit time calculation for the LIN bus baud rate of 1000 bps with 4 MHz SLIC system clock (bus clock). The bit time in the SLIC is measured in SLIC system tick, which is driven by the SLIC system frequency. The bit time (SLCBT value) is the number of SLIC system ticks that occur during one LIN bus bit time.
- LIN bus bit time = SLIC system tick × SLCBT

  where:

$$LIN\text{ bus bit time } = \frac{1}{LIN\text{ bus baud rate}} = 1/1000\text{ bps } = 1\text{ ms}$$

and

$$SLIC\text{ system tick } = \frac{1}{SLIC\text{ system clock}} = 1/2\text{ MHz } = 0.0005\text{ ms}$$

$$SLCBT = \frac{LIN\text{ bus bit time}}{SLICK\text{ system tick}} = \frac{1\text{ ms}}{0.00025\text{ ms}} = 4000(SLIC\text{ clock counts per bit})$$

Therefore, a 1 SLIC clock count would be 1/4000th of a bit or 0.025% of a bit.

- Bit time calculation for the LIN bus baud rate of 1000 bps with 20 MHz SLIC system clock (bus clock)
- LIN bus bit time = SLIC system tick × SLCBT

where:

$$LIN\text{ bus bit time } = \frac{1}{LIN\text{ bus baud rate}} = 1/1000\text{ bps } = 1\text{ ms}$$

and

$$SLIC\text{ system tick } = \frac{1}{SLIC\text{ system clock}} = 1/20\text{ MHz } = 0.00005\text{ ms}$$

$$SLCBT = \frac{LIN\text{ bus bit time}}{SLICK\text{ system tick}} = \frac{1\text{ ms}}{0.0005\text{ ms}} = 2000(SLIC\text{ clock counts per bit})$$

Therefore, a 1 SLIC clock count would be 1/20000th of a bit or 0.005% of a bit.

- Bit time calculation for the LIN bus baud rate of 19200 bps with 4 MHz SLIC system clock (bus clock)
- LIN bus bit time = SLIC system tick × SLCBT

where

$$LIN\text{ bus bit time } = \frac{1}{LIN\text{ bus baud rate}} = \frac{1}{19200\text{ bps}} = 52\text{ us}$$

and

$$SLIC\text{ system tick } = \frac{1}{SLIC\text{ system clock}} = 1/4\text{ MHz } = 0.25\text{ us}$$

$$SLCBT = \frac{LIN\text{ bus bit time}}{SLICK\text{ system tick}} = \frac{52\text{ us}}{0.25\text{ us}} = 208(SLIC\text{ clock counts per bit})$$

Therefore, a 1 SLIC clock count would be 1/208th of a bit or 0.481% of a bit.

- Bit time calculation for the LIN bus baud rate of 19200 bps with 20 MHz SLIC system clock (bus clock)
- LIN bus bit time = SLIC system tick × SLCBT

where

$$LIN\text{ bus bit time } = \frac{1}{LIN\text{ bus baud rate}} = \frac{1}{19200\text{ bps}} = 52\text{ us}$$

and

$$SLIC\text{ system tick } = \frac{1}{SLIC\text{ system clock}} = 1/20\text{ MHz} = 0.05\text{ us}$$

$$SLCBT = \frac{LIN\text{ bus bit time}}{SLICK\text{ system tick}} = \frac{52\text{ us}}{0.05\text{ us}} = 1040(SLIC\text{ clock counts per bit})$$

Therefore, a 1 SLIC clock count would be 1/1040th of a bit or 0.096% of a bit

3.2 Bit Error Detection Enable/Disable

Unlike the M68HC08 SLIC, the HCS08 SLIC can disable and enable bit error detection using a new control bit in the SLCC1. For further information about the new control bit, refer to Section 3.1.2, "Changes in SLIC Control Register 1 (SLCC1)."

This feature has been added because bit error detection is not recommended during byte transfer mode (BTM). In BTM, the bit error detection circuitry reports bit errors on bit boundaries and not on byte boundaries. This can result in misaligned data.

In LIN mode, the bit error detection circuitry must be enabled because the bit error detection is a part of the LIN protocol specification.

If the SLIC runs in LIN high-speed mode (where the LIN protocol speeds are exceeded), then bit-error detection should also be disabled due to delays in the LIN physical interface that cause bit errors in high-speed LIN traffic. Please refer to the HCS08 SLIC (e.g. MC9S08EL32 specification) for further information.

Further information about products that Freescale offers for LIN designs can be found at following website: http://www.freescale.com/lin.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: AN3451
Rev. 0
03/2007