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MSC711x Overview

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This application note describes the MSC711x architecture and compares the MSC711x family of DSPs with the MSC81xx family of DSPs (MSC8101, MSC8102, MSC8103, MSC8122, and MSC8126).

The MSC711x family is a medium-to-high performance line of products built on the StarCore™ SC1400 architecture. The MSC711x is the first DSP in the market with a double data rate (DDR) memory interface, offering the same low cost memory used in today's PC. The MSC711x family bridges the gap between the DSP56300 family and the MSC8100 family of DSPs and is the third generation of StarCore-based DSPs:

- First generation: MSC8101/ MSC8103.
- Second generation: MSC8102/MSC8122/ MSC8126.
- Third generation: MSC7110, MSC7112, MSC7113, MSC7115, MSC7116, MSC7118, MSC7119.

To preserve your software investment, the MSC711x family maintains compatibility with the instruction set and binary software of the MSC81xx family.

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In **Table 1** and **Table 2**, the differences within the family are highlighted in bold. As the tables show, devices in the MSC711x family differ according to the core speed, the amount of M1 and M2 SRAM memory, the number of TDMs, and whether there is an Ethernet MAC. All devices are pin-to-pin compatible, so you can start an application on one MSC711x device and then move it to another device as your application changes (for example, additional memory, more TDMs, Ethernet, and so on).

Table 1. Recent Additions to the MSC711x Family

Products	MSC7119	MSC7118
Target Markets	VoIP Enterprise, ROBO, Wireless Communication, Industrial Control, Automation, General-Purpose	VoIP Enterprise, ROBO, Wireless Communication, Industrial Control, Automation, General-Purpose
Features	**300 MHz** 16 KB ICache DDR Controller HDI16 UART I^2C **256 KB SRAM (M1)** **192 KB SRAM (M2)** **2 TDM** **Ethernet MAC**	**300 MHz** 16 KB ICache DDR Controller HDI16 UART I^2C **256 KB SRAM (M1)** **192 KB SRAM (M2)** **3 TDM**

Table 2. Base Members of the MSC711x Family

Products	MSC7116	MSC7115	MSC7113	MSC7112	MSC7110
Target Markets	VoIP Enterprise, ROBO, Wireless Communication, Security Systems, Industrial Control, Automation, General-Purpose	VoIP Enterprise, ROBO, Wireless Communication, Security Systems, Industrial Control, Automation, General-Purpose	VoIP Enterprise, SOHO/ROBO, IAD, Wireless Communication, Security Systems, Industrial Control, Automation, General-Purpose	VoIP Enterprise, SOHO/ROBO, IAD, Wireless Communication, Security Systems, Industrial Control, Automation, General-Purpose	VoIP enterprise, SOHO/ROBO, IAD, Wireless Communication, Security Systems, Industrial Control, Automation, General-Purpose
Features	**266 MHz** 16 KB ICache DDR Controller HDI-16 UART I^2C **192 KB SRAM (M1)** **192 KB SRAM (M2)** **2 TDM** **Ethernet MAC**	**266 MHz** 16 KB ICache DDR Controller HDI-16 UART I^2C **192 KB SRAM (M1)** **192 KB SRAM (M2)** **3 TDM**	**266 MHz** 16 KB ICache DDR Controller HDI-16 UART I^2C **192 KB SRAM (M1)** **2 TDM** **Ethernet MAC**	**266 MHz** 16 KB ICache DDR Controller HDI-16 UART I^2C **192 KB SRAM (M1)** **2 TDM**	**266 MHz** 16 KB ICache DDR Controller HDI-16 UART I^2C **64 KB SRAM (M1)** **1 TDM**

The MSC7119, MSC7116, and MSC7113 have an Ethernet MAC but have only two TDMs. An Ethernet MAC replaces one of the TDMs. The MSC7118 and MSC7115 have three TDMs and no Ethernet MAC. The MSC7112 and MSC7113 have 192 KB of M1 memory and no M2 memory. The low-end MSC7110 contains the least memory: 64 KB of M1 and no M2 SRAM, and it has only one TDM.

All MSC711x devices are available in either a lead-bearing or a lead-free[1] package. **Table 3** shows a quick overview of the MSC711x family.

Table 3. MSC711x Quick Overview

Core	SC1400
Instruction Cache	16 KB
Peripherals	DDR controller 16- or 32-bit data bus 10/100 Ethernet MAC (MSC7119, MSC7116, MSC7113) 1–3 TDMs
Performance	MSC7110/2/3/5/6 (266 MHz): 1064 MMACs MSC7118/9 (300 MHz): 1200 MMACs
Estimated Typical Power (EFR, 2 TDMs, 2 timers, 10 I/O, 16 data DDR, 25° C)	MSC7110/2/3/5/6 (266 MHz): 764 mW MSC7118/9 (300 MHz): 785 mW
Package	400 pin MAP BGA (17 × 17 mm)
Temperature	–40 to 105° C (Industrial)
Power Supplies	1.2 V, 2.5 V, 3.3 V

The estimated typical power, defined as running an EFR algorithm, two TDMs, two timers, 10 I/O, 16 bit data DDR at room temperature (25° C) is 764 mW for the MSC7110/2/3/5/6 running at 266 MHz, and 785 mW for the MSC7118/9 running at 300 MHz. Refer to the device data sheet for updates.

The MSC711x package comes in a 400-pin ball grid array, 17 × 17 mm square package. The MSC711x family requires three power supplies: 1.2 V for the core, 2.5 V for DDR memory, 3.3 V for the IO. If DDR memory is not used, the 2.5 V is optional. For details, see the *MSC711x Design Checklist* (AN2786).

1 New Family Members

The MSC7119 and MSC7118 are the most recent additions to the MSC711x family. **Table 4** shows the enhancements added to these parts.

Table 4. MSC7119/MSC7118 Versus MSC7116/MSC7115/MSC7113/MSC7112/MSC7110

	MSC7116/MSC7115/MSC7113/MSC7112/MSC7110	**MSC7119/MSC7118**
Extended core speed	266 MHz	300 MHz
Internal memory (SRAM)	M1: 64 KB–192 KB M2:–192 KB	M1: 256 KB M2: 192 KB
GPIO	35 multiplexed GPIO signal pins	39 multiplexed GPIO signal pins

1. Some countries require or will require that all devices reflowed or soldered to a board be lead free. This has to do with how much lead are placed in the spheres (balls) of the part. Typically you cannot mix lead and lead-free parts on a board because they have different processes to place the part on the board. The European Union enacted the Restriction of Hazardous Substances (RoHS) and the Waste Electrical and Electronic Equipment (WEEE) directive mandating that by July 1, 2006, only lead-free electronic and electrical products will be legally salable in member countries. Military systems are, for the moment, exempt from the lead free requirements. Lead-bearing (also known as eutectic) parts can withstand reflow temperatures up to 225° C. Lead-free parts can withstand reflow temperatures from 245 to 260° C.

Table 4. MSC7119/MSC7118 Versus MSC7116/MSC7115/MSC7113/MSC7112/MSC7110 (Continued)

	MSC7116/MSC7115/MSC7113/MSC7112/MSC7110	MSC7119/MSC7118
Boot Modes	HDI16 I^2C (no H/W SPI)	HDI16 I^2C SW SPI
	DDR Prefetch Buffer (1M88B mask set only)	DDR Prefetch Buffer
	Address Detection Unit (1M88B mask set only)	Address Detection Unit

The MSC7119/MSC7118 have faster extended core speeds, more internal memory, four more GPIO pins, and one more boot mode (software SPI). The DDR prefetch buffer increases DDR throughput. The address detection unit is for debugging your application.

2 Estimated Channel Densities

The channel densities discussed in this section are only estimates of what the MSC711x family can achieve using optimized application code. The two biggest parameters to increase channel density are speed and internal memory. The MSC7119/MSC7118 core runs 50 percent faster and has 64 KB more M1 memory than the MSC7116/MSC7115. The MSC7119/MSC7118 handle approximately 50 percent more channels than the MSC7116/MSC7115.

Table 5 shows the number of estimated mid-complexity channels for the MSC711x family. Mid-complexity channels are defined as G.729ab, G.726, and T.38 FAX. The MSC7110 handles an estimated 8 channels compared to 24 channels for the MSC7119/MSC7118.

Table 5. MSC711x Estimated Mid Complexity Channels

Products	MSC7119 (300 MHz)	MSC7118 (300 MHz)	MSC7116 (200 MHz)	MSC7115 (200 MHz)	MSC7113 (200 MHz)	MSC7112 (200 MHz)	MSC7110 (200 MHz)
Estimated Mid-Complexity Channels	24	24	16	16	12	12	8

Table 6 shows the estimated number of premium voice mid/high complexity, G.711 10 ms/5 ms and modem relay channels for the MSC7115/MSC7116 at 200 MHz and MSC7118/MSC7119 at 300 MHz. High complexity is defined as G.729i, G.723.1, and GSM-EFR.

Table 6. Channel Densities

Channel Type	Estimated MSC7116/ MSC7115 Channels at 200 MHz	Estimated MSC7119/ MSC7118 Channels at 300 MHz
Premium Voice – Mid Complexity	16	24
Premium Voice – High Complexity	12	18
G.711 – 10 ms	30	45
G.711 – 5 ms	24	36
Modem Relay	8	12

3 MSC711x Architecture Overview

As **Figure 1** shows, the MSC711x architecture consists of three major subsystems:

- Extended core, which contains the SC1400 core.
- Data transfer subsystem, which manages data movement throughout the device.
- Peripheral subsystem, which moves data in and out of the device.

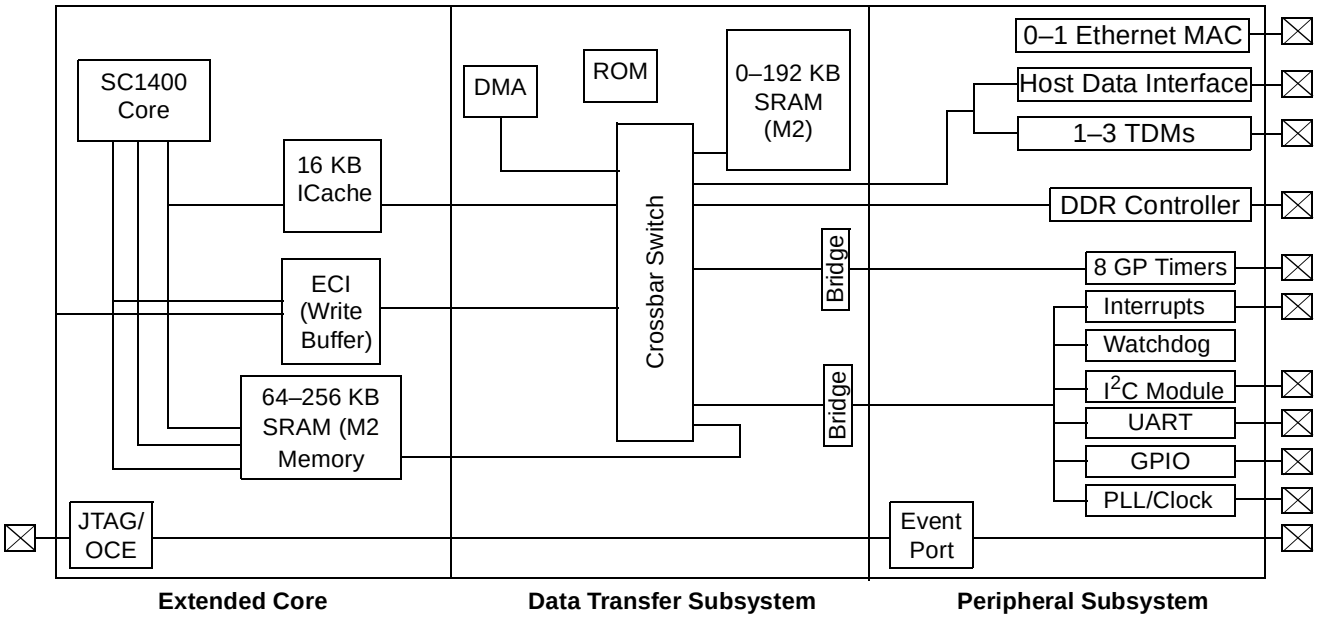


Figure 1. MSC711x Architecture

The extended core runs at the core speed—for example, 300 MHz. Only one core clock cycle is required to read from the instruction cache (ICache), write into the write buffer (WB), and read/write into M1. All modules in the data transfer and peripheral blocks run at the core clock divided by 2. For example, in a 300 MHz core, DDR is clocked at 150 MHz. This is called the bus clock. The core performs a single read or write access from M2 using 7–9 core clock cycles. For eight consecutive read or write accesses, access time is reduced to an average of five core clock cycles per access. Depending on the peripheral used, the core can read or write 5–10 core clock cycles. The ICache can read from M2 on the average of two core clock cycles per access. **Figure 2** shows the MSC7116 internal buses and their widths.

The SC1400 has three buses that work concurrently:

- 128-bit program (P) bus.
- 64-bit XA data bus.
- 64-bit XB data bus.

The DDR controller supports 16 or 32 data bits. The DDR bus size is set via bit 5 in the DEVCFG register. When this bit is set after reset, it can no longer be reset. A value of 1 selects the 32-pin DDR interface. The crossbar switch supports buses of 32, 64, and 128 bits. Up to four crossbar buses can work concurrently. The host interface (HDI16) supports 8 or 16 data bits. The HDI16 bus size is determined during power-on reset (the H8BITpin is sampled at the rising edge of $\overline{\text{PORESET}}$. A value of 0 selects 16-bit operation.

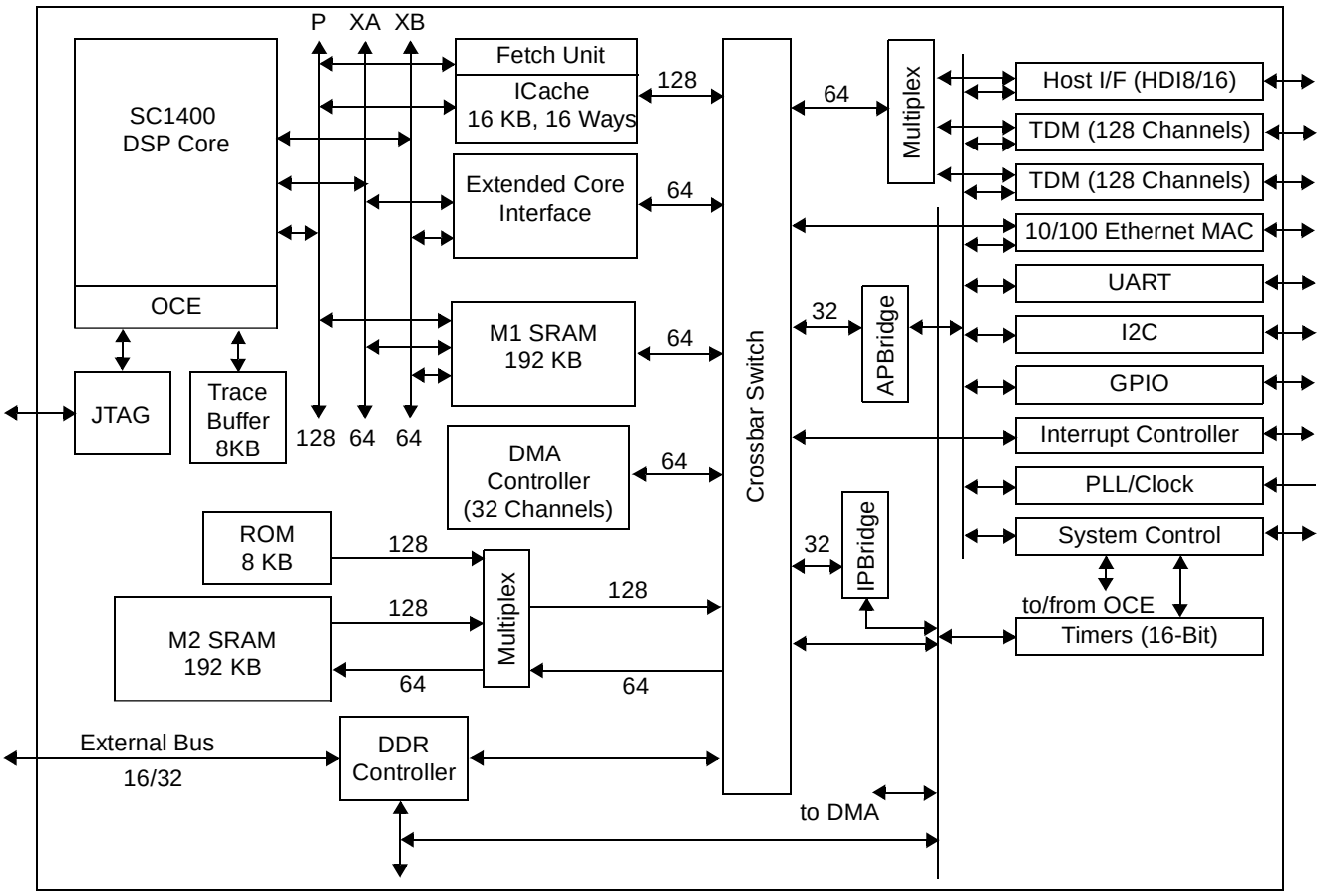


Figure 2. MSC7116 Buses

4 MSC711x Memory Hierarchy

As shown in **Figure 3**, the MSC711x family has three levels of memory. Level 1 memory is faster than level 2, which is faster than level 3:

- Level 1 consists of the ICache, write buffer and M1 SRAM. Level 1 can be accessed in a single core clock cycle.
- Level 2 consists of M2 SRAM.
- Level 3 consists of external DDR. Level 3 support the largest memory map.

Critical data typically resides in M1 with critical application code in M1 and/or the ICache. The ICache can pull application code from both M2 and external DDR memory. Data can also reside in M2 and/or external DDR memory. Application code running out of external DDR memory runs much more slowly. Typically, DMA is used to bring application code from external DDR into M2 or M1 memory.

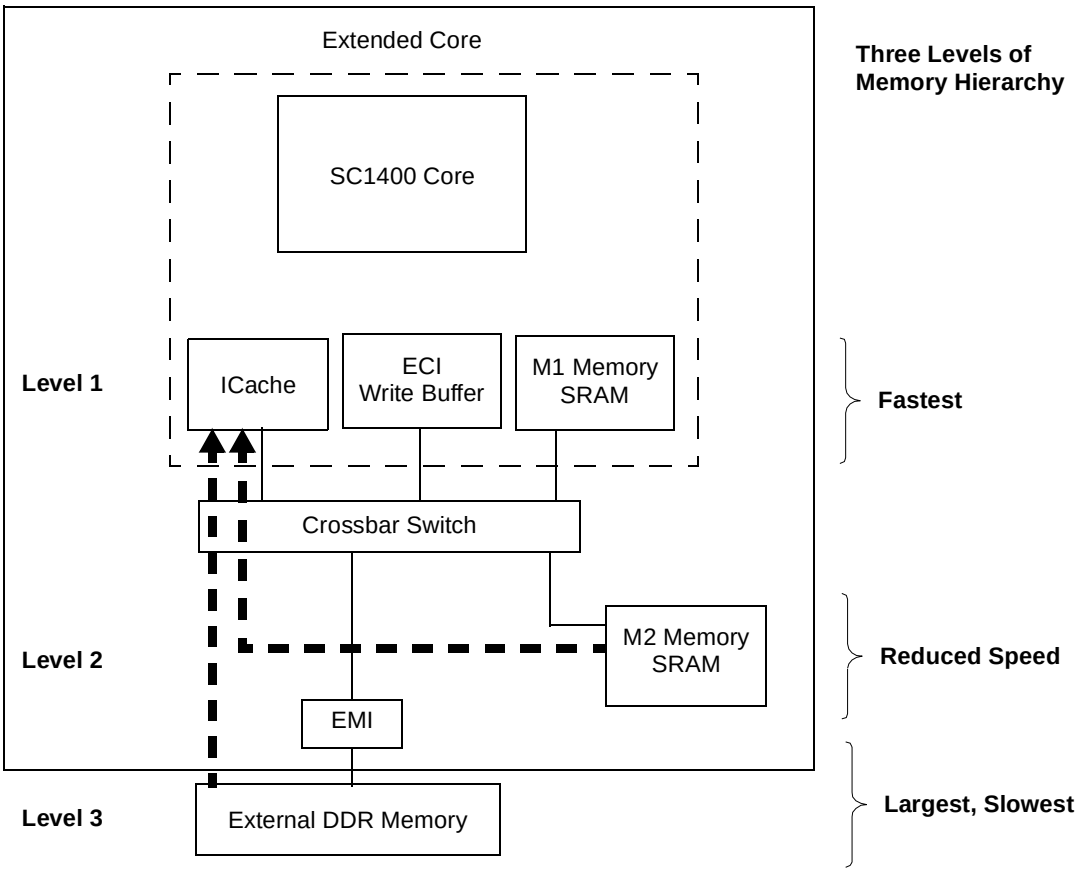


Figure 3. MSC711x Memory Hierarchy

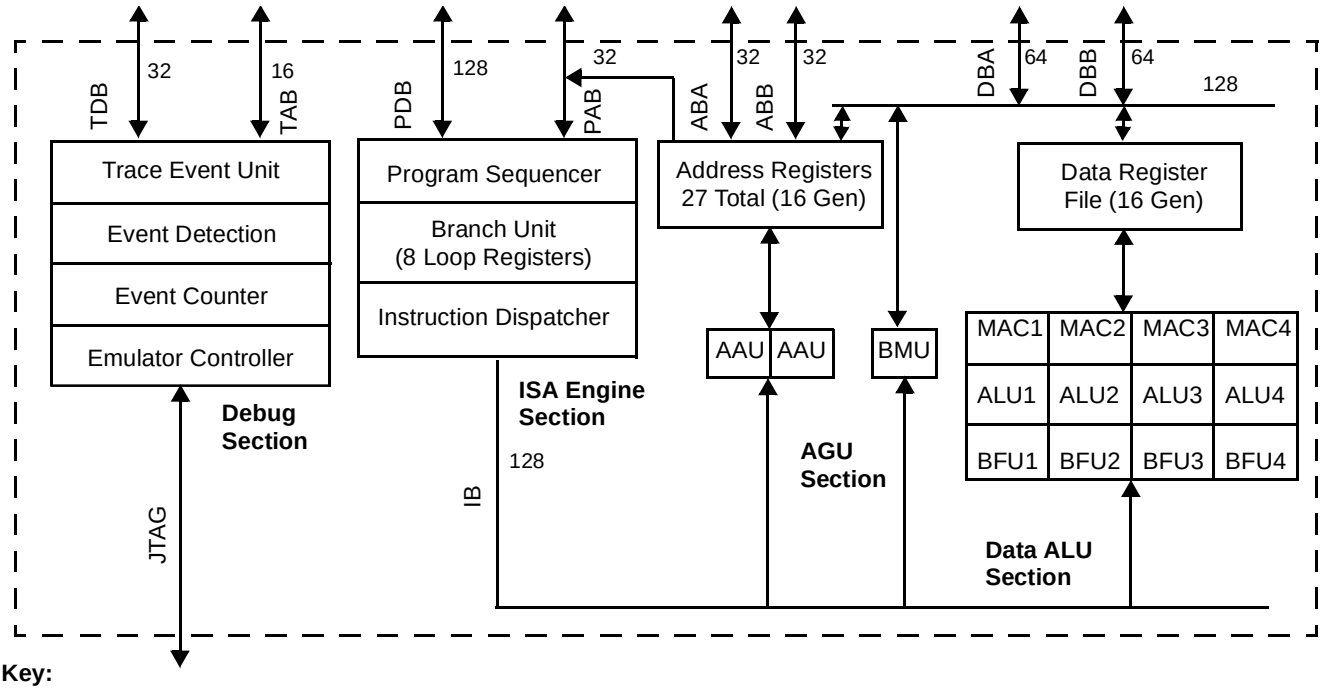
5 Extended Core

As shown in **Figure 1**, the extended core consists of the following:

- SC1400 core.
- 16 KB ICache.
- Extended core interface.
- M1 SRAM.
- JTAG/OCE emulator.

5.1 SC1400 Core

The SC1400 core is functionally equivalent to the SC140 core used in the MSC81xx family. The only difference between the SC1400 and the SC140 cores is that the SC1400 core is synthesized versus hard macro, so future derivatives using the SC1400 core can be made more rapidly. **Figure 4** shows the SC1400 core block diagram.



Key:

AAU	Address arithmetic unit, which contains a 32-bit adder.
AGU	Address generation unit, which performs address calculations using integer arithmetic (for example, update pointers).
ALU	Arithmetic logic unit, which contains a MAC and a BFU.
BFU	Bit field unit, which contains a 40-bit barrel shifter.
BMU	Bit mask unit, which sets, clears, inverts, or tests groups of bits in a register or memory location.
MAC	Multiply accumulate unit, which is a 40-bit MAC that supports a 16 × 16 multiply operation.

Figure 4. SC1400 Core

In the SC1400 core are three computational blocks (ISA engine, AGU, data ALU) and a debug section. The AGU and data ALU are defined as follows:

- *Data arithmetic logic unit (*data *ALU)*. Contains four bit field units (BFUs), four ALUs, four 40-bit multiply accumulate units (MACs), and data registers. The MAC completes a 16 × 16 multiply operation in one core clock cycle. The BFU contains a 40-bit barrel shifter.
- *Address generation unit (AGU)*. Consists of two address arithmetic units (AAU), a bit mask unit (BMU), and 27 address registers. The registers perform address calculations using integer arithmetic to address data operands in memory. It implements linear, modulo, multiple wrap-around modulo, and reverse-carry arithmetic. Each AAU contains a 32-bit adder. The BMU provides an easy way to set, clear, invert, or test a selected, but not necessarily adjacent, group of bits in a register or memory location.

The units of the SC1400 offer a high degree of parallelism. You can run 4 ALUs + 2 AAUs (or 1 AAU + 1 BMU) all in one core clock cycle. The million multiply accumulates per second (MMACS) is an industry standard for DSP performance. Because each of the four ALUs supports its own MAC, the SC1400 running at 300 MHz supports 1200 MMACs (refer to **Equation 1**).

Equation 1

$$1\ core \times 4\ MACs \times 300\ MHz = 1200\ MMAC$$

5.2 Instruction Cache (ICache)

Each MSC711x device has a 16 KB, 16-way ICache. There is no data cache. One way is 4 lines, and a line is 256 bytes. The SC1400 core can run instructions out of the ICache in one core clock cycle just as it runs application code out of M1.

When the core runs an instruction directly out of the ICache, a cache hit occurs. A cache miss occurs when the instruction fetch unit (IFU) in the ICache pulls the instruction from either M2 or external DDR. Depending on how the IFU is programmed, a ICache miss fetches 16, 32, or 64 bytes. If prefetch is enabled, it fetches to the end of the 256-byte line. For example, suppose you run an instruction out of M2 memory starting at hexadecimal address 0x0100_0000, and an ICache miss occurs. The IFU is programmed to pull in 16 bytes, so it pulls instructions from address 0x0100_0000 to 0x0100_000F. If prefetch is enabled, it fetches to the end of the line or from address 0x0100_0010 to 0x0100_000FF. For the first IFU fetch, the core actually stalls while waiting for an instruction. However, the prefetch works in parallel with the core, so there are no core stalls. A prefetch is based on spatial locality; the application code that runs next is typically right after the application code currently running.

You can either lock parts of the ICache or use the least recently used algorithm to replace old application code with new application code. The ICache is locked in 1 KB increments for critical application code or application code that is used repeatedly so that it is inefficient to store it in M1 memory. Locked section(s) of ICache do not use the LRU algorithm. The ICache is divided into four least recently used (LRU) sections. The minimum size for LRU replacement is 16 bytes.

Figure 5 shows the ICache overhead (in percent) with prefetch turned on and off. To support single-clock access, application code is stored in M2 rather than M1 memory The overhead percentages in **Figure 5** are only approximations. The main point is that the overhead of using the ICache with prefetch turned on is low compared to running an application code out of M1 memory. The x-axis in **Figure 5** shows mainly vocoders with prefetch turned on and off for comparison purposes. SIP10 consists of application control code. Notice that *AMR compiled 1ch* has a performance overhead of 2.8 percent with prefetch turned off and 0.8 percent with prefetch turned on. The worst case ICache overhead with prefetch off is premium voice G.729I at approximately 9 percent with prefetch turned off (1.8 percent with prefetch turned on). The worst case ICache overhead with prefetch on is 2.3 percent (9% with prefetch turned on.) There is not a big penalty for using ICache with prefetch turned on, only between 0.5 and 2.3 percent.

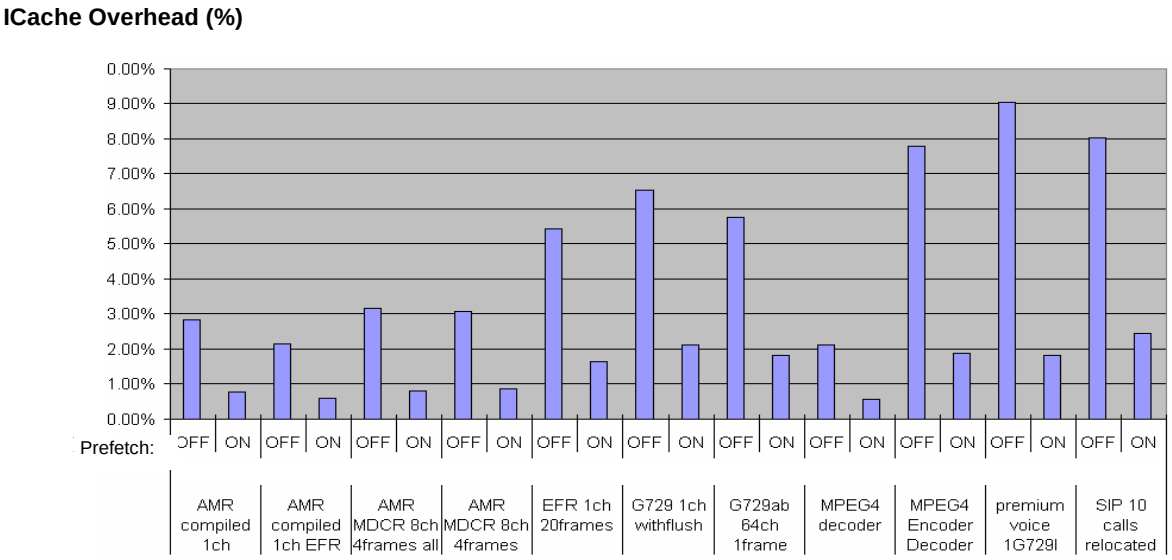


Figure 5. ICache Performance Overhead (application code in M2)

If you run application code out of M1 memory, there is no performance overhead because M1 memory supports accesses of one core clock. If the application code runs from M2 memory without the ICache, performance can be several hundred percent slower than running the code from of M1 memory. With the ICache and prefetch turned on, the performance is comparable to running application code out of M1 memory—with an additional small percentage of overhead. The ICache therefore reduces the need for a larger M1 memory space.

5.3 Extended Core Interface (ECI)

The extended core interface (ECI) enables the SC1400 core to communicate with blocks outside the extended core. It contains a 0 wait state, 4-entry × 64 bit FIFO called a write buffer. When the write buffer is enabled, all core writes except to M1 memory are queued to prevent the SC1400 core from stalling. The write buffer queues up only writes (not reads) from the core. It boosts core performance because the core does not have to finish write transactions to entities outside the extended core, stalling to wait for the access to complete. Instead, external accesses are first written to the write buffer, which releases the core and then completes the access when its destination becomes available. Not all writes beyond the M1 memory are routed through the write buffers. Write accesses do not use the write buffer in the following cases:

- The address of the destination belongs to a bank that is defined as immediate.
- It is an atomic operation essentially writing to a semaphore.
- The write buffer is disabled.

The write buffer counts the number of clocks that elapse between the time data is written to the write buffer and the time it is emptied. When the counter exceeds a pre-programmed value, the contents of the write buffer are flushed so that the time for the write accesses through the write buffer can be limited. There is an “immediate access” mode to bypass the write buffer, which improves latency through the ECI because the writes are not buffered. The user specifies a range of addresses to bypass the write buffer. The write buffer is flushed when it is turned off, a flush command executes, the watchdog timer times out, or there is a read from a pending write address.

5.4 Examples of Stalling the Core

Following are example situations in which the SC1400 core stalls:

- The SC1400 core performs a read operation from a module outside the extended core. The write buffer is used only to write, not read from outside the extended core.
- The write buffer is full, which is typically not the case because it is a four-entry buffer.
- A write then a read to the same address occurs outside the extended core. The write is buffered by the write buffer but because of the latency of the write buffer, the read can occur before the write. The write buffer recognizes when a read to the same address executed after the write and flushes the write buffer before the read is allowed to execute.
- The ICache IFU performs a fetch.

5.5 On-Chip Emulator (OCE)

As shown in **Figure 6**, the on-chip emulator (OCE) module connects to the core and internal buses (P, XA, XB). It is a non-intrusive way to interface with the SC1400 core and its peripherals so that you can examine registers, memory, or on-chip peripherals as well as define breakpoints and read the trace-FIFO. The emulator is accessed through the JTAG port or the core under software control. It works in parallel with the core. The emulator contains an 8 KB trace buffer, breakpoint units, up/down counters, selector, transmit/receive registers, and control logic.

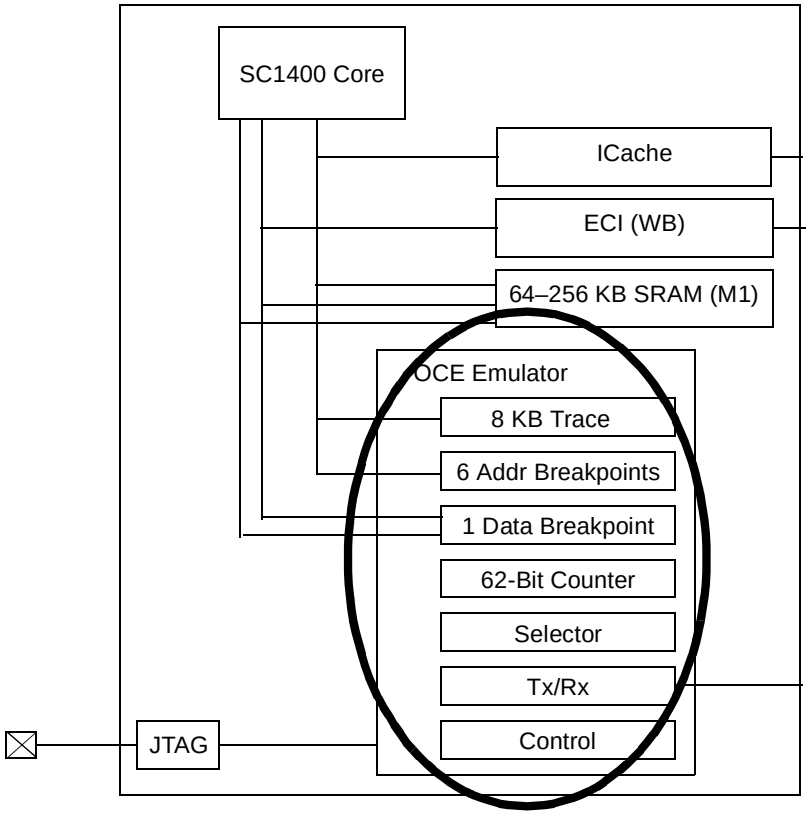


Figure 6. On-Chip Emulator (OCE)

Figure 7 shows the 8 KB emulator trace buffer, which can capture any combination of the following: normal variable-length execution set (VLES) instructions, change-of-flow instructions (such as interrupt or branch instructions), loops, interrupts, mark instructions, and emulator counter values.

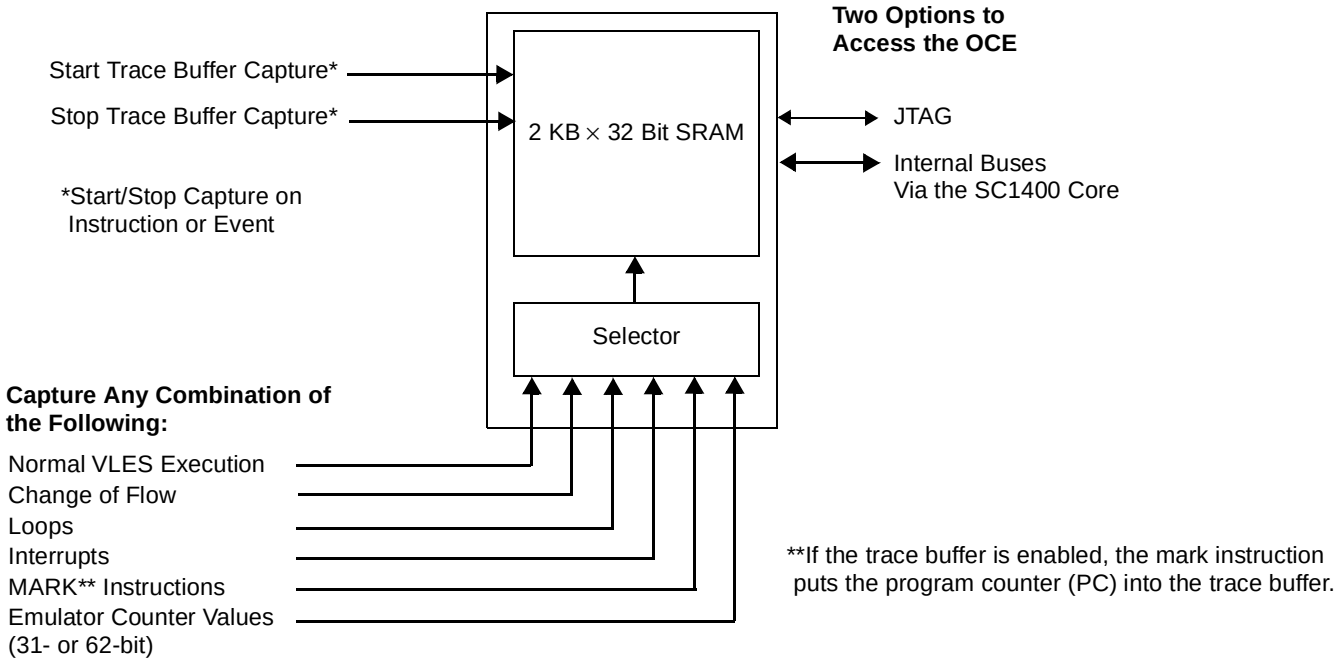


Figure 7. OCE Trace Buffer (8 KB)

Figure 8 shows the OCE counter, which can be configured as one 31-bit counter or two 31-bit counters cascaded together. The counters can be clocked using the core clock, number of instructions executed, debugev instructions, external pins, or trace captures.

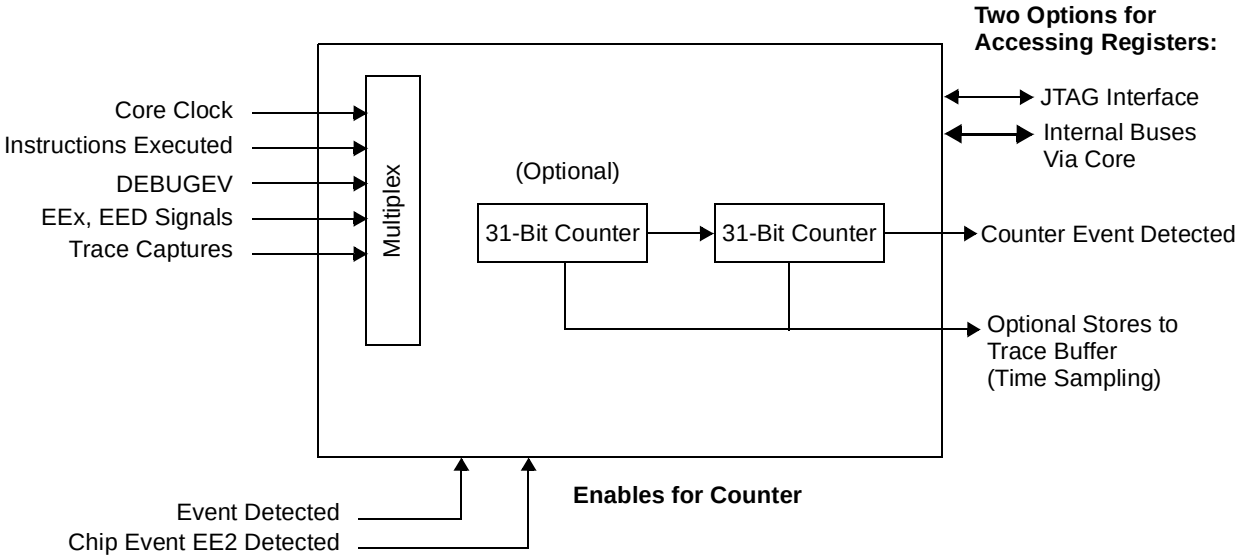


Figure 8. OCE Emulator Counter

6 Data Transfer Subsystem

Figure 9 depicts the data transfer subsystem, which manages all data flow through an MSC711x device. As the figure shows, the components of this subsystem are a crossbar switch, a DMA controller, ROM and M2 memory, and bridges to the peripheral block.

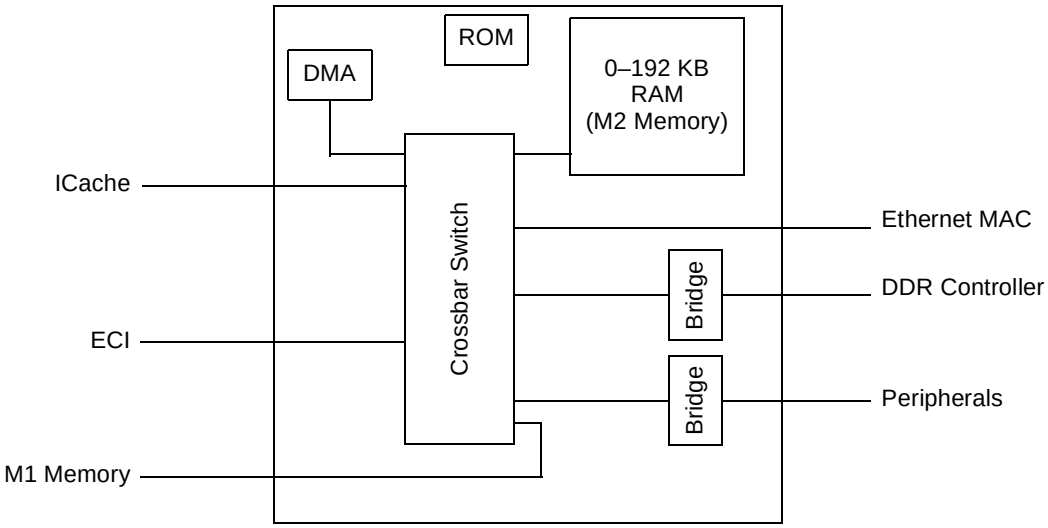


Figure 9. Data Transfer Subsystem

6.1 Crossbar Switch

At the heart of the data transfer subsystem is the crossbar switch, which is a four layer switch that conducts up to four parallel transfers from a master to a slave port with zero wait states. Four masters and six slave devices connect to the crossbar. The four master ports are as follows:

- ICache instruction fetch unit.
- Extended core interface with write buffer.
- DMA controller.
- Ethernet MAC DMA engine.

The six slave ports are as follows:

- M1 and M2 memory spaces.
- DDR controller.
- Three internal peripheral buses.

The crossbar supports buses of different sizes. The ICache bus is 128 bits, and the M1 memory, ECI and DMA controller use 64-bit buses. **Figure 10** the crossbar switch with all four transactions occurring in parallel.

- Ethernet DMA to M1.
- From ECI master writing to the timers.
- A cache burst from M2.
- DMA transfer to DDR.

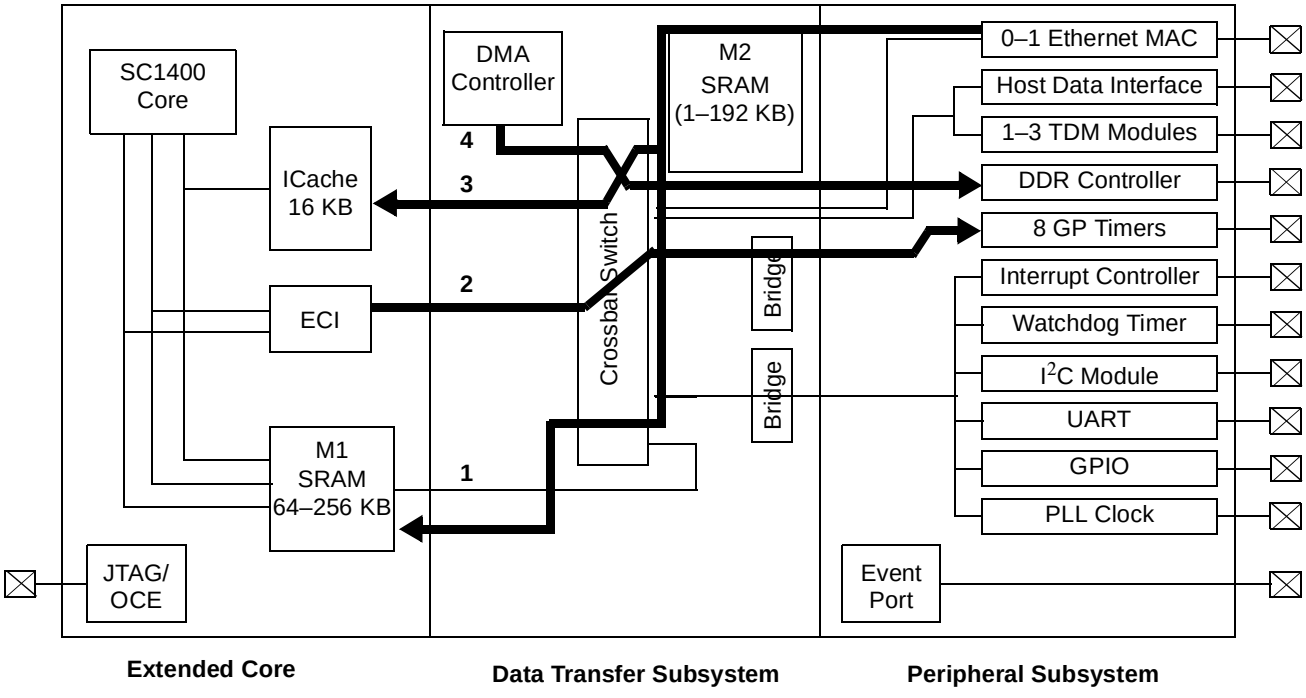


Figure 10. Example Using the Crossbar Switch

The crossbar switch has two arbitration schemes:

- Fixed-priority.
- Round-robin.

The arbitration scheme is independently programmable for each slave port. If multiple masters simultaneously request use of a slave port, arbitration logic selects the highest-priority master and grants it ownership of the slave port. All other masters requesting that slave port stall until the higher-priority master completes its transactions.

6.2 DMA Controller

The DMA controller works in parallel with the SC1400 core, as follows:

- 32 independent, bidirectional channels.
- Round-robin or fixed-priority arbitration scheme.
- Master on the crossbar switch.
- Single transfers of 8, 16, 32, 64 bits of data.
- Bursts of 256 bits (4 beats of 64 bits).

Figure 11 shows an example DMA transfer using one DMA channel to transfer 32 bytes of data from M1 memory to an external DDR device.

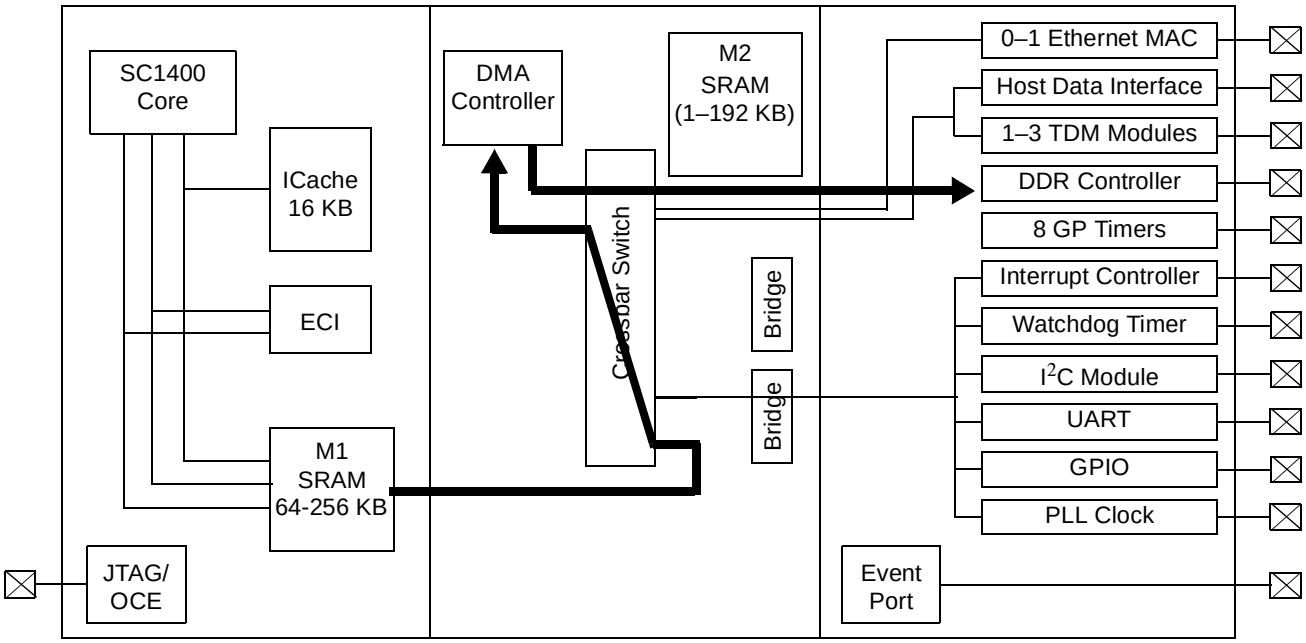


Figure 11. Example DMA Transfer

The DMA controller reads 32 bytes from M1 memory through the crossbar to a 32-byte DMA buffer. Next, it writes 32 bytes to the DDR device through the crossbar switch. These two transactions make up on one channel. In the MSC81xx family, such a transaction is treated as two channels. As shown in **Table 4**, MSC7118 and MSC7119 DMA throughput uses a DDR prefetch buffer. **Table 7** shows the estimated DMA throughput for the MSC7118 and MSC7119 transferring 512 bytes in 32-byte bursts using a 16- and 32-bit DDR bus.

Table 7. MSC7118/MSC7119 DMA Throughput

Type	DDR	Core Clock Cycles (MBps at 300 MHz)
16-bit	M1 memory to DDR	288 cycles (533 MBps)
	DDR to M1 memory	352 cycles (436 MBps)
32-bit	M1 memory to DDR	288 cycles (522 MBps)
	DDR to M1 memory	286 cycles (537 MBps)

Notice that a write to DDR using the DMA controller is the same for a 16-bit as for a 32-bit DDR interface because both interfaces must accommodate the maximum performance of the internal DMA controller. You may wonder why a 32-bit DDR interface is even used for the MSC7118 and MSC7119. There are two reasons. With a 32-bit interface, there are fewer accesses on the bus, possibly reducing power. Also, the read throughput is faster for a 32-bit DDR.

7 Peripheral Subsystem

Figure 12 shows the peripheral subsystem, which drives data into and out of the MSC711x device.

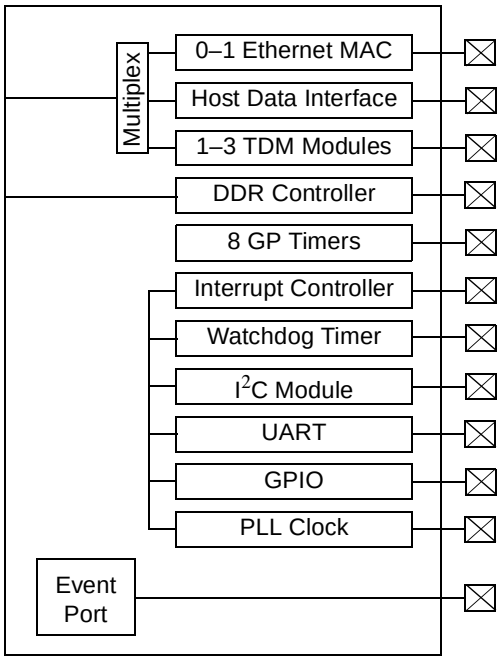


Figure 12. Peripheral Subsystem

The peripheral transfer block contains the following components:

- 0–1 Ethernet MAC.
- 8- or 16-bit host interface (HDI16).
- 16- or 32-bit DDR controller.
- 1–3 TDMs.
- Eight general-purpose timers.

- One interrupt controller versus three on the MSC81xx family.
- Watchdog timer.
- I^2C module, which is a two-wire synchronous interface that can be clocked at up to 400 KHz.
- Universal Asynchronous Receiver/Transmitter (UART) controller.
- Up to 46 GPIO signal pins.
- Clock, which contains a phase lock loop (PLL).
- Event port to work with the OCE port. Based on predefined events, the event port can trigger other events, such as interrupts, start/stop timers, and DMA. The event port can toggle events with no core processing except setting up the event port.

The remainder of this section focuses on the Ethernet, time-division multiplexing, and the DDR controller.

7.1 Ethernet

The MSC7113, MSC7116 and MSC7119 devices contain an Ethernet MAC, which connects to an Ethernet PHY (transceiver) or directly to another Ethernet MAC. Two Ethernet interfaces, both of which operate at 10 or 100 Mbps and full or half duplex, are supported:

- Media-independent interface (MII). An 18-wire interface that is an **IEEE** Std. 802.3™ standard. It contains four transmit and four receive data lines.
- Reduced media-independent interface (RMII). A 10-wire interface that is an industry standard. It contains two transmit and two receive data lines.

The Ethernet MAC can accept or reject a multicast broadcast address or a point-to-point 48-bit unicast address, as well as multicast addressing. It can operate in promiscuous mode. The Ethernet MAC contains its own DMA engine that processes 32-byte bursts. The DMA controller in the data transfer subsystem is not used to transfer data to/from the Ethernet DMA engine, which offloads the SC1400 core and the DMA controller. The built-in Ethernet MAC has an internal loopback feature to test application code without sending data outside the device.

7.2 Host Interface (HDI16)

Each MSC711x device has a high-speed parallel port HDI16 interface to connect to an external host. The external host initiates all read/write transactions, and the HDI16 handles 8- or 16-bit data transfers. The HDI16 is a slave-only interface that looks like a memory-mapped asynchronous SRAM interface. The host has no direct access to the MSC711x internal memory. The host processor writes to a host buffer inside the HDI16, and the MSC711x SC1400 core or DMA controller transfers the data. The SC1400 core or DMA controller can be triggered when the internal HDI16 buffer is full or empty. **Figure 13** shows a glueless interface between a MSC81xx 60x host and the MSC711x HDI16.

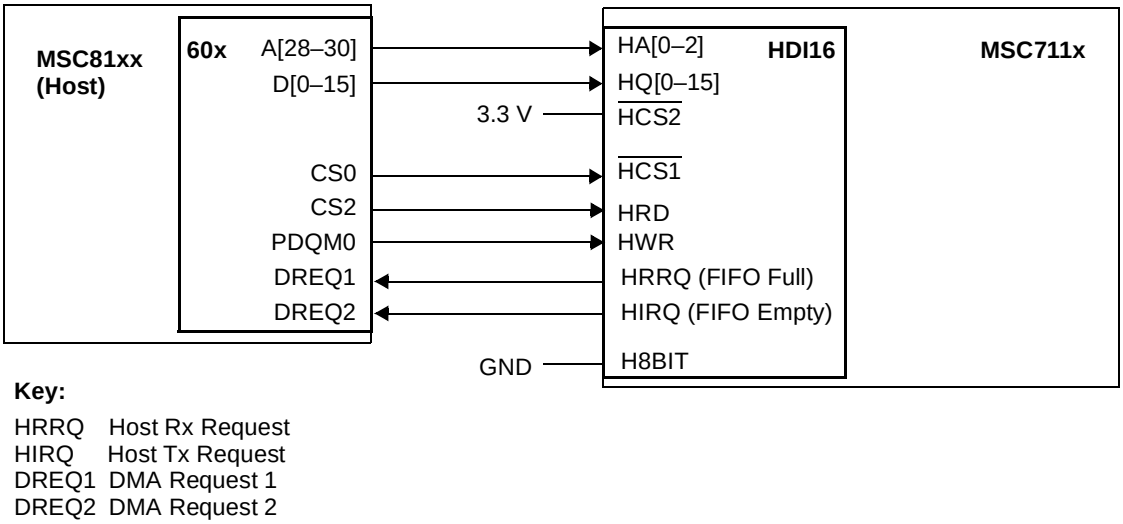


Figure 13. MSC81xx 60x Bus to MSC711x HDI16

The MSC81xx 60x address bus connects to three address lines of the MSC711x HDI16 (HA[0–2]). In **Figure 13**, H8BIT is grounded, so the HDI16 operates as a 16-bit host interface (HD[0–15]). $\overline{\text{HCS1}}$ and $\overline{\text{HCS2}}$ are ORed together. To address multiple MSC711x devices individually, you can use multiple chip selects and/or address decoding. The polarity of the $\overline{\text{HCS1}}$ and $\overline{\text{HCS2}}$ signal pins is programmed via the HPCR[HCSP] bit. The HRD and HWR lines are control lines to the HDI16 interface to indicate read/write access.

In the example depicted in **Figure 13**, when the HDI16 interface has data for the host to read, the MSC711x device asserts HRRQ to trigger DREQ1 (DMA request 1) on the host. DREQ1 can be programmed to trigger the host DMA controller to begin reading data from the HDI16 receive buffers. When the HDI16 transmit FIFO is empty, the MSC711x asserts HTRQ to trigger DREQ2 (DMA request 2) on the host. DREQ2 can be programmed to trigger the host DMA controller to begin writing data to the HDI16 transmit buffers.

7.3 Time-Division Multiplexing (TDM)

MSC711x devices support between one and three TDMs, each with the following features:

- Up to 128 channels.
- Up to 50 Mbps.
- 8/16 bit channel sizes.
- Glueless connection to E1/T1 framers, H.110, SCAS, and MVIP.
- A/µ-law conversion according to 8-bit compander (compression and expansion) schemes. A-law is 13 bits, µ-law is 14 bits. Both are padded to 16 bits with the right bits cleared to zero.
- Generates/receives clock and frame sync signals.
- Operation in independent or shared mode.

Figure 14 and **Table 8** show the difference between independent and shared mode. In independent mode, the TDM is a six-wire interface. In shared mode, the TDM is a four-wire interface in which the transmit and receive clocks are shared on one line, and the transmit and receive frame syncs are shared on one line. The MSC711x clock and frame sync signals are bidirectional, as on the MSC8122. The MSC8101 TDM clock and frame sync are all inputs.

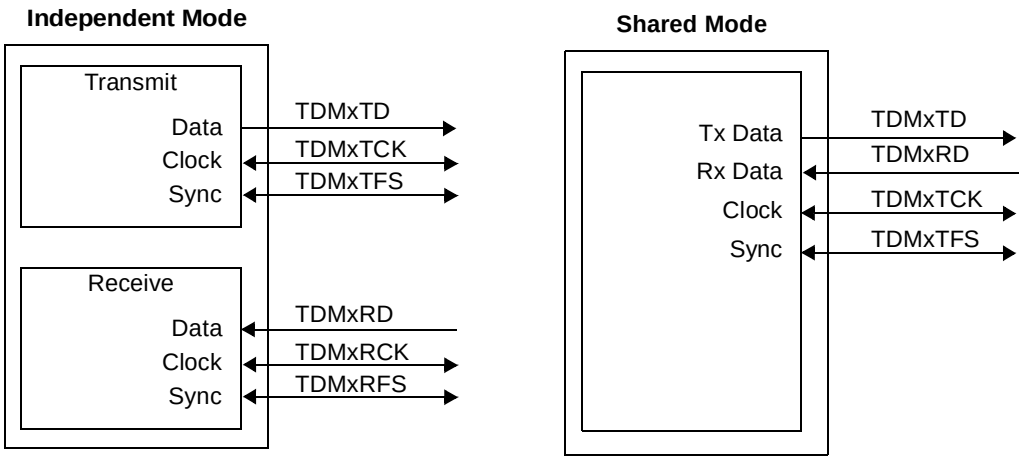


Figure 14. TDM Independent and Shared Modes

Table 8. TDM Independent and Shared Modes Signals

TDM Independent Mode	TDM Shared Mode
Transmit Data	Transmit Data
Transmit Clock	Transmit/Receive Clock
Transmit Frame Sync	
Receive Data	Receive Data
Receive Clock	
Receive Frame Sync	Transmit/Receive Frame Sync

7.4 Double Data Rate (DDR) Controller

The built-in DDR controller supports DDR1 SDRAM and runs at half the core speed. For example, if the SC1400 core runs at 300 MHz, the DDR controller runs at 150 MHz. The DDR can output data on both the rising and falling clock edges in comparison to only one clock edge for the older SDRAM technology. A DDR controller running at 150 MHz requires a DDR 300 or faster DDR memory. As **Figure 15** shows, the MSC711x family supports one 16-bit DDR or one-32 bit (or two 16-bit) DDR for additional performance. The 16-bit DDRs are more common, but 32-bit DDRs are available. Two 16-bit DDR memories require more board space than one 16-bit or one 32-bit DDR memory device.

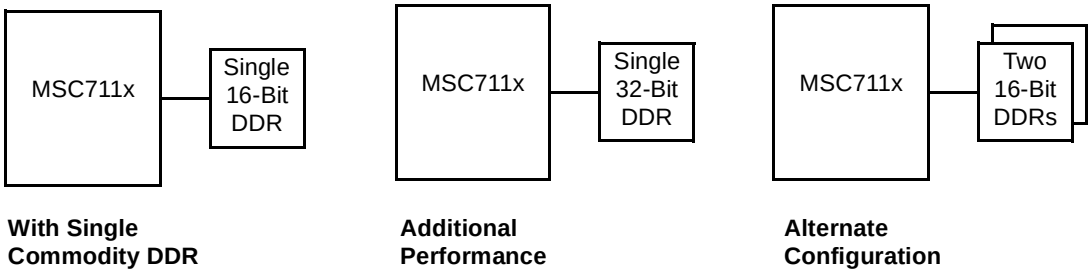


Figure 15. MSC711x DDR Configurations

The MSC711x DDR controller supports a 14-bit address bus to address up to 1 GB of memory. The DDR controller supports the JEDEC JESD79D and JEDEC SSTL_2 (Stub Series Termination Logic) standards. Dynamic power management mode gives the user tight control of power consumption by trading power for performance. In sleep

mode, the DDR memory controller can be configured to take advantage of self-refreshing SDRAMs or to provide no refresh support. You can turn sleep mode on or off depending on whether the DDR is self refreshing. Self refreshing occurs at the end of a cycle and before the next cycle begins, adding a one-cycle performance hit.

Auto precharge mode causes the DDR controller to issue an auto precharge command with every read or write transaction. In addition, auto precharge mode can be enabled for separate chip selects.

7.4.1 DDR Circuit Configurations

DDR supports two circuit configurations: active termination and push pull (or passive). Active consumes more power but switches more rapidly and offers cleaner signals. Passive circuit configurations require less power. The MSC711x DDR supports SSTL-2. SSTL is adopted by a Joint Electronic Device Engineering Committee (JEDEC)) standard and is endorsed by major memory module, workstation, and PC manufacturers. SSTL is optimized for the main memory environment, which has long stubs off the bus due to the routing traces. SSTL-2 indicates that this is 2.5 V SSTL logic. SSTL-2 inputs are typically a differential pair common source amplifier with one input connected to Vref. As **Figure 16** shows, Vref is 1.25 V. Active DDR lines are terminated via a resistor (RT in **Figure 16**). RT is 25 Ω for the SSTL-2 class 2 specification and 50 Ω for class 1. Class 2 is a more stringent specification than class 1. For both circuit configurations, RS is typically 0 Ω for a short stub (trace) to 25 ohms for longer stub.

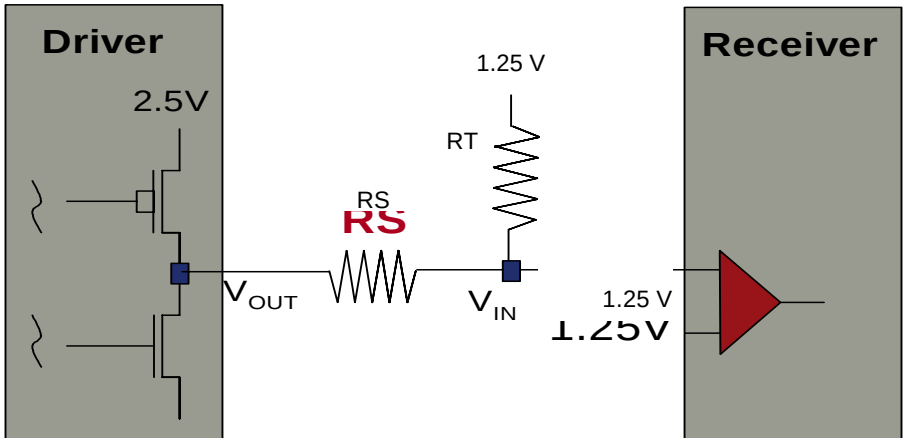


Figure 16. DDR SSTL-2

8 Field Built-In Self-Test (fieldBIST)

Through JTAG and CLKIN (clock in), fieldBIST provides the means to isolate an MSC711x device and test internal logic, memory, and the PLL. fieldBIST is not accessible through the SC1400 core. fieldBIST ensures that the device has structural integrity, operates at the rated speed, and is free from reliability defects. fieldBIST diagnostics can report partial or complete device inoperability. As **Figure 17** shows, the fieldBIST components are:

- Three logic built-in self test (LBIST) controllers to test the SC1400 core, peripherals and other miscellaneous logic grouped under the name “top logic.” Top logic connects internal peripherals to the core and to the pads. The LBIST controllers test over 95 percent of the internal logic and are independent of temperature and voltage.
- Six memory built-in self test (MBIST) controllers to test 100 percent of the internal memory, including M1, M2, the ICache, ROM, DMA, and the trace buffer. Unlike the LBIST tests, MBIST tests are dependent on voltage, temperature, and frequency.
- One PLL BIST controller to test for excessive PLL jitter.

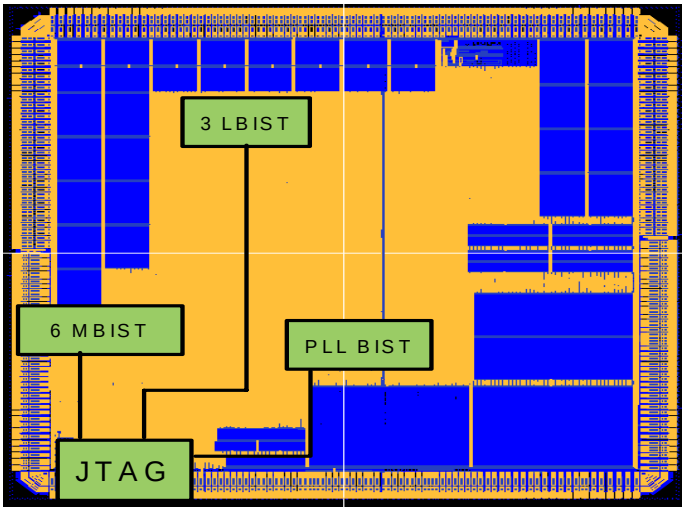


Figure 17. fieldBIST

9 MSC711x Evolution and MSC81xx Comparison

This section describes the progression across all three generations of Freescale StarCore-based DSPs. As **Figure 18** shows, the first-generation MSC8101/MSC8103 contain a StarCore SC140 core and a large 512 KB of internal SRAM to hold application code to run and critical data. The CPM is used for networking (TDM, Ethernet, SPI, I^2C, UART, and so on). The 60x bus connects the device to external memory.

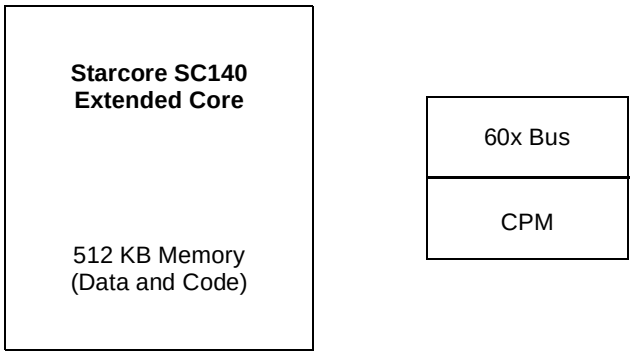


Figure 18. First Generation: MSC8101/MSC8103

As **Figure 19** shows, the second-generation MSC8102 contains four SC140 extended cores, each with its own memory and ICache.

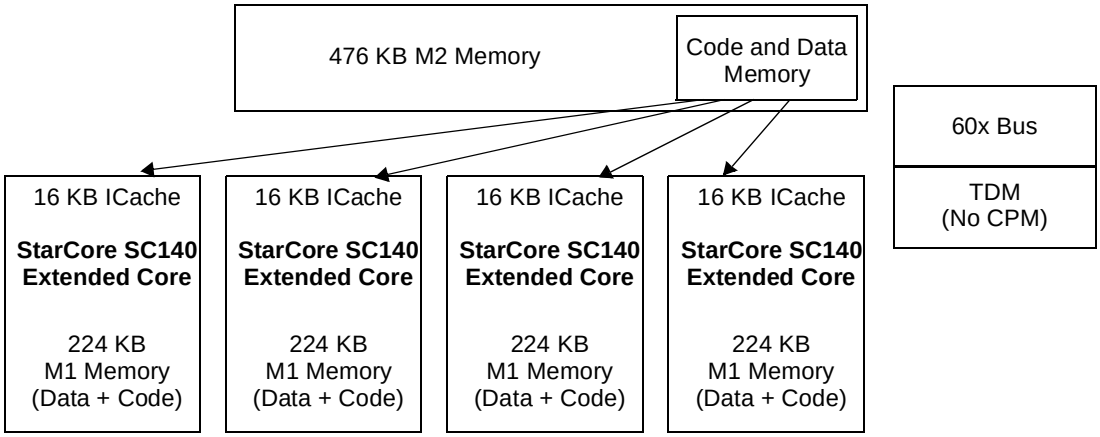


Figure 19. Second Generation: MSC8102/MSC8122/MSC8126

The MSC8102 M1/M2/ICache memory hierarchy is similar to that of the MSC711x family. The MSC8122 is similar to the MSC8102, but adds Ethernet, runs at a higher frequency, and uses a lower core voltage. The MSC8102 has TDM and UART interfaces but does not contain a CPM as do the first-generation MSC8101/MSC8103 devices. As **Figure 20** shows, the third-generation MSC711x contains one SC1400 extended core.

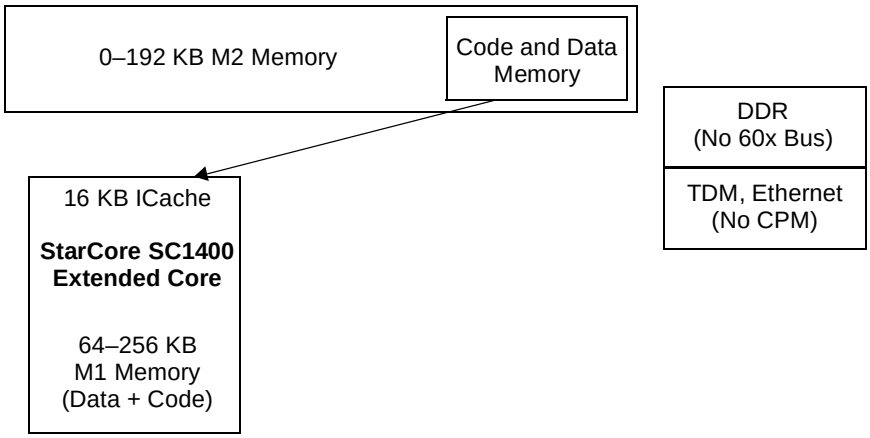


Figure 20. Third Generation: MSC711x

There is no 60x bus as in the MSC81xx family, but there is a DDR interface. It has no CPM, but it offers similar functionality in the TDM, Ethernet, UART and I^2C interfaces.

9.1 Blocks Reused from MSC81xx

Knowing which MSC81xx modules are reused in MSC711x devices may assist you in software reuse if you are migrating to an MSC711x device. All MSC711x devices reuse the following modules, which are common to all MSC81xx devices: SC140 core (called the SC1400 core in MSC711x DSPs), the JTAG module, and the EOnCE module (called the OCE in MSC711x DSPs). In addition, MSC711x devices reuse the following modules specific to the first and second generations of StarCore DSPs:

- MSC8101/MSC8103 host interface, HDI16.
- MSC8102/MSC8122/MSC8126 M1/M2 memory hierarchy.

9.2 MMACS

Table 9 compares the number of MMACS for the MSC711x and MSC81xx families. The MSC711x performs at up to 1200 MMACs, which is the same number for the MSC8103. The MSC8101 EFCOP adds 300 more MMACS to the MSC8101 performance. The MSC8102, MSC8122, and MSC8126 are quad-core devices that therefore support a much higher number of MMACS in addition to running at a higher frequency.

Table 9. MMACS (Million Multiply Accumulates Per Second)

DSP	MMACS
MSC7110/2/3/5/6 MSC7118/9	1064 MMACs @ 266 MHz 1200 MMACs @ 300 MHz
MSC8103/MSC8101	1200/1500 MMACs @ 300 MHz
MSC8102	4400 MMACs @ 275 MHz
MSC8122/MSC8126	8000 MMACs @ 500 MHz

9.3 MSC711x and MSC81xx High-Level Comparison

Table 10 compares a the MSC711x and MSC81xx families at a high level. All devices contain a minimum of one SC140x core, large internal SRAM, and either an HDI16 or direct slave interface (DSI) host interface. The MSC8101/MSC8103 and some members of the MSC711x family (MSC7113, MSC7116, MSC7119) support 10/100 Mbps Ethernet MAC. The MSC8101/MSC8103 and MSC711x have the smallest package size. The MSC8101/MSC8103 have a communications processor module (CPM). The MSC811x has a multi-master 60x bus. MSC711x devices offer DDR, lowest device power, and lowest device cost.

Table 10. Overview of StarCore-Based DSPs

Feature	MSC8122/ MSC8126	MSC8102	MSC8101/ MSC8103	MSC711x
StarCore Core	X	X	X	X
Internal SRAM	X	X	X	X
HDI16 or DSI	X	X	X	X
10/100 Mbps Ethernet	X		X	X
Smallest package size			X	X
CPM (microcode)			X	
60x-compatible bus (multi-master)	X	X	X	
DDR controller				X
Lowest device power				X
Lowest device cost				X

10 Documentation

Table 11 lists documentation available at for the MSC711x at the web site listed on the back cover of this application note.

Table 11. MSC711x Documentation

Document	Description
MSC711x Technical Data sheets	Individual data sheets for each device provide the features list and physical, electrical, timing, and package specifications.
MSC711x chip errata	Known problems and suggested workarounds.
MSC711x Reference Manual (MSC711xRM) *MSC7118 Reference Manual* (MSC7118RM) *MSC7119 Reference Manual* (MSC7119RM)	Detailed functional description of the MSC711x memory and peripheral configuration, operation, and register programming.
StarCore SC140 DSP Core Reference Manual	Detailed description of the SC140 family processor core and instruction set.
SC1000 Family Processor Core Reference Manual (10180-01). See the StarCore LLC web site at www.starcore-dsp.com.	Detailed description of the SC1000 family processor cores, including the SC1400, and instruction set.
OCE10 On-Chip Emulator Reference Manual (10055-03). See the StarCore LLC web site at www.starcore-dsp.com.	Information on the architecture and programming model of the OCE10 on-chip emulator, which is the StarCore implementation of the EOnCE™. The OCE10 on-chip emulator is a peripheral that facilitates debugging the StarCore SC1000-family processor core and peripherals.
Application notes	A growing list of application notes.

11 Customer Support

Customer support is available at the web site listed on the back cover of this application note. When submitting questions, be specific about the product or family of interest to you—for example, MSC711x family or MSC7115 device. You can also contact your local Freescale sales office.

12 Acronyms and Abbreviations

AAU	address arithmetic unit
AGU	address generation unit
ALU	arithmetic logic unit
BFU	bit field unit
BIST	built-in self test
BMU	bit mask unit
CLKIN	clock in
CPM	communication processor module
DDR	double data rate
DMA	direct memory access
DREQ1	DMA request 1
DREQ2	DMA request 2
DSI	direct slave interface
ECI	extended core interface
EFCOP	enhanced filter coprocessor
EFR	enhanced full rate
fieldBIST	field built-in self test

GB	gigabyte
GBps	gigabytes per second
Gbps	gigabits per second
GPIO	general-purpose I/O
GSM	Global System for Mobile Communication
HDI16	host interface
HRRQ	host receive request
HTRQ	host transmit request
I^2C	inter-integrated communication
IAD	integrated access device (router, voice gateway)
ICache	instruction cache
IFU	instruction fetch unit
I/O or IO	input/output
JEDEC	Joint Electronic Device Engineering Committee
JTAG	Joint Test Action Group
KB	kilobyte
LBIST	logic built-in self test
LRU	least recently used
MAC	media access controller
MAC	multiply accumulate
MAP	molded array package
MAP-BGA	molded array package ball grid array
MBIST	memory built-in self test
MBps	megabytes per second
Mbps	megabits per second
MHz	megahertz
MII	media-independent interface
MMAC	million multiply accumulates per second
ms	millisecond
OCE	on-chip emulator
PHY	physical interface
PLL	phase lock loop
PV	premium voice (G.729AB, and so on)
ROBO	remote office/branch office
RoHS	restriction of hazardous substances
RAM	read access memory
RMII	reduced media-independent interface
ROM	read-only memory
R/W	read/write
SOHO	small office/home office
SPI	serial peripheral interface
SRAM	static random access memory
SSTL_2	Stub Series Termination Logic - 2.5 V logic
SW	software

TB	trace buffer
TDM	time-division multiplexing
UART	universal asynchronous receiver/transmitter
V	volt

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