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MSC711x Memory Controller Usage Guidelines

Supporting Double Data Rate (DDR) SDRAM Devices

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The MSC711x memory controller supports double data rate synchronous dynamic random access memory (DDR SDRAM) devices, which are designed to be a high data rate migration path from the standard single data rate (SDR) memory devices. This application note examines the basics of DDR, provides general board-level design guidelines for using the MSC711x DDR, and illustrates these concepts with MSC711x memory controller initialization and timing examples.

CONTENTS

1 DDR SDRAM Basics

In addition to the basic functionality of SDR SDRAM devices, such as the command structure, DDR SDRAMs contain several enhancements:

- Double data rate
- Source synchronous operation
- Low voltage signaling
- Differential clocks

1.1 Double Data Rate

Unlike SDR SDRAM, which clocks data at the rising edge of the system clock, DDR SDRAM clocks data on both edges of the clock. This architecture transfers two data words per clock cycle so that it effectively doubles the bandwidth, as shown in **Figure 1**. For example, a DDR device that runs with a 100 MHz clock transfers data at 200 Mbits/sec per signal pin.

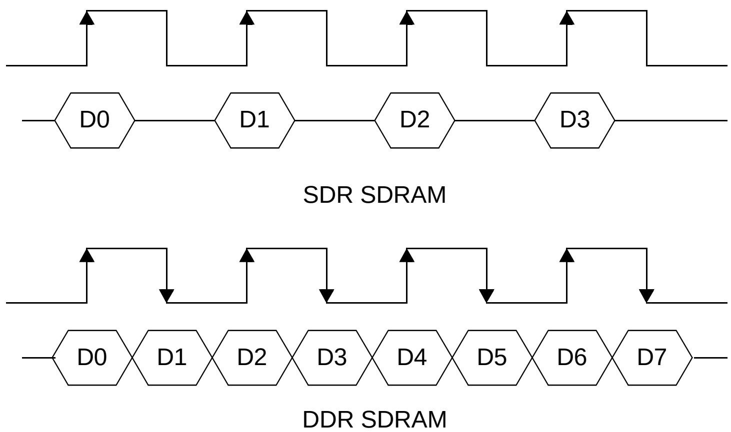


Figure 1. SDR Versus DDR SDRAM

1.2 Source Synchronous Operation

To reduce clock skew problems, a critical issue with high-speed buses, DDR SDRAM uses source synchronous data capture in which a bidirectional data strobe (DQS) is transmitted and received with the data. The data strobe is driven by the memory controller for write accesses and by the DDR SDRAM for read accesses. Including the data strobe loaded with the data gives all the signals in the group very similar electrical characteristics and allows for higher data rates.

1.3 Low Voltage Signaling

In addition to increased memory bandwidth over SDR, DDR also reduces power consumption by reducing supply voltages. DDR operates at 2.5 V, and SDR operates 3.3V. **Table 1** shows the four voltages that must be generated in a DDR system. The V_{DDQ} supplies power to the DDR SDRAM I/O, clock synthesizer, and output drivers. This supply operates at a nominal 2.5 V. The V_{DDQ} has the same specifications as the V_{DD}, and these two supplies are externally connected as one. To maintain signal integrity and to get high speed, the bus impedance is terminated through a resistor to the mid-level voltage, V_{TT}. The V_{TT} voltage tracks the mid-level reference voltage, V_{REF}. Both V_{TT} and V_{REF} operate at a nominal 1.25 V. Refer to **Section 2.1**, *Signal Termination*, on page 3 for more information on these voltages.

Table 1. DDR Voltages

Symbol	Parameter	Min	Nom	Max
V_{DD}	Device Supply Voltage	2.3 V	2.5 V	2.7 V
V_{DDQ}	Output Supply Voltage	2.3 V	2.5 V	2.7 V
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$
V_{TT}	Termination Voltage	$V_{REF} - 0.4$ V	V_{REF}	$V_{REF} + 0.4$ V

1.4 Differential Clocks

DDR uses a differential pair for the system clock and has a true clock CK and a complementary clock $\overline{\text{CK}}$. The crossing of CK going high and $\overline{\text{CK}}$ going low is the positive edge of CK. The crossing of CK going low and $\overline{\text{CK}}$ going high is the negative edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of the data strobe DQS and to both edges of CK.

2 Layout Considerations

Resistive signal termination schemes, printed circuit board (PCB) signal routing requirements, and generation and supply of required reference voltages are critical issues for a reliable DDR memory system. This section provides board designers with general recommendations in these areas. Another source of layout design considerations is the Freescale application note entitled *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582), which is available on the Freescale website listed on the back cover of this document.

2.1 Signal Termination

Systems that use DDR memory must terminate the DDR signals. Several methods for terminating DDR signals are offered in a JEDEC standard developed to provide signal reliability at high transfer rates, called stub series terminated logic at 2.5 V (SSTL_2). This standard offers adequate output current drive to permit parallel termination schemes and proper termination to reduce signal reflections. The typical SSTL_2 interface includes a single series resistor, r R_S, and a single parallel resistor, R_T. The R_S connects from the memory controller to the memory device and has a value between 10 and 30 Ω, typically 22 Ω. The R_T, typically between 22 and 28 ohms, is attached to the V_{TT} termination rail. Values for R_T and R_S are system-dependent and should be derived by board simulation. The SSTL_2 interface uses a reference voltage and differential input to determine the logic levels. The reference voltage, V_{REF}, is defined as half the supply voltage, V_{DD}, and the termination voltage, V_{TT}, equals the V_{REF}. **Figure 2** shows a typical output buffer and input receiver stage with SSTL_2 in a DDR SDRAM.

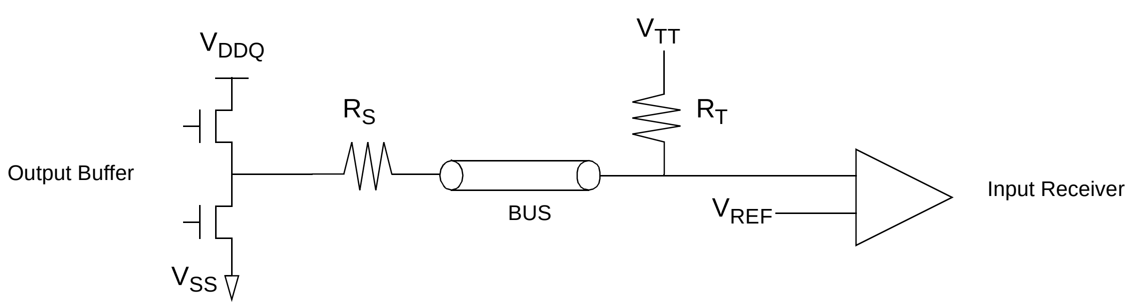


Figure 2. SSTL_2 Single Terminated Output

Figure 3 shows the MSC711x Application Development System (MSC711xADS), which implements an SSTL_2 single series and single parallel resistor termination scheme. Each data, address, and control signal connects to a 22 Ω series resistor and a 24 Ω parallel resistor.

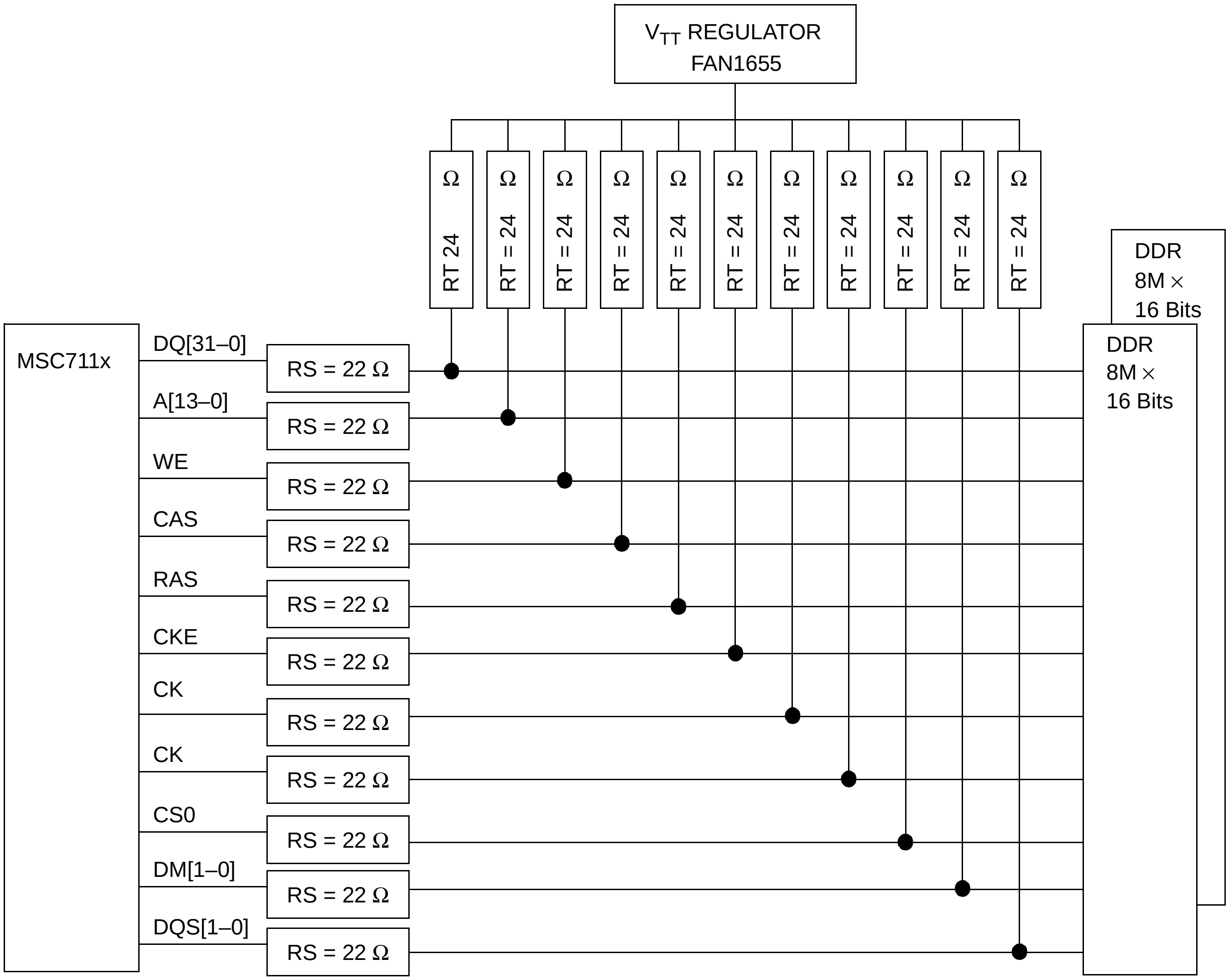


Figure 3. MSC711x to DDR Connection

2.2 Reference Voltage Generation

To avoid potential timing errors, jitter, and erratic memory bus behavior, the reference voltage V_{REF}, which controls the switching levels, must meet the following requirements:

- V_{REF} must track the midpoint of the signal voltage swing, generally $0.5 \times V_{DD}$ within 3 percent over all valid voltage, temperature, and noise level conditions.
- Each V_{REF} pin must use a proper decoupling scheme to keep the noise within the specified ranges by using 0.1 or 0.01 µF capacitors.
- A clearance of 20–25 mil should be kept between V_{REF} and other traces.
- The V_{REF} trace width should be routed at a minimum of 20–25 mil.
- V_{REF} and V_{TT} must be on different planes due to the sensitivity of V_{REF} to the termination plane noise.

- V_{REF} and V_{TT} must share a common voltage supply. Several off-the-shelf power solutions provide both the V_{REF} and V_{TT} voltages from a common circuit. The MSC711xADS uses the Fairchild Semiconductor FAN1655 low dropout regulator to ensure regulation of V_{TT} to $0.5 \times V_{DDQ} \pm 40$ mV. Other potential V_{TT} power solutions include:
  — Fairchild FAN1655, FAN6555, ML6554
  — Philips NE57814, NE57810
  — TI TL5002
  — National Semiconductor LP2995, LP2994
  — Semtech SC1110

2.3 PCB Signal Routing

DDR signals must be properly routed to guarantee reliable operation at the maximum supported DDR frequency. The following PCB layout guidelines ensure that designs operate at the highest possible frequencies:

- Do not route DDR signals on any PCB layer that is not directly adjacent to a common reference plane.
- Signals within a data lane should be routed on the same layer as they traverse to the memory devices and to the V_{TT} termination end of the bus. This recommendation helps to ensure uniform signal characteristics for each data lane.
- All clock pairs should be routed on the same layer.
- Match the data, data strobe, and data mask signals in each data lane in trace lengths (± 25 mm) to propagation delays, and minimize the skew.
- Separate data and control nets by a minimum of 0.5 mm to minimize crosstalk.
- Isolate signal groups via different resistor packs. Place the termination resistors on a top layer. The R_S resistors should be close to the first memory bank. The R_T should directly tie into the V_{TT} island at the end of the memory bus. Each of the following groups should use a resistor pack:
  — Data signals and data strobes
  — Address and command signals
  — Clock signals
- Route the data, address, and command signals in a daisy chain topology. Total trace lengths for any daisy-chained signal must not exceed 75 mm.
- Route control and clock signals point-to-point. Total trace lengths for any point-to-point signal must not exceed 50 mm.

3 DDR Memory Controller

The fully programmable MSC711x DDR memory controller provides a glueless interface to most Joint Electron Device Engineering Council (JEDEC)-compliant DDR SDRAM devices available today. Its features are:

- Glueless interface to JEDEC-compliant first generation DDR SDRAMs (DDR-I)
- 16-bit or 32-bit DDR SDRAM data bus
- Programmable DDR SDRAM timing parameters
- 14-bit DDR SDRAM address
- Two chip-select signals

- Single access or burst mode
- Data mask signals and read-modify-write
- Open page management
- Auto-precharge mode
- Sleep power management mode

Figure 4 shows a system-level view of the MSC711x connected to a DDR device. All accesses to the DDR memory controller occur from the AHB masters through the crossbar switch, which directly controls the DDR pins.

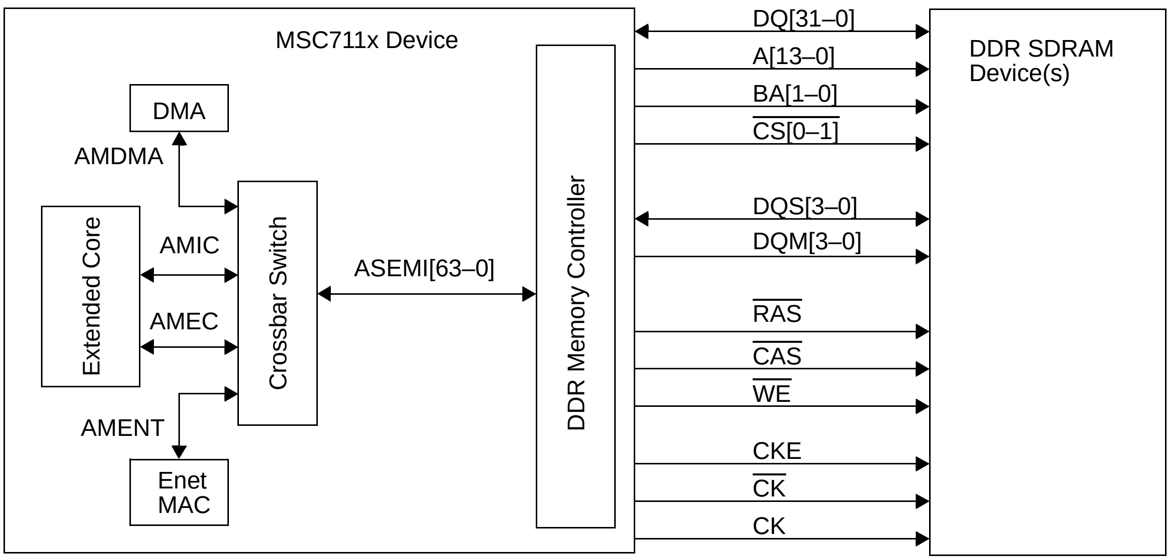


Figure 4. System-Level View of DDR Memory Controller

3.1 DDR Memory Controller Pins

The DDR memory controller external signals, depicted in **Figure 4**, are described as follows:

- DQ[31–0]. Data bus signals. The DDR memory controller supports a 16-pin or 32-pin data path size. DQ0 is the least significant bit.
- A[13–0]. Address bus signals. The DDR memory controller supports DDR device densities from 64 Mbit to 1 Gbit. A0 is the least significant bit.
- BA[1–0]. Bank address signals that specify the bank on which an ACTIVE, READ, WRITE, or PRECHARGE command is applied. BA0 is the least significant bit.
- $\overline{\text{CS[1–0]}}$. Chip-select signals that provide physical bank selection on systems with multiple banks. The DDR memory controller asserts these signals for memory accesses according to the bank starting and ending addresses.
- DQS[3–0]. Data strobe signals that are transmitted, along with data, by the DDR device during READ operations and by the DDR memory controller during WRITE operations. They are edge-aligned with data for READ operations and center-aligned with data for WRITE operations.
- DQM[3–0]. Data mask signals to prevent writing of unwanted data to the DDR device.
- $\overline{\text{RAS}}$. The row address strobe that, along with $\overline{\text{CS}}$, defines the command being entered.
- $\overline{\text{CAS}}$. The column address strobe that, along with $\overline{\text{CS}}$, defines the command being entered.
- $\overline{\text{WE}}$. The write enable signal that, along with $\overline{\text{CS}}$, defines the command being entered.

- CKE. The output clock enable signal.
- $\overline{\text{CK}}$ and CK. Differential clock signals. All addresses and control input signals are sampled on the crossing edge of the positive edge of CK and the negative edge of $\overline{\text{CK}}$.

3.2 DDR Commands

Table 2 shows the JEDEC DDR commands.

Table 2. DDR Commands

Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR
NO OPERATION (NOP)	L	H	H	H	H
ACTIVE	L	L	H	H	Bank/Row
READ	L	H	L	H	Bank/Col
WRITE	L	H	L	L	Bank/Col
PRECHARGE	L	L	H	L	Code
AUTO REFRESH or SELF REFRESH	L	L	L	H	x

3.2.1 NO OPERATION (NOP)

The NO OPERATION (NOP) command instructs the DDR SDRAM to perform a NOP by keeping $\overline{\text{CS}}$ low and $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ high. It prevents unwanted commands from being registered during idle or wait states. This command does not affect operations already in progress.

Table 3. DDR Commands, NOP

Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR
NO OPERATION (NOP)	L	H	H	H	H

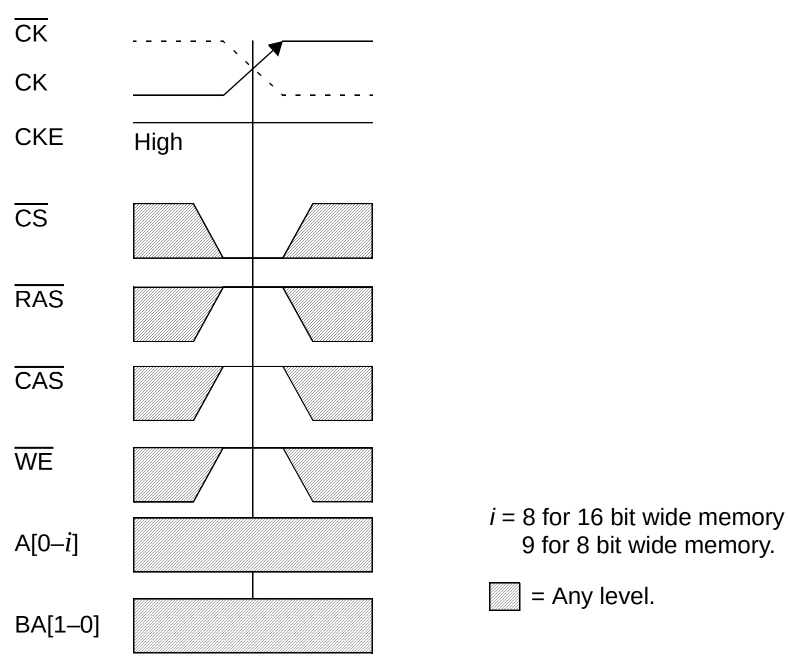


Figure 5. NOP Command

3.2.2 ACTIVE

The ACTIVE command opens or activates a row in a particular bank for a subsequent access. BA[0–1] select the bank, and A[0–11] provide the row address. A row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before a different row in the same bank is opened. When a bank is precharged, it is in the idle state and must be activated before any READ or WRITE commands are issued to that bank. A PRECHARGE command is treated as a NOP if there is no open row in the same bank.

Table 4. DDR Commands, ACTIVE

Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR
ACTIVE	L	L	H	H	Bank/Row

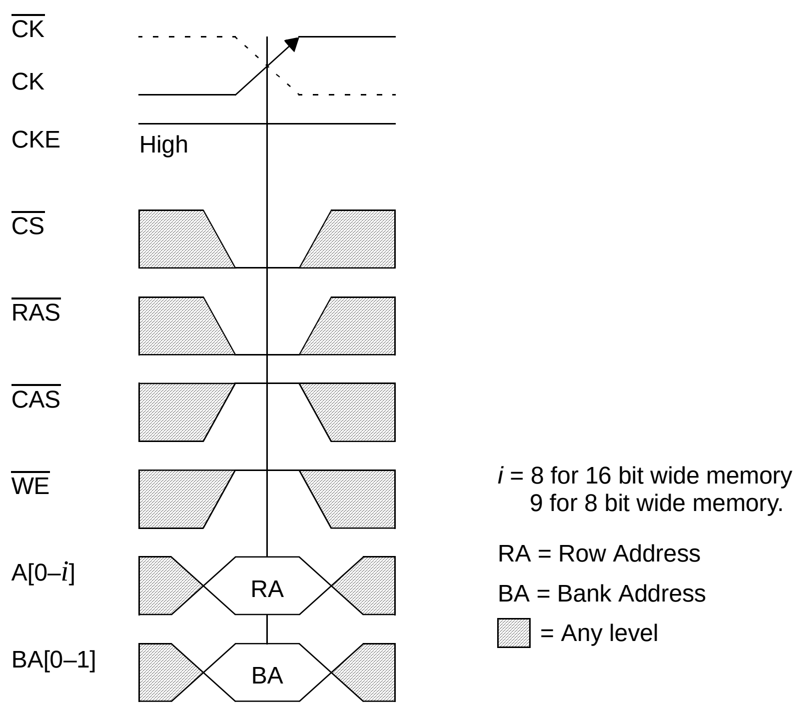


Figure 6. ACTIVE Command

3.2.3 READ

The READ command initiates a burst read access to an active row. BA[0–1] select the bank, and A[0–*i*] (where *i* = 8 for 16 bit wide memory and 9 for 8 bit wide memory) select the starting column address. The value on input A10 determines whether AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the accessed row is precharged at the end of the READ burst. If AUTO PRECHARGE is not selected, the row remains open for subsequent accesses.

Table 5. DDR Commands, READ

Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR
READ	L	H	L	H	Bank/Col

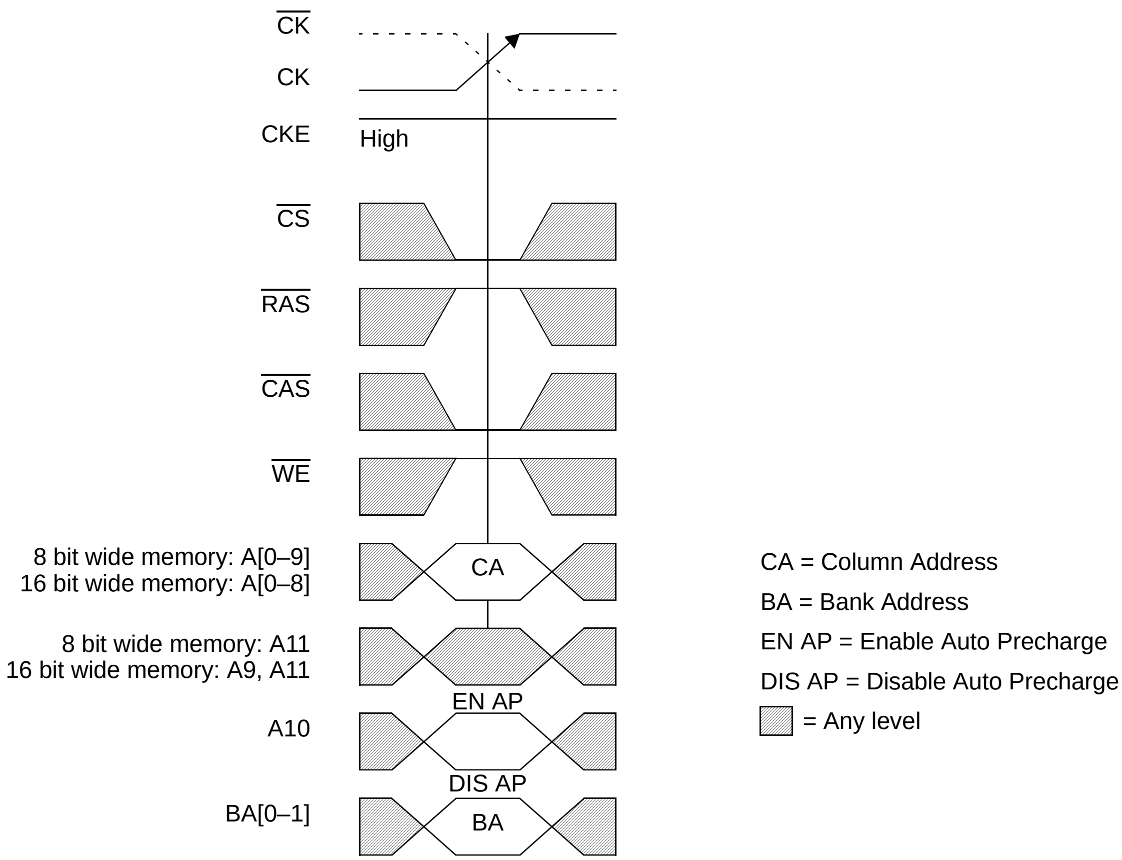


Figure 7. READ Command

3.2.4 WRITE

The WRITE command initiates a burst write access to an active row. BA[0–1] select the bank and A[0–*i*] (where *i* = 8 for 16 bit wide memory and 9 for 8 bit wide memory) select the starting column address. The value on input A10 determines whether AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the accessed row accessed is precharged at the end of the WRITE burst. If AUTO PRECHARGE is not selected, the row remains open for subsequent accesses. Input data on the DQ is written to the memory array according to the DM logic level coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory. If the DM signal is registered high, the corresponding data inputs are masked or ignored and a WRITE command is not executed to that byte/column location.

Table 6. DDR Commands, WRITE

Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR
WRITE	L	H	L	L	Bank/Col

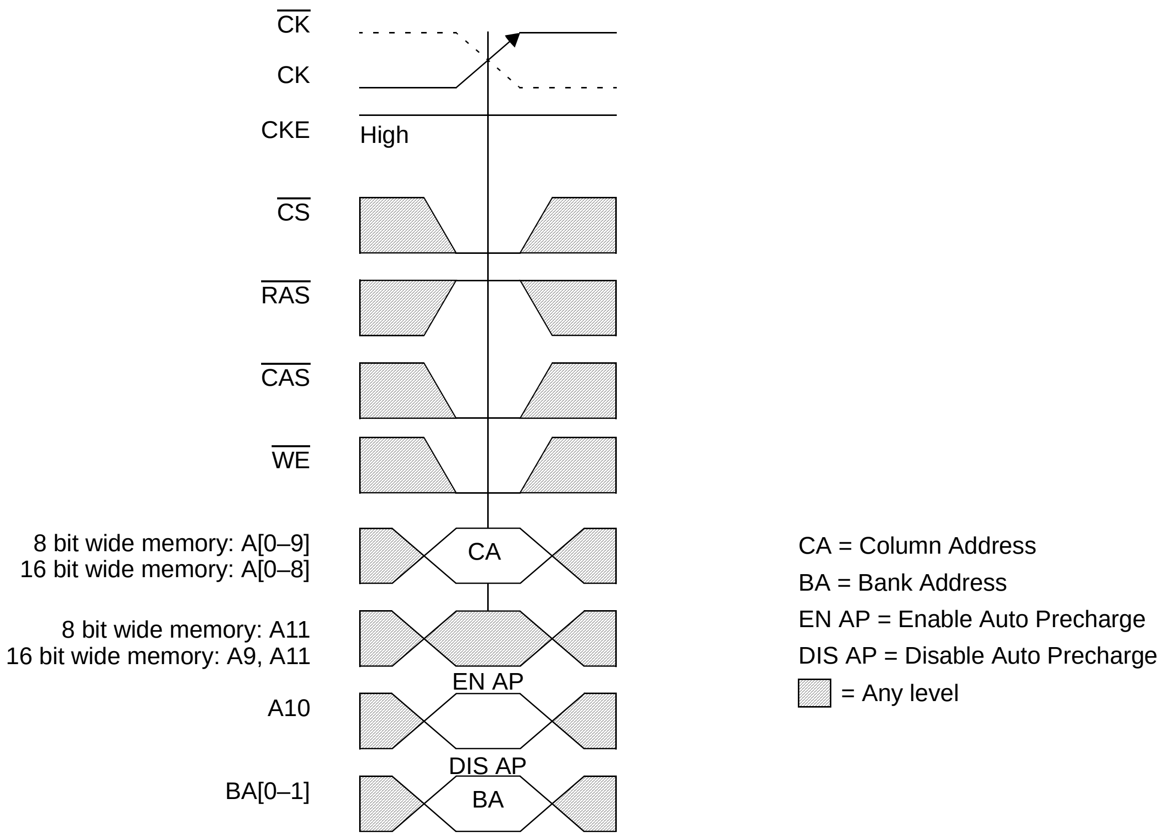


Figure 8. Write Command

3.2.5 PRECHARGE

The PRECHARGE command deactivates the open row in a selected bank or in all banks. The bank(s) are available for a subsequent row access at a specified time (t_{rp}) after the PRECHARGE command is issued. A10 determines whether one or all banks are to be precharged. When only one bank is to be precharged, BA[0–1] select the bank. Otherwise, BA[0–1] are treated as “Any Level.” After a bank is precharged, it is idle and must be activated before any READ or WRITE commands are issued to it.

Table 7. DDR Commands, PRECHARGE

Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR
PRECHARGE	L	L	H	L	Code

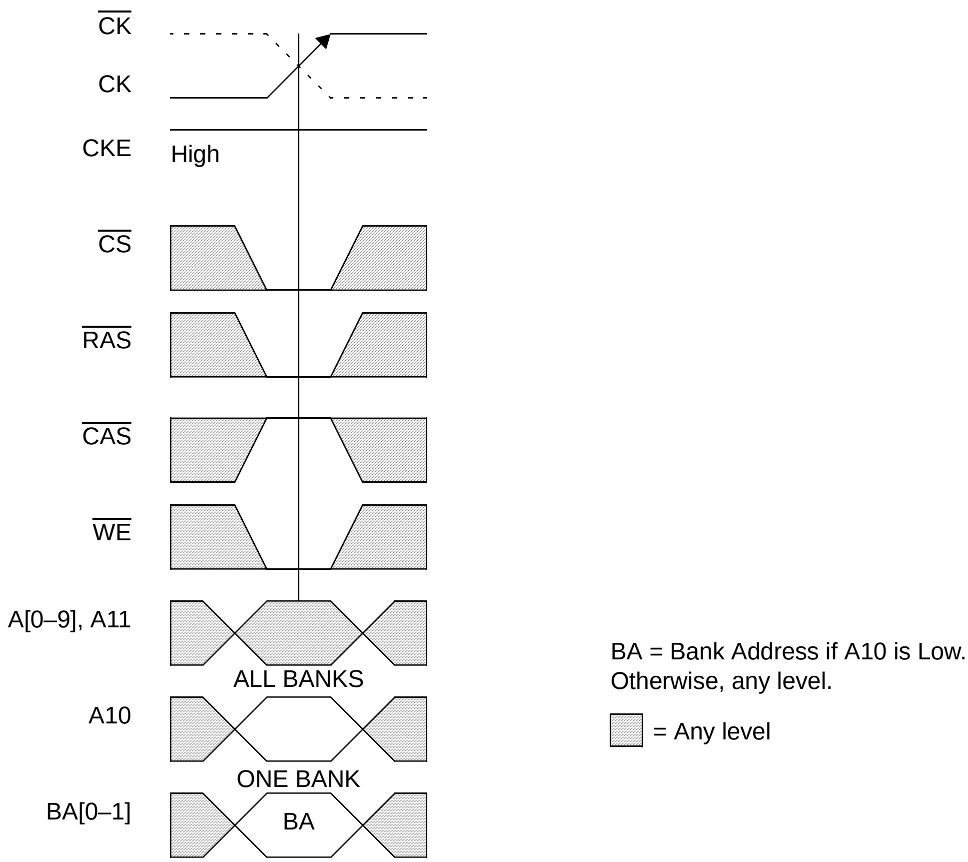


Figure 9. PRECHARGE Command

3.2.6 AUTO REFRESH or SELF REFRESH

The AUTO REFRESH command must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued. The SELF REFRESH command retains data in the DDR SDRAM even if the rest of the system is powered down. The DDR SDRAM retains data without external clocking. This command is initiated like an AUTO REFRESH command, except that CKE is disabled.

Table 8. DDR Commands, AUTO REFRESH or SELF REFRESH

Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR
AUTO REFRESH or SELF REFRESH	L	L	L	H	x

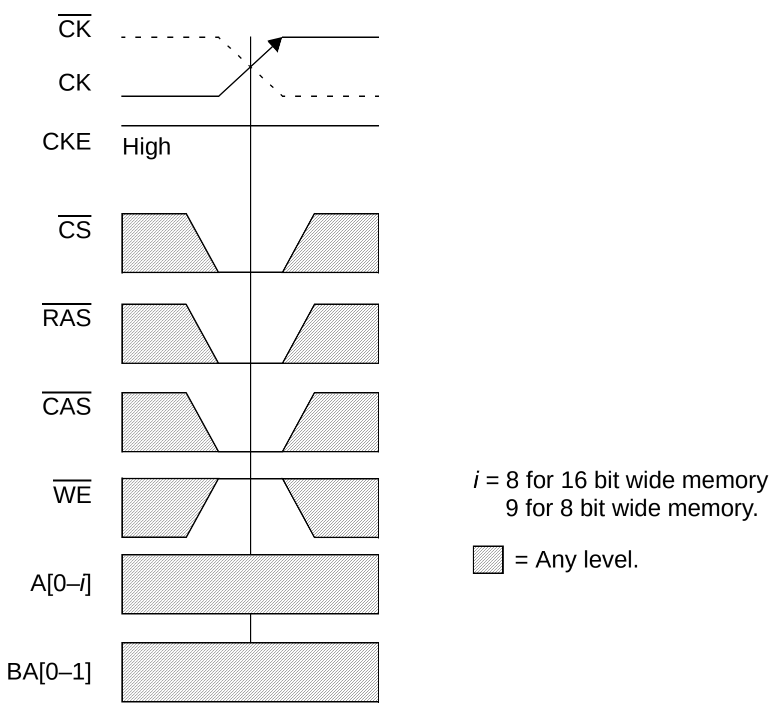


Figure 10. AUTO REFRESH Command

3.3 Example DDR Operations

This section presents DDR signal timing examples of DDR operations.

3.3.1 Read Burst

The READ command is sampled on the rising edge of CK at T = 0. The bank is already activated before the READ command is initiated. With a $\overline{\text{CAS}}$ latency of 2, the first rising edge of DQS occurs at T = 2 when the first read data is launched onto data pin DQ. The data strobe signal, DQS, toggles during a burst with the same frequency as the CK clock. **Figure 11** shows a burst length of 4 bytes so that three subsequent data elements follow with each rising and falling edge of CK.

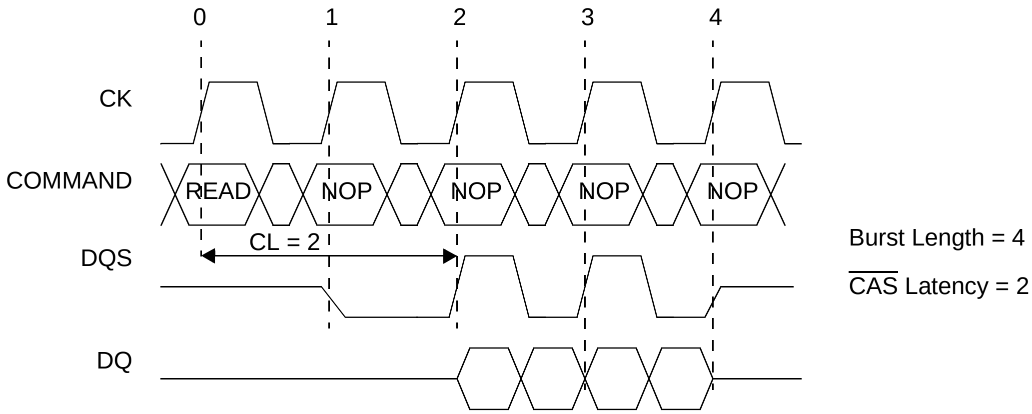


Figure 11. Read Burst

3.3.2 Write Burst

A WRITE command is sampled on the rising edge of CK at T = 0. The interval between the WRITE command and first DQS latching transition is known as t_{DQSS}. For the Micron MT46V8M16-75, this value ranges from 0.75 to 1.25 CK cycles. In **Figure 12**, t_{DQSS} is 1 CK cycle so that the first rising edge of DQS occurs at T = 1. DQS toggles during the burst at the same frequency as the CK clock. Here, the burst length is 4 bytes so that three subsequent data elements follow with each rising and falling edge of CK.

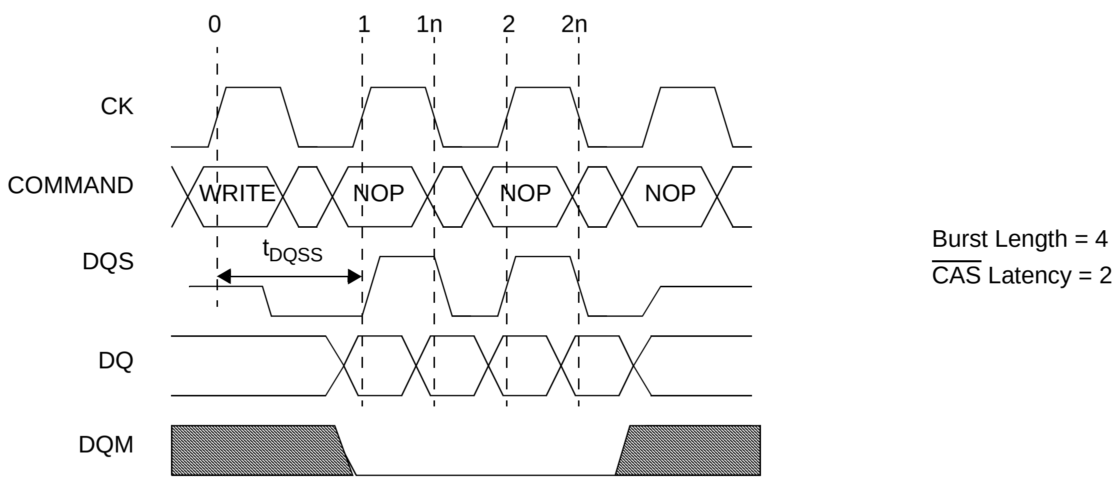


Figure 12. Write Burst

3.3.3 Consecutive Read Bursts

For a consecutive or back-to-back read burst operation, after the first read command at T = 0, a consecutive READ command can be initiated after BL/2 CK cycles at T = 2. **Figure 13** shows a burst length of 4, so the second READ command is initiated after 2 CK cycles. Issuing the second read command earlier than 2 CK cycles after the first read command interrupts the previous data from the first READ command.

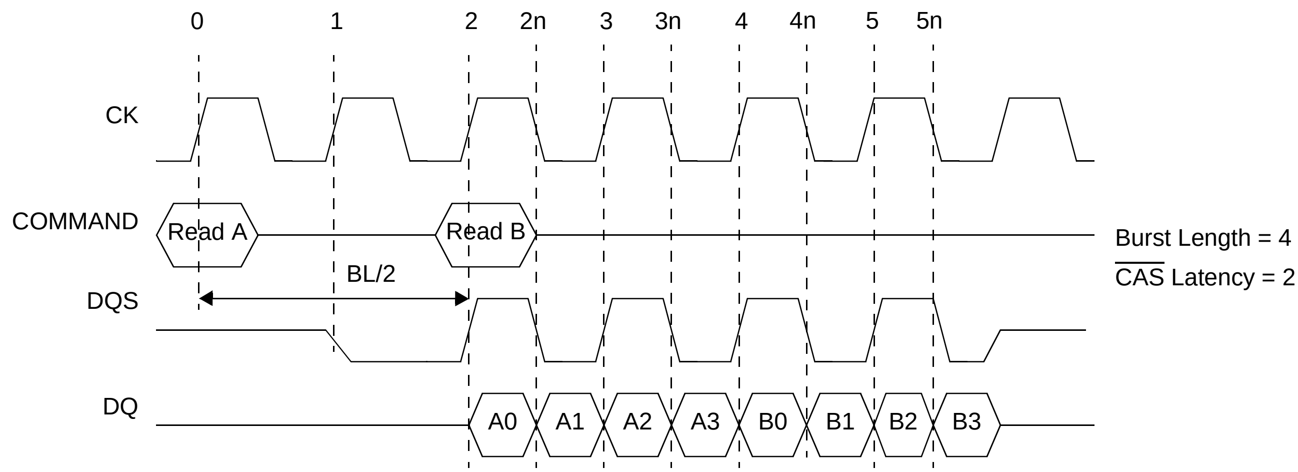


Figure 13. Consecutive Read Bursts

3.3.4 Consecutive Write Burst

During a consecutive or back-to-back write burst operation, after the first WRITE command at T = 0, a consecutive WRITE command can be initiated after BL/2 CK cycles at T = 2. The example in **Figure 14** has a burst length of 4, so the second WRITE command is initiated after 2 CK cycles. Issuing the write command earlier than 2 CK cycles after the first READ command interrupts the previous data from the first WRITE command.

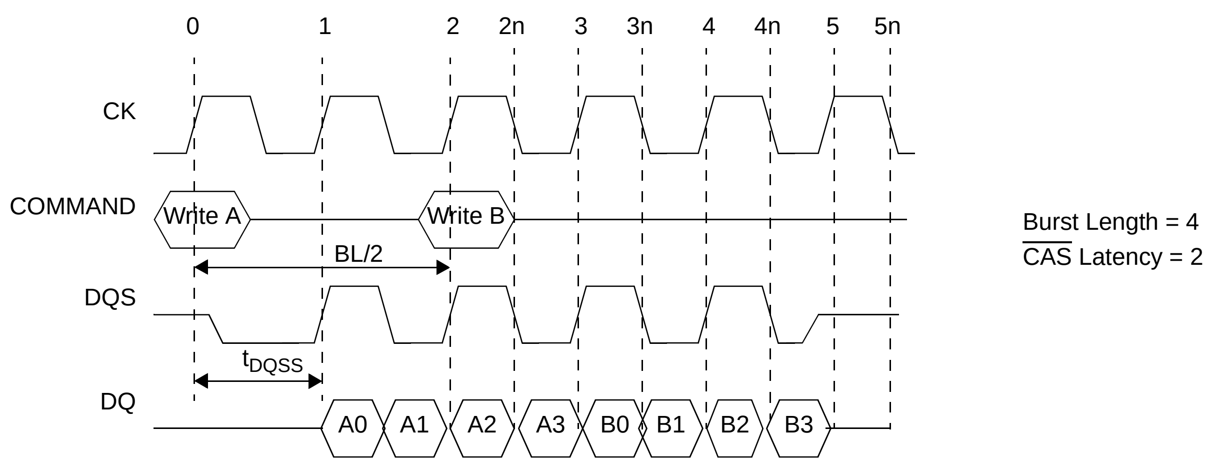


Figure 14. Consecutive Write Burst

3.3.5 Burst Read Followed by Burst Write

For a burst read followed by a burst write operation, after the first read command at T = 0, a consecutive write command can be initiated after CL + BL/2 CK cycles at T = 4. The example in **Figure 15** assumes a $\overline{\text{CAS}}$ latency of 2 and a burst length of 4, so the consecutive WRITE command is initiated after 4 CK cycles. Issuing the consecutive WRITE command earlier than 4 CK cycles after the READ command interrupts the previous data from the READ command.

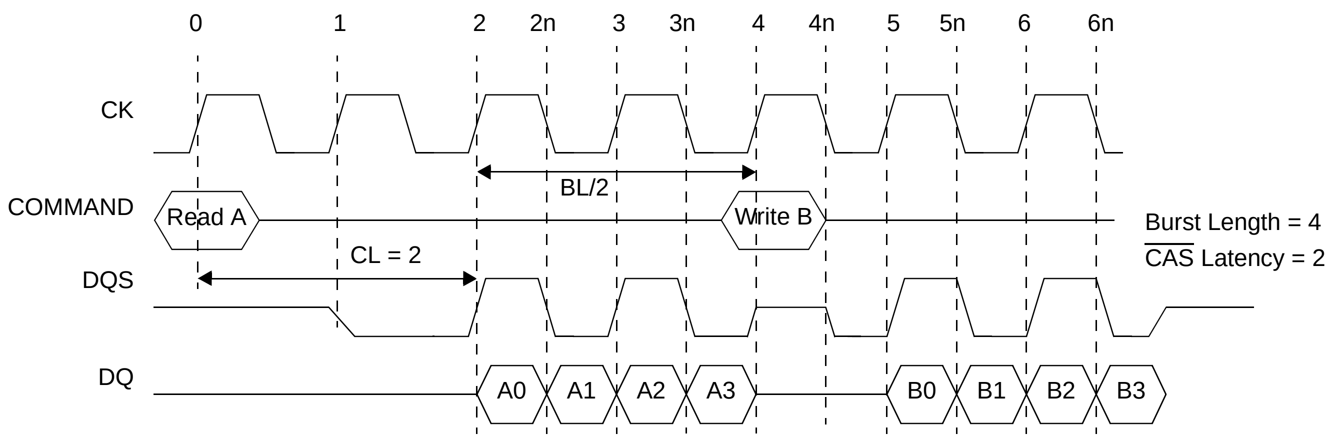


Figure 15. Burst Read Followed By Burst Write

3.3.6 Burst Write Followed by Burst Read

For a burst write followed by a burst read operation, after the first WRITE command at T = 0, a consecutive READ command can be initiated after BL/2 + t_{DQSS} + t_{WTR} CK cycles at T = 4. The internal WRITE to READ command delay, t_{WTR}, is 1 CK cycle for the Micron MT46V8M16-75 device. The example in **Figure 16** shows a $\overline{\text{CAS}}$ latency of 2 and a burst length of 4, so the consecutive READ command is initiated after 4 CK cycles. Issuing the consecutive READ command earlier than 4 CK cycles after the WRITE command interrupts the previous data from the WRITE command.

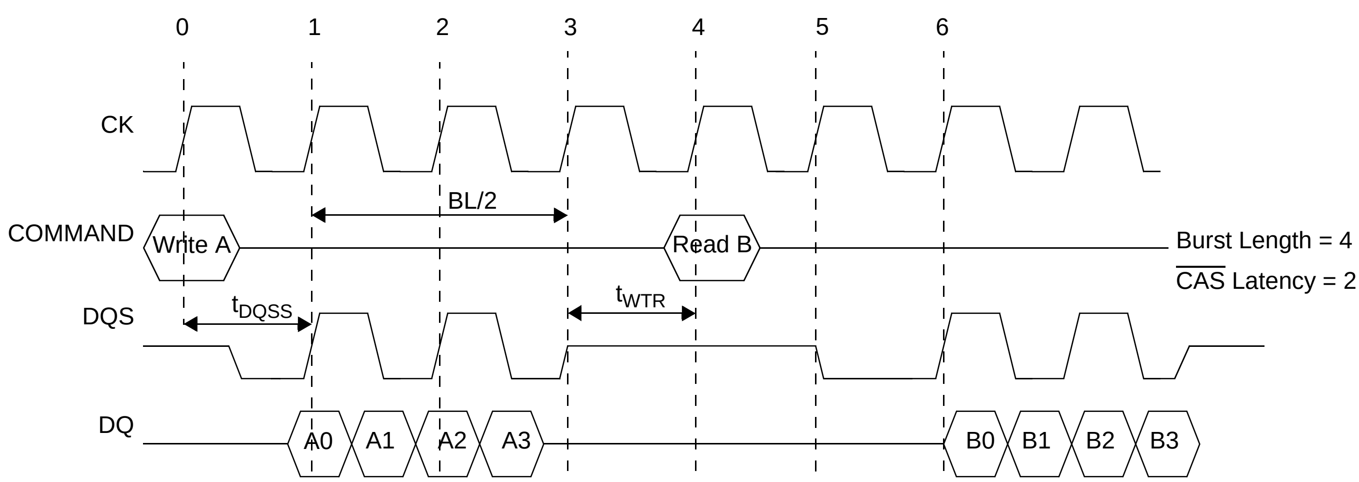
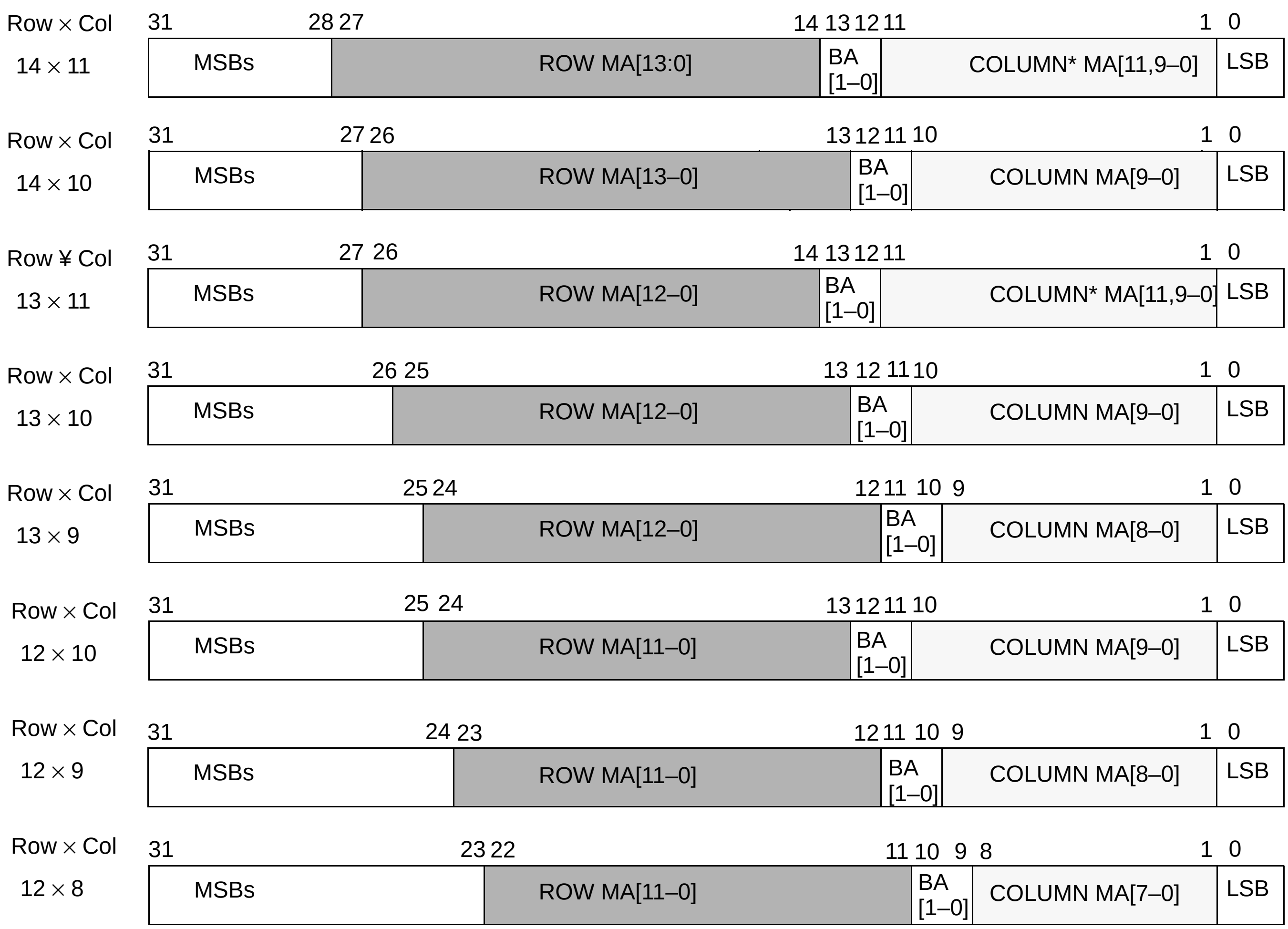


Figure 16. Burst Write Followed by Burst Read

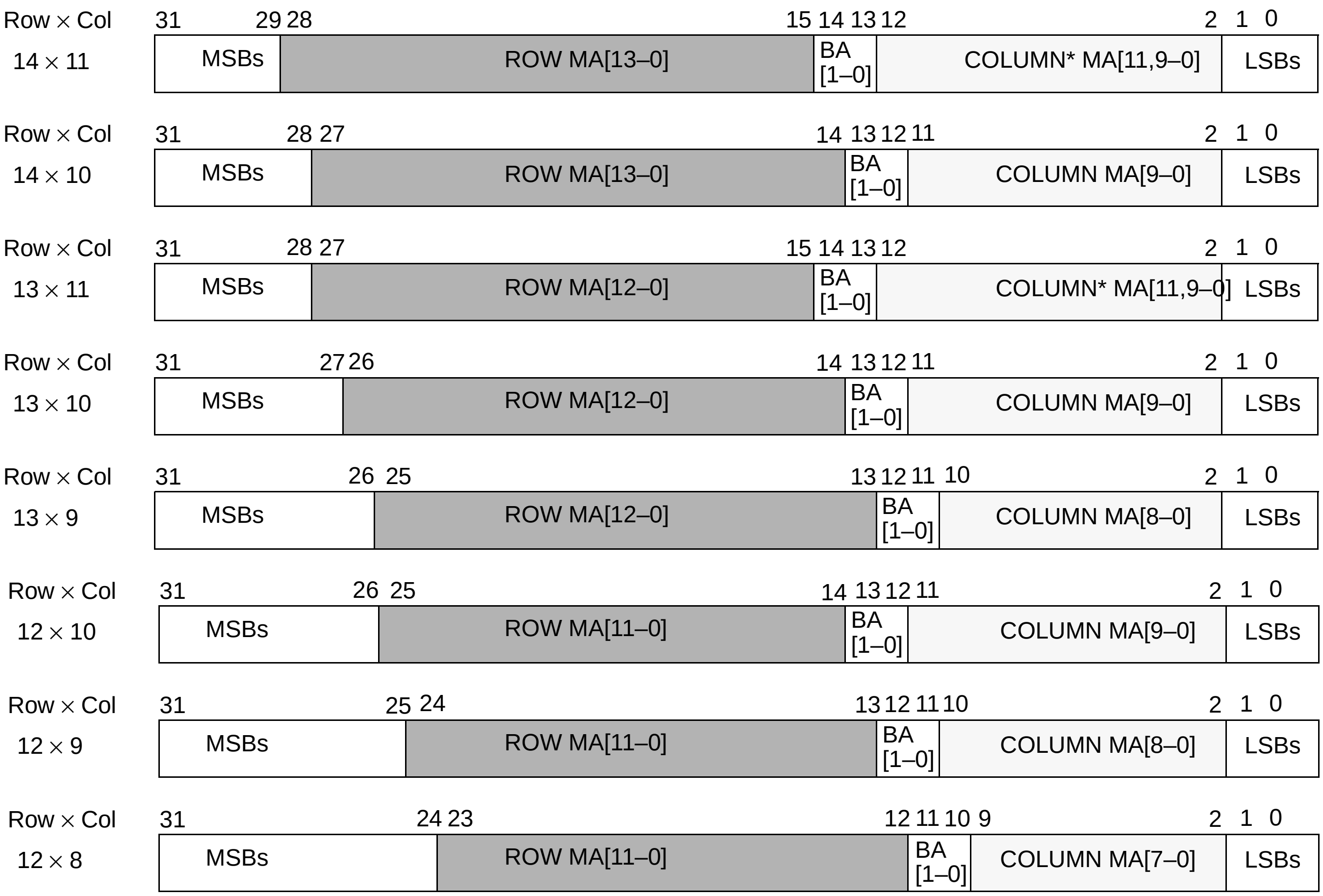
3.4 Address Multiplexing

Figure 17 and **Figure 18** show the address multiplexing for each supported DDR SDRAM configuration in 16-pin and 32-pin modes. In *n* × 11 configurations, the lowest 11 address pins for the column address are MA11, MA[9–0] where MA10 is skipped. MA10 is used as AUTO PRECHARGE command signal during the READ/WRITE command cycle, and it is not available for column address The next signal address, MA11, is used instead. For example, in a 14 row × 11 column DDR configuration in 32-pin mode, the logic address bits 29–15 are driven to the DDR address pins MA[13–0] during the row address strobe. The logic address bits 14–13 are driven to the DDR address pins BA[1–0] to select the bank. The logic address bits 12–2 are driven to the DDR address pins MA11, MA[9–0] during the column address strobe. MA10 is skipped because it is reserved for the AUTO PRECHARGE command.



Note:
MA10 is used as the auto precharge bit for reads and writes, so the column address can never use MA10.
The column addresses are numbered as MA11, MA[9–0], where MA10 is skipped.

Figure 17. Address Multiplexing in 16-Pin Mode



Note:
MA10 is used as the auto precharge bit for reads and writes, so the column address can never use MA10.
The column addresses are numbered as MA11, MA[9–0], where MA10 is skipped.

Figure 18. Address Multiplexing in 32-Pin Mode

4 Configuring the DDR Controller

To configure the MSC711x DDR controller, the software must perform the following steps:

1. Define the address range for each bank via the Chip-Select Memory Bound Registers (CSBR*x*).
2. Define the organization of the memory device via the Chip-Select Configuration Registers (CS*x*CFG).
3. Define the timing of the memory device via the DDR SDRAM Timing Configuration Registers (TCFG1 and TCFG2).
4. Define the mode registers of the memory device via the DDR SDRAM Mode Configuration Register (SMCFG).
5. Set up a precharge interval and a refresh interval via the DDR SDRAM Interval Configuration Register (SICFG).
6. Enable the DDR controller.

   After all parameters are configured, system software must set the memory controller SCFG[MEMEN] bit to enable the memory interface. Setting this bit asserts the CKE signal. The DDR memory controller then automatically performs the initialization sequence to prepare the JEDEC-compliant DDR SDRAM array for accesses.

4.1 DDR SDRAM Initialization

The JEDEC DDR SDRAM specification requires that the DDR SDRAM must be initialized in a predefined manner.

1. Wait 200 µs after all power supply, reference voltages, and clock are stable before applying an executable command.
2. Apply the DESELECT or NOP command.
3. Apply the PRECHARGE ALL command.
4. Issue the MODE REGISTER SET command for the Extended Mode Register to enable the DLL.
5. Wait for two DDR SDRAM cycles.
6. Issue the MODE REGISTER SET command for the Mode Register to reset the DLL and to program the operating parameters.
7. Wait for two DDR SDRAM cycles.
8. Apply the PRECHARGE ALL command.
9. Wait for the PRECHARGE command period.
10. Apply the AUTO REFRESH command.
11. Wait for the AUTO REFRESH command period.
12. Apply the AUTO REFRESH command.
13. Wait for the AUTO REFRESH command period.
14. Issue the MODE REGISTER SET command for the Mode Register with the reset DLL bit deactivated to program the operating parameters without resetting the DLL.
15. Wait for two DDR SDRAM cycles.

These steps are not required to program the DDR memory controller, which automatically performs steps 2 to 15 after it is enabled.

4.2 Chip-Select Memory Bounds Registers

The two Chip-Select Memory Bounds Registers (CSBR0 and CSBR1) define the starting and ending addresses of the memory space that corresponds to chip selects $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$. **Figure 19** and **Figure 20** show the CSBRx registers for both 16-pin and 32-pin modes. The starting address is defined in the SA*n* field. In 16-pin mode, this value is compared to the most significant 10 bits of the 32-bit address. In the 32-pin mode, this value is compared to the most significant 9 bits of the 32-bit address. Similarly, the ending address is defined in the EA*x* field. In 16-pin mode, this value is compared to the most significant 10 bits of the 32-bit address. In 32-pin mode, this value is compared to the most significant 9 bits of the 32-bit address.

31					26	25 16	15					10	9 0
0	0	0	0	0	0	SA*x*	0	0	0	0	0	0	EA*x*

Figure 19. CSBRx, 16-Pin Mode

31						25	24 16	15						9	8 0
0	0	0	0	0	0	0	SAx	0	0	0	0	0	0	0	EAx

Figure 20. CSBRx, 32-Pin Mode

To program the DDR controller for the MSC711xADS, which maps the MSC7115 external memory space 0x20000000–0x21FFFFFF and uses chip-select $\overline{\text{CS0}}$ to select the DDR SDRAM, DDR memory controller initialization requires the following values to be written to the CSBR0 register:

- CSBR0[SA*x*] = 001000000 to set 0x20000000 as the starting address.
- CSBR0[EA*x]* = 001000011 to set 0x21FFFFFF as the ending address.
- CSBR0 = 0x00400043.

4.3 Chip-Select Configuration Registers

The two Chip-Select Configuration Registers (CS0CFG and CS1CFG) enable the DDR chip selects and set the row and column configuration. **Figure 21** shows the CS*x*CFG register.

31	30						24	23	22											11	10–8	7				3	2–0
CSxEN	0	0	0	0	0	0	0	APxEN	0	0	0	0	0	0	0	0	0	0	0	0	RBCSx	0	0	0	0	0	CBCSx

Figure 21. CS*x*CFG Register

- *CSxEN*. Enables the corresponding chip select. Setting this bit activates the chip select and assumes the state set in CSBRx.
- *APxEN*. Enables auto precharge. Setting this bit issues an AUTO PRECHARGE command for read and write transactions.
- *RBCSx*. Configures the number of row bits on the corresponding chip select. The MSC711x supports 12, 13, and 14 row bits.
- *CBCSx*. Configures the number of column bits on the corresponding chip select. The MSC711x supports 8, 9, 10, and 11 column bits.

In this example, the Micron MT46V8M16-75, which is used on the MSC711xADS, is am 8 MB × 16-bit DDR SDRAM device with 12 rows and 8 columns. The CS0CFG register is written with the following values:

- CS0CFG[CS0EN] = 1 to enable the $\overline{\text{CS0}}$
- CS0CFG[AP0EN] = 0 to enable precharge only if the global auto precharge is enabled
- CS0CFG[RBCS0] = 000 to configure 12 row bits
- CS0CFG[CBCS0] = 001 to configure 9 column bits
- CS0CFG = 0x80000001

4.4 Timing Configuration 1

The DDR SDRAM Timing Configuration Register 1 (TCFG1) sets the timing of various control commands (see **Figure 22**). The DDR SDRAM timing requirements are detailed in the device data sheet.

31	30–28	27–24	23	22–20	19	18–16	15–12	11	10–8	7	6–4	3	2–0
0	PREACT	ACTPRE	0	ACTRW	0	CASLAT	REFREC	0	WRREC	0	ACTACT	0	WRRD

Figure 22. TCFG1

- *PREACT*. The number of clock cycles between a PRECHARGE command and an ACTIVATE or REFRESH command. This interval is indicated as t_{rp}. Up to 7 t_{rp} clocks are supported.

- *ACTPRE*. The number of clock cycles between an ACTIVATE command and a PRECHARGE command. The activate to precharge command is indicated as t_{ras}. Up to 15 t_{ras} clocks are supported.
- *ACTRW*. The number of clock cycles between an ACTIVATE command and a READ or WRITE command. This interval is indicated as t_{rcd}. Up to 7 t_{rcd} clocks are supported.
- *CASLAT*. The read latency between the READ command and the first output data. Up to 4 clocks in 0.5 clock increments are supported. The $\overline{\text{CAS}}$ latency must also be programmed in the DDR SDRAM Mode Configuration Register (SMCFG).
- *REFREC*. The number of clock cycles between a REFRESH command and an ACTIVATE command. The refresh recovery time is indicated by t_{rfc}, which is equal to eight plus the REFREC value. Valid REFREC values are 9 to 23 clocks.
- *WRREC*. The number of clock cycles between the last data associated with a WRITE command and a PRECHARGE command. This interval is indicated as t_{wr}. Up to 7 t_{wr} clocks are supported.
- *ACTACT*. The number of clock cycles between an ACTIVATE command and another ACTIVATE command for a different logical bank within the same physical bank. This interval is indicated as t_{rrd}. Up to 4 t_{rrd} clocks are supported.
- *WRRD*. The number of clock cycles between the last write data pair and the subsequent READ command to the same physical bank. This interval is indicated as t_{wtr}. Up to 7 t_{wtr} clocks are supported.

The Micron MT46V8M16-75 has the timing requirements shown in **Table 9**. If the DDR clock operates at 100 MHz, the clock cycle time is t_{ck} = 10 ns. The TCFG1 register is configured as follows:

- TCFG1[PREACT] = 010 for 2 clocks cycles
- TCFG1[ACTPRE] = 0100 for 4 clock cycles
- TCFG1[ACTRW] = 010 for 2 clock cycles
- TCFG1[CASLAT] = 011 for 2 clock cycles
- TCFG1[REFREC] = 0001 for the minimum 9 clock cycles
- TCFG1[WRREC] = 010 for 2 clock cycles
- TCFG1[ACTACT] = 0010 for 2 clock cycles
- TCFG1[WRRD] = 001 for 1 clock cycle
- TCFG1 = 0x24231221

Table 9. Micron MT46V8M16-75 Timing

Parameter	Symbol	Parameter	Min	Num of t_{ck}
PRECHARGE to ACTIVATE	t_{rp}	PREACT	20 ns	2
ACTIVATE to PRECHARGE	t_{ras}	ACTPRE	40 ns	4
ACTIVATE to READ/WRITE	t_{rcd}	ACTRW	20 ns	2
$\overline{\text{CAS}}$ Latency	CL	CASLAT	2	2
Refresh Recovery	t_{rfc}	REFREC	75 ns	8
Last data WRITE to PRECHARGE	t_{wr}	WRREC	15 ns	2
ACTIVATE to ACTIVATE	t_{rrd}	ACTACT	15 ns	2
Last data WRITE to READ	t_{wtr}	WRRD	1 t_{ck}	1

4.5 Timing Configuration 2

The DDR SDRAM Timing Configuration Register 2 (TCFG2) allows timings to be adjusted for more efficient operation (see **Figure 23**).

31			28	27 24	23			20	19	18					13	12 10	9									0
0	0	0	0	CPO	0	0	0	0	ACSM	0	0	0	0	0	0	WRDD	0	0	0	0	0	0	0	0	0	0

Figure 23. TCFG2

- *CPO*. $\overline{\text{CAS}}$ to preamble timing. This field controls the number of clock cycles between when a READ is issued and when the corresponding DQS is valid for the memory controller. Up to CASLAT + 5 clock cycles in increments of 0.5 clock cycles are supported. This field affects only read accesses.
- *ACSM*. Address and control shift mode. When this bit is set, the address and control buses are shifted by 0.5 clock cycles before they are driven onto the pins. Otherwise, the address and control buses are output in the default mode.
- *WRDD*. The WRITE command to write data strobe timing. This field controls the amount of delay between the data and data strobes for write accesses. Up to 1 clock cycle in increments of 0.25 cycle delay is supported. When the default value of 0 clock delay is selected, the memory controller automatically adds an extra turnaround cycle between reads and writes.

In this example, the TCFG2 register is configured as follows:

- TCFG2[CPO] = 0000; default $\overline{\text{CAS}}$ to preamble of CASLAT + 1 cycles.
- TCFG2[ACSM] = 0; address and control buses are output in the default mode
- TCFG2[WRDD] = 001; 0.25 clock delay
- TCFG2 = 0x00000400

4.6 DDR SDRAM Control Configuration

The DDR SDRAM Control Configuration Register (SCFG) enables the interface and specifies certain operating features such as self refresh, error checking and correcting, and dynamic power management (see **Figure 24**).

31	30	29	28	27	26	25 24	23	22	21	20		18	17	16	15	14														0
MEMEN	SREN	0	RDEN	0	0	STYPE	0	0	DPWR	0	0	0	NCAP	0	2TEN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 24. SCFG

- *MEMEN*. Enables the DDR SDRAM interface logic. This bit must not be set until all other memory configuration parameters are appropriately configured.
- *SREN*. Enables self refresh during sleep or soft-stop. Clearing this bit disables the self refresh.
- *RDEN*. The type of DIMM used in the system. When set, this field indicates registered DIMMs. When cleared, this field indicates unbuffered DIMMs.
- *STYPE*. Selects the type of SDRAM device. The MSC711x supports only DDR SDRAM. This field must be set to 0b10.

- *DPWR*. Enables dynamic power management mode. To reduce power consumption, this bit can be set to deassert the CKE pin to power down dynamically when there is no memory activity. The CKE pin is reasserted when a new access or refresh is scheduled or when the dynamic power management mode is disabled. Clearing this bit disables the power management mode.
- *NCAP*. Whether the DDR SDRAM devices support concurrent auto precharge. When this bit is set, the DDR SDRAM devices do not support concurrent auto precharge. When this bit is cleared, the DDR SDRAM devices support concurrent auto-precharge.
- *2TEN*. The timing for the address and control signals. When this bit is set, the address and control signals assert for 2 cycles. The chip select still asserts for only 1 cycle. When this bit is cleared, the address and control signals assert for 1 cycle.

In this example, the SCFG is configured as follows:

- SCFG[MEMEN] = 1 to enable the DDR SDRAM interface logic
- SCFG[SREN] = 1 to enable the self refresh during sleep or soft-stop
- SCFG[RDEN] = 0 to specify unbuffered DIMMs
- SCFG[STYPE] = 10 to specify DDR SDRAM
- SCFG[DPWR] = 0 to disable dynamic power management
- SCFG[NCAP] = 0 to specify support for concurrent auto precharge
- SCFG[2TEN] = 0 to specify that the address and control signals assert for 1 cycle
- SCFG = 0xC2000000

4.7 DDR SDRAM Mode Configuration

The DDR SDRAM Mode Configuration Register (SMCFG) sets the values loaded into the DDR mode register (see **Figure 25**). The ESDMOD field specifies the initial value loaded into the DDR SDRAM Extended Mode Register. The ESDMOD value is dependent on the DDR SDRAM device. In this example, the Micron MT46V8M16 defines the Extended Mode Register as shown in **Table 10**.

31 — 16	15 — 0
ESDMOD	SMMOD

Figure 25. SMCFG

Bits 13 and 12 must have values of 0 and 1, respectively, to select the Extended Mode Register instead of the Mode Register. Bits 11 through 2 must be cleared to all zeros for valid operating mode. Bit 1 defines the drive strength, and bit 0 specifies DLL enable/disable. In this example, the ESDMOD field has a value of 0x1000.

Table 10. Extended Mode Register Definition

Bit	Parameter	Value
13	—	Must be cleared to 0
12	—	Must be set to 1
11–2	Operating Mode	Must be cleared to 0b0000000000
1	Drive Strength	0 Normal 1 Reduced

Table 10. Extended Mode Register Definition

Bit	Parameter	Value
0	DLL Enable	0 DLL is enabled 1 DLL is disabled

The SMMOD field specifies the initial value loaded into the DDR SDRAM Mode Register. This value is also dependent on the DDR SDRAM device. In this example, the Micron MT46V8M16 defines the Mode Register as shown in **Table 11**. Bits 13 and 12 must be cleared to 0 to select the Mode Register instead of the Extended Mode Register. Bits 11–7 are cleared to all zeros for normal operation. Bit 6–4 have a value of 010 to specify a $\overline{\text{CAS}}$ latency of 2. Bit 3 is cleared to select sequential burst type. Bits 2–0 have a value of 010 to specify four beats in a burst. In this example, SMMOD has a value of 0x0022.

Table 11. Mode Register Definition

Bit	Parameter	Value
13	—	Must be cleared to 0
12	—	Must be cleared to 0
11–7	Operating Mode	00000 Normal Operation 00010 Normal Operation/Reset DLL
6:4	$\overline{\text{CAS}}$ Latency	010 2 110 2.5 All other values are reserved.
3	Burst Type	0 Sequential 1 Interleaved
2–0	Burst Length	001 2 010 4 011 8 All other values are reserved

This example sets the SMCFG to the following values:

- SMCFG[ESDMOD] = 0x1000
- SMCFG[SMMOD] = 0x0022
- SMCFG = 0x10000022

4.8 DDR SDRAM Interval Configuration

The DDR SDRAM Interval Configuration Register (SICFG) controls the number of clock cycles between bank refreshes and the number of cycles to maintain a page after it is accessed (see **Figure 26**).

31	30	29 … 16	15 … 0
0	0	REFINT	PI

Figure 26. SICFG

- *REFINT*. The refresh interval. This value represents the number of cycles between refresh cycles. The Micron MT46V8M16 has an average periodic refresh interval of 15.6 µs. With a DDR clock cycle of 10 ns, the refresh interval takes 1560 cycles or 0x618 cycles.

- *PI*. The precharge interval. This value represents the number of cycles that a page is retained as an open page after a DDR SDRAM access. When this field is cleared, the DDR memory controller operates in global auto precharge mode by using auto precharge read write commands rather than open page mode. In this example, the PI is cleared.

This example configures the SICFG as follows:

- SICFG[REFINT] = 0x0618 to specify a refresh interval of 1560 cycles
- SICFG[PI] = 0x0000 to operate in open page mode
- SICFG = 0x06180000

5 Revision History

Table 12 provides a revision history for this application note.

Table 12. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	11/2004	Initial release.
1	03/2007	Corrected the bit numbers in Figure 23 on page 21. Figure 23 displays the register TCFG2.

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