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MSC711x Design Checklist

MSC7110, MSC7112, MSC7113, MSC7115, MSC7116, MSC7118, and MSC7119

This application note provides a set of recommendations to assist you in designing systems using an MSC711x device. The MSC711x family is a high-performance, cost effective family of DSPs based on the StarCore® SC1400 core, which offers one core architecture to support lower cost, low-channel density applications. This document can be useful as a general guideline for designing new systems because it highlights the aspects of a design that merit special attention. Before you get started, you should become familiar with the available documentation, silicon revisions, software, models, and tools. Refer to **Section 8**, *Related Reading*, on page 15.

CONTENTS

1 Pin Assignments

During the first phase of designing a system with a MSC711x device, your main task is to make the pin assignments. Some MSC711x pins are multiplexed, depending on the device programming. Take care in programming MSC711x registers to configure these multiplexed pins as needed for your system design. Pin multiplexing is configured in the Port Control Registers (GPxCTL). The default configuration after reset for all signals is software-controlled general-purpose input (GPI). Some of these GPIs can be reconfigured as external interrupt inputs. Leaving the port configuration for a signal line as software-controlled and changing the data direction to output changes the signal to a general-purpose output (GPO). Changing the port configuration for a signal to hardware-controlled dedicates the signal functionality to the TDM, HDI16, I^2C, UART, or event port. Under hardware control, some pins have an alternate function that is determined by the settings in the Device Configuration Register (DEVCFG). Also, the following signals have one function during deassertion of $\overline{\text{PORESET}}$ but switch to another multiplexed function during regular operation: H8BIT, BM[3–0], SWTE, and HDSP.

2 Power

This section outlines the MSC711x power considerations: power supply, power sequencing, power planes, decoupling, power supply filtering, and power consumption. It also presents a recommended power supply design and options for low-power consumption. For information on AC/DC electrical specifications and thermal characteristics, refer to the data sheet for your device.

2.1 Power Supply

The MSC711x requires four input voltages, as shown in **Table 1**.

Table 1. MSC711x Voltages

Supply	Symbol	Nominal Voltage	Current Rating
Core	V_{DDC}	1.2 V	1.5 A per device
Memory	V_{DDM}	2.5 V	0.5 A per device
Reference	V_{REF}	1.25 V	10 µa per device
I/O	V_{DDIO}	3.3 V	1.0 A per device

You should supply the MSC711x core voltage via a variable switching supply or regulator to allow for compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied with 1.2 V (+5% and –10%) across V_{DDC} and GND. The I/O section is supplied with 3.3 V (± 10%) across V_{DDIO} and GND. The memory and reference voltages supply the double data rate (DDR) memory controller. The memory voltage is supplied with 2.5 V across V_{DDM} and GND. The reference voltage is supplied across V_{REF} and GND and must be between $0.49 \times V_{DDM}$ and $0.51 \times V_{DDM}$. Refer to the JEDEC standard JESD8 (*Stub Series Terminated Logic for 2.5 Volts* (STTL_2)) for memory voltage supply requirements.

The following equations permit estimated power usage to be calculated for individual design conditions. Overall power is derived by totaling the power used by each of the major subsystems:

$$P_{TOTAL} = P_{CORE} + P_{PERIPHERALS} + P_{DDRIO} + P_{IO} + P_{LEAKAGE} \quad \textbf{Equation 1}$$

This equation combines dynamic and static power. Dynamic power is determined using the generic equation:

$$C \times V^2 \times F \times 10^{-3}\ mW \quad \textbf{Equation 2}$$

where,

C = load capacitance in pF
V = peak-to-peak voltage swing in V
F = frequency in MHz

Estimation of core power is straightforward. It uses the generic dynamic power equation and assumes that the core load capacitance is 750 pF, core voltage swing is 1.2 V, and the core frequency is 200 MHz. This yields:

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 200\ MHz \times 10^{-3} = 194.4\ mW \quad \textbf{Equation 3}$$

This equation allows for adjustments to voltage and frequency if necessary.

Peripherals include the DDR memory controller, DMA controller, HDI16, TDM, UART, timers, GPIOs, and the I^2C module. Basic power consumption by each module is assumed to be the same and is computed by using the following equation which assumes an effective load of 20 pF, core voltage swing of 1.2 V, and a switching frequency of 100 MHz. This yields:

$$P_{PERIPHERAL} = 20\ pF \times (1.2\ V)^2 \times 100\ MHz \times 10^{-3} = 2.88\ mW\ per\ peripheral \quad \textbf{Equation 4}$$

Multiply this value by the number of peripherals used in the application to compute the total peripheral power consumption. Estimation of power consumption by the DDR memory system is complex. It varies based on overall system signal line usage, termination and load levels, and switching rates. Because the DDR memory includes terminations external to the MSC711x device, the 2.5 V power source provides the power for the termination, which is a static value of 16 mA per signal driven high. However, the dynamic power is computed using a differential voltage swing of ±0.200 V, yielding a peak-to-peak swing of 0.4 V. The equations for computing the DDR power are:

$$PDDRIO = PSTATIC + PDYNAMIC \quad \textbf{Equation 5}$$

$$PSTATIC = (unused\ pins \times \%\ driven\ high) \times 16\ mA \times 2.5\ V \quad \textbf{Equation 6}$$

$$P_{DYNAMIC} = (pin\ activity\ value) \times 20\ pF \times (0.4\ V)^2 \times 200\ MHz \times 10^{-3}\ mW \quad \textbf{Equation 7}$$

$$pin\ activity\ value = (active\ data\ lines \times \%\ activity \times \%\ data\ switching) + (active\ address\ lines \times \%\ activity) \quad \textbf{Equation 8}$$

For example, assume the following:

unused pins = 16 (DDR uses 16-pin mode)
% driven high = 50%
active data lines = 16
% activity = 60%
% data switching = 50%
active address lines = 3

In this example, the DDR memory power consumption is:

$$P_{DDRIO} = ((16 \times 0.5) \times 16 \times 2.5) + (((16 \times 0.6 \times 0.5) + (3 \times 0.6)) \times 20 \times (0.4)^2 \times 200 \times 10^{-3}) = 324.2\ mW \quad \textbf{Equation 9}$$

The estimation of the I/O power is similar to the computation of the peripheral power estimates. The power consumption per signal line is computed assuming a maximum load of 20 pF, a voltage swing of 3.3 V, and a switching frequency of 25 MHz, which yields:

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 25\ MHz \times 10^{-3} = 5.44\ mW\ per\ I/O\ line \quad \textbf{Equation 10}$$

Multiply this number by the number of I/O signal lines used in the application design to compute the total I/O power.

Note: The signal loading depends on the board routing. For systems using a single DDR device, the load could be as low as 7 pF.

The leakage power is for all power supplies combined at a specific temperature. The value is temperature dependent. The observed leakage value at room temperature is 64 mW.

Using the examples in this section and assuming four peripherals and 10 I/O lines active, a total power consumption value is estimated as the following:

$$P_{TOTAL} = 194.4 + (4 \times 2.88) + 324{,}2 + (10 \times 5.44) + 64 = 648.52\ mW \quad \textbf{Equation 11}$$

2.2 Power Sequencing

For details on power sequencing, see the *Technical Data* sheet for your MSC711x device.

2.3 Power Planes

Each power supply pin (V_{DDC}, $V_{DDM,}$ and V_{DDIO}) should have a low-impedance path to the board power supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The MSC711x V_{DDC} power supply pins should be bypassed to ground using decoupling capacitors. The capacitor leads and associated printed circuit traces connecting to device power pins and GND should be kept to less than half an inch per capacitor lead. A minimum four-layer board that employs two inner layers as power and GND planes is recommended. See **Section 4** for DDR Controller power guidelines. For details on MSC711x layout, consult the “Power Supply Design Considerations” section of the *Technical Data* sheet for your MSC711x device.

2.4 Decoupling

Both the I/O voltage and core voltage should be decoupled for switching noise. For I/O decoupling, use standard capacitor values of 0.01 µF for every two to three voltage pins. For core voltage decoupling, use two levels of decoupling. The first level should consist of a 0.01 µF high frequency capacitor with low effective series resistance (ESR) and effective series inductance (ESL) for every two to three voltage pins. The second decoupling level should consist of two bulk/tantalum decoupling capacitors, one 10 µF and one 47 µF, (with low ESR and ESL) mounted as closely as possible to the MSC711x voltage pins. Additionally, the maximum drop between the power supply and the DSP device should be 15 mV at 1 A.

2.5 PLL Power Supply Filtering

The MSC711x V_{DDPLL} power signal provides power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to this pin should be filtered with capacitors that have low and high frequency filtering characteristics. V_{DDPLL} can be connected to V_{DDC} through a 2 Ω resistor. V_{SSPLL} can be tied directly to the GND plane. A circuit similar to the one shown in **Figure 1** is recommended. The PLL loop filter should be placed as

closely as possible to the V_{DDPLL} pin (which are located on the outside edge of the silicon package) to minimize noise coupled from nearby circuits. The 0.01 µF capacitor should be closest to V_{DDPLL}, followed by the 0.1 µF capacitor, the 10 µF capacitor, and finally the 2-Ω resistor to V_{DDC}. These traces should be kept short.

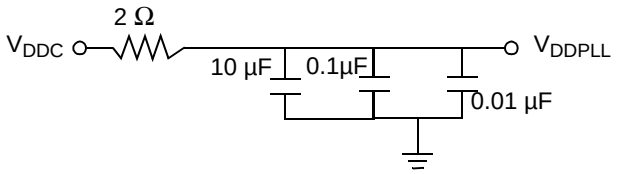

Figure 1. PLL Power Supply Filter Circuits

2.6 Power Consumption

The *MSC711x Technical Data* sheet provides preliminary power dissipation estimates for various configurations. You can reduce power consumption in your design by controlling the power consumption of the following regions of the device:

- *Extended core.* Use the SC1400 Stop and Wait modes by issuing a **stop** or **wait** instruction.
- *Clock synthesis module.* Disable the PLL, timer, watchdog, or DDR clocks or disable the CLKO pin.
- *AHB subsystem.* Freeze or shut down the AHB subsystem using the GPSCTL[XBR_HRQ] bit.
- *Peripheral subsystem.* Halt the individual on-device peripherals such as the DDR memory controller, Ethernet MAC, HDI16, TDM, UART, I^2C, and timer modules.

For details, see the “Clocks and Power Management” chapter of the *MSC711x Reference Manual*.

2.7 Power Supply Design

One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3 V supply can be used. However, a separate adjustable linear regulator supply for the core voltage V_{DDC} should be implemented. For the memory power supply, regulators are available that take care of all DDR power requirements.

3 Reset and Boot

This section describes the recommendations for configuring the MSC711x at reset and boot.

3.1 Reset Circuit

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC711x output current, the pull-up value should not be too small (a 1 KΩ pull-up resistor is used in the MSC711xADS reference design).

3.2 Boot

Table 2 shows the MSC711x boot mode pins BM[3–0]. These signals are sampled at the deassertion (rising edge) of PORESET. For details, refer to the Reset chapter of the *MSC711x Reference Manual*. After a power-on reset, the PLL is bypassed and the device is directly clocked from the CLKIN pin. Thus, the device operates slowly during the boot process. After the boot program is loaded, it can enable the PLL and start the device at a higher speed. An MSC711x device can boot from an external host through the HDI16 or download a user program through the I^2C port. For the MSC7110, MSC7112, MSC7113, MSC7115, and MSC7116, the boot operating mode is set by configuring the BM[1–0] signals sampled at the rising edge of PORESET. For the MSC7118 and MSC7119, two additional boot mode pins BM[3–2] determine the PLL settings.

Table 2. Boot Mode Signals

Signal	Description	Settings
BM[3–0]	Determines boot mode.	For the MSC7110, MSC7112, MSC7113, MSC7115 and MSC7116, only BM[1–0] are used: **BM[1–0] Boot Mode** 00 Boot from HDI16. Bypass PLL. 01 Boot from I^2C. Bypass PLL. 1x Reserved For the MSC7118 and MSC7119, BM[3–0] are used: **BM[3–0] Boot Mode** 0000 Boot from HDI16. Bypass PLL. 0001 Boot from I^2C. Bypass PLL. 0010 Boot from HDI16. $F_{out} = F_{in} \times 32/2/2$ 0011 [1]Boot from Test Mode. $F_{out} = F_{in} \times 32/2$ 0100 Boot from HDI16. $F_{out} = F_{in} \times 12/2$ 0101 Boot from HDI16. $F_{out} = F_{in} \times 12/1$ 0110 Reserved 0111 Boot from HDI16. $F_{out} = F_{in} \times 12/3$ 1000 Boot from main SPI. Bypass PLL. 1001 Boot from main SPI. $F_{out} = F_{in} \times 17/2$ 1010 Boot from main SPI. $F_{out} = F_{in} \times 16/2/2$ 1011 Boot from main SPI. $F_{out} = F_{in} \times 18/3/2$ 1100 Boot from alternate SPI. Bypass PLL. 1101 Reserved 1110 Reserved 1111 [1]Boot from Test Mode. $F_{out} = Fin \times 16/2$
SWTE	Determines watchdog functionality.	0 Watchdog timer disabled. 1 Watchdog timer enabled.
HDSP	Configures HDI16 strobe polarity.	0 Host Data strobes active low. 1 Host Data strobes active high.
H8BIT	Configures HDI16 operation mode.	0 HDI16 port configured for 16-bit operation. 1 HDI16 port configured for 8-bit operation.

Notes: 1. For internal use only.

3.2.1 HDI16 Boot

If the MSC711x device boots from an external host through the HDI16, the port is configured as follows:

- Operate in Non-DMA mode.
- Operate in Polled mode on the device side.
- Operate in Polled mode on the external host side.
- External host must write four 16-bit values at a time with the first word as the most significant and the fourth word as the least significant.

When the device is booted from a power-on reset, the HDI16 is additionally configurable as follows:

- 8- or 16-bit mode as specified by the H8BIT pin.
- Data strobe as specified by the HDSP and HDDS pins.

These pins are sampled only at the deassertion of power-on reset. During a boot from a hard reset, the configuration of these pins is unaffected.

Note: When the HDI16 is used for booting or other purposes, bit 0 is the least significant bit and not the most significant bit as for other DSP products.

3.2.2 I^2C Boot

When the MSC711x device is configured to boot from the I^2C port, the boot program configures the GPIO pins shared with the I^2C pins as I^2C pins. The I^2C interface is configured as follows:

- I^2C in master mode.
- EPROM in slave mode.

For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

3.2.3 SPI Boot

When the MSC7118 or MSC7119 device is configured to boot from SPI, the boot program configures the GPIO pins to emulate SPI signals to boot from an SPI Flash or EEPROM device. The SPI boot has two sub-modes: main SPI and alternate SPI. They differ in the GPIO signal pins used to emulate the SPI. The pin assignments are shown in **Table 3**.

Table 3. Main and Alternate SPI Pin Assignments

Sub-Mode	SPI Pin	GPIO
Main SPI (Boot modes 8, 9, 10, 11)	SPISEL	HA3
	SPICLK	BM2
	MOSI	BM3
	MISO	HCS2
	ERROR	EVNT3
Alternate SPI (Boot mode 12)	SPISEL	SDA
	SPICLK	URXD
	MOSI	UTXD
	MISO	SCL
	ERROR	EVNT3

4 DDR Memory

The MSC711x memory controller provides a glueless interface to external DDR SDRAM memory modules with class 2 series stub termination logic 2.5 V (SSTL_2). There are two termination techniques, as shown in **Figure 2**. Technique A, a more conservative scheme, can be used with longer trace lengths. Technique B is less conservative and uses less power. Use the IBIS models available on the Freescale web site to evaluate device performance.

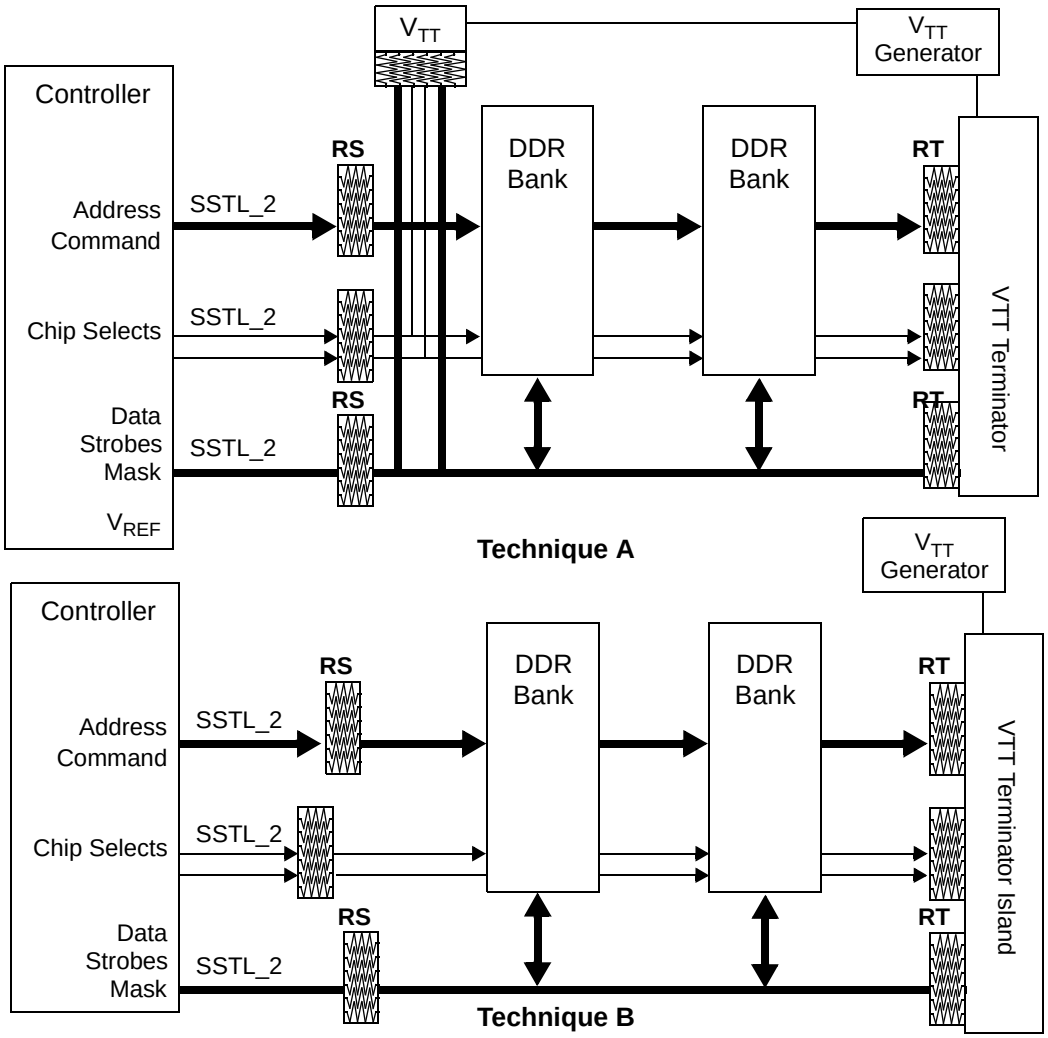

Figure 2. SSTL Termination Techniques

Figure 3 illustrates typical resistor values.

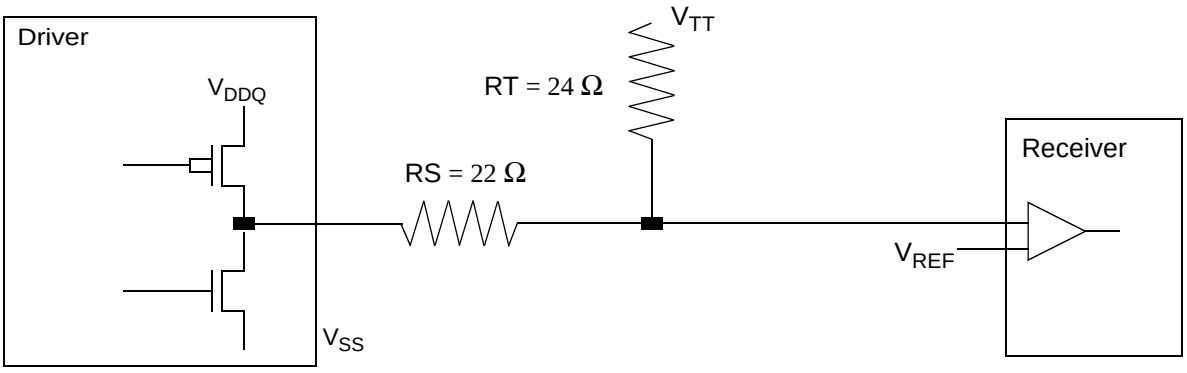

Figure 3. SSTL Power Values

4.1 V_{REF} and V_{TT} Design Constraints

V_{TT} and V_{REF} are isolated power supplies at the same voltage, with V_{TT} as a high current power source. This section outlines the voltage supply design needs and goals:

- Minimize the noise on both rails.
- V_{TT} must track variation in the V_{REF} DC offsets. Although they are isolated supplies, one possible solution is to use a single IC to generate both signals.
- Both references should have minimal drift over temperature and source supply.
- It is important to minimize the noise from coupling onto V_{REF} as follows:
  - Isolate V_{REF} and shield it with a ground trace.
  - Use 15–20 mils track.
  - Use 20–30 mils clearance between other traces for isolating.
  - Use the outer layer route when possible.
  - Use distributed decoupling to localize transient currents and return path and decouple with an inductance less than 3 nH.
- Max source/sink transient currents of up to 1.8 A for a 32-bit data bus.
- Use a wide island trace on the outer layer:
  - Place the island at the end of the bus.
  - Decouple both ends of the bus.
  - Use distributed decoupling across the island.
  - Place SSTL termination resistors inside the V_{TT} island and ensure a good, solid connection.
- Place the V_{TT} regulator as closely as possible to the termination island.
  - Reduce inductance and return path.
  - Tie current sense pin at the midpoint of the island.

4.2 Decoupling

The DDR decoupling considerations are as follows:

- DDR memory requires significantly more burst current than previous SDRAMs.
- In the worst case, up to 64 drivers may be switching states.
- Pay special attention and decouple discrete ICs per manufacturer guidelines.
- Leverage V_{TT} island topology to minimize the capacitors to supply the burst current of the termination rail.
- See the Micron DesignLine publication entitled *Decoupling Capacitor Calculation for a DDR Memory Channel* (`http://download.micron.com/pdf/pubs/designline/3Q00dl1-4.pdf`).

4.3 General Routing

The general routing considerations for the DDR are as follows:

- All DDR signals must be routed next to a solid reference:
  - For data, next to solid ground planes.
  - For address/command, power planes if necessary.
- All DDR signals must be impedance controlled. This is system dependent, but typical values are 50–60 ohm.
- Minimize other cross-talk opportunities. As possible, maintain at least a four times the trace width spacing between all DDR signals to non-DDR signals.
- Keep the number of vias to a minimum to eliminate additional stubs and capacitance.
- Signal group routing priorities are as follows:
  - DDR clocks CK and $\overline{\text{CK}}$.
  - Route MVTT/MVREF.
  - Data group D[31–0], DQM[3–0], and DQS[3–0].
  - Command/address $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, A[13–0], and BA[1–0].
- Minimize data bit jitter by trace matching.

4.4 Routing Clock Distribution

The DDR clock distribution considerations are as follows:

- DDR controller supports six clock pairs:
  - 2 DIMM modules.
  - Up to 36 discrete chips.
- For route traces as for any other differential signals:
  - Maintain proper difference pair spacing.
  - Match pair traces within 25 mils.
- Match all clock traces to within 100 mils.
- Keep all clocks equally loaded in the system.

- Route clocks on inner critical layers.

4.5 Data Routing

The DDR data routing considerations are as follows:

- Route each data group (8-bits data + DQS + DM) on the same layer. Avoid switching layers within a byte group.
- Take care to match trace lengths, which is extremely important.
- To make trace matching easier, let adjacent groups be routed on alternate critical layers.
- Pin swap bits within a byte group to facilitate routing (discrete case).
- Tight trace matching is recommended within the DDR data group. Keep each 8-bit datum and its DM signal within ± 25 mils of its respective strobe.
- Minimize lengths across the entire DDR channel:
  - Between all groups maintain a delta of no more than 500 mils.
  - Allows greater flexibility in the design for readjustments as needed.
- DDR data group separation:
  - If stack-up allows, keep DDR data groups away from the address and control nets.
  - Route address and control on separate critical layers.
  - If resistor networks (RNs) are used, attempt to keep data and command lines in separate packages.

4.6 Considerations for Multiple DSPs

If multiple MSC711x DSP devices reside closely on a board, adjacent DDR data groups should be routed on alternating critical board layers as shown in **Figure 4**. Note that simultaneous switching draws more power if the clocks on DSPs are synchronized.

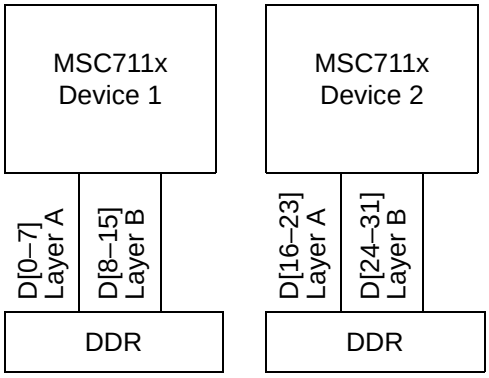

Figure 4. Example of Data Routing For Multiple DSPs

4.7 Considerations for No DDR

When DDR memory is not used, the following steps are recommended to disconnect the 2.5 V supply and disable the DDR memory controller.

- Connect the 2.5 V supply to the 1.2 V supply on the board. It is not necessary to connect all the 2.5 V power balls/pins to 1.2 V. Since the external memory interface is inactive, connecting one pair of 2.5 V/1.2 V is sufficient.
- Connect V_{REF} to GND. Connecting one pair of V_{REF}/GND is sufficient.
- Ensure that the DDR port is disabled internally by clearing SCFG[MEMEN]. All DDR pins are disabled/tri-stated if the controller is disabled except for CK and $\overline{CK}$. These pins toggle. To disable CK/$\overline{CK}$, set STOPCTRL[DDRCK] = 01.
- Since the DDR port is disabled, leave all the SSTL pins (input/output) floating/as is. To reduce power consumption, all parallel termination can be removed.

5 OCE10/JTAG Interface

The MSC711x device includes an OCE10 enhanced on-chip emulator that gives internal access to scan chains for debug purposes and provides a serial connection to the SC1400 core for emulator support. An OCE10/JTAG connection adds little or no cost to a system but adds significant advantages during early system development. This interface uses a standard 14-pin header, as shown in **Figure 5**.

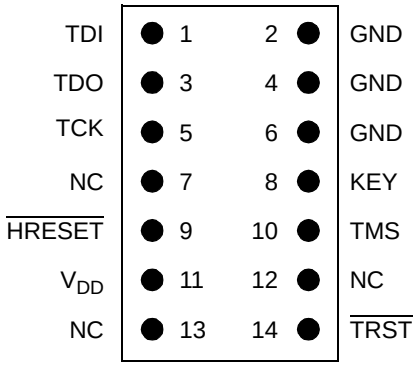

Figure 5. 14-Pin Header for JTAG/Emulator Interface

The emulator interface connects through the JTAG port on an MSC711x device with some additional status monitoring signals. **Table 1** shows the pin definitions and recommendations.

Table 4. JTAG/OCE10 Interface Pin Definitions

Pins	Connection	Description	Recommendations
1	TDI	Test Data In	If there are multiple devices on the JTAG chain, connect TDI to the TDO signal of the previous device in the chain.
2,4, 6	GND	System Ground Plan	Connect to digital ground.
3	TDO	Test Data Out	If there are multiple devices on the JTAG chain, connect TDO to the TDI signal of the next device in the chain.
5	TCK	Test Clock	Add a 10 KΩ pull-up resistor.

Table 4. JTAG/OCE10 Interface Pin Definitions (Continued)

Pins	Connection	Description	Recommendations
7, 13, 12	NC	No Connect	Leave unconnected.
8	KEY	Mechanical Keying	Pin should be removed.
9	$\overline{\text{HRESET}}$	Reset	This pin is bidirectional.
10	TMS	Test Mode Select	None.
11	V_{DD}	I/O Power Supply	Connect to MSC711x I/O Voltage V_{DDIO} through a 220 Ω current limiting resistor.
14	$\overline{\text{TRST}}$	Test Reset	$\overline{\text{TRST}}$ has an internal pull-up, so no external pull-up or pull-down is required. However, you should add a 10k pull-down to GND on this signal to keep the JTAG in reset mode while the device is operating normally.

Connecting multiple devices via their JTAG ports is commonly referred to as *daisy chaining*. Multiple target DSP devices can be connected in a series so that a single command converter and JTAG connector can control multiple target DSP devices. Daisy chaining should be considered for a board with multiple DSPs.

6 Signal Connectivity and Terminations

This section summarizes the connections and special conditions, such as pull-up or pull-down resistors, for the MSC711x devices. Following are guidelines for signal groups and configuration settings:

- Clock and reset signals:
  - SWTE is used to configure the MSC711x device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{DDC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$, this signal can be left floating.
  - BM[3–0] configure the MSC7118 and MSC7119 devices and are sampled until $\overline{\text{PORESET}}$ is deasserted, so they should be tied to V_{DDIO} or GND either directly or through pull-up or pull-down resistors. For MSC7110, MSC7112, MSC7113, MSC7115, and MSC7116 only BM[1–0] are used.
  - $\overline{\text{HRESET}}$ should be pulled up.
  - $\overline{\text{NMI}}$ should be pulled up.
- Interrupt signals:
  - When they are used, $\overline{\text{IRQ}}$ pins must be pulled up.
- HDI16 signals:
  - When they are configured for open-drain, the $\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ signals require a pull-up resistor. However, these pins are also sampled at power-on reset to determine the HDI16 boot mode and may need to be pulled down. When these pins must be pulled down on reset and pulled up otherwise, a buffer can be used with the $\overline{\text{HRESET}}$ signal as the enable.
  - When the device boots through the HDI16, the HDDS, HDSP and H8BIT pins should be pulled up or down, depending on the required boot mode settings.
- Ethernet MAC/TDM2 signals:

— The MDIO signal requires an external pull-up resistor.

- I^2C signals:
  — The SCL and SDA signals, when programmed for I^2C, requires an external pull-up resistor.
- General-purpose I/O (GPIO) signals:
  — An unused GPIO pin can be disconnected. After boot, you should program it as an output pin.
- Other signals:
  — The $\overline{\text{TEST0}}$ pin must be connected to ground.
  — The $\overline{\text{TPSEL}}$ pin should be pulled up to enable debug access via the emulator port and pulled down for boundary scan.
  — Pins labeled No Connect (NC) must not be connected.
  — When a 16-pin double data rate (DDR) interface is used, the 16 unused data pins should be no connects (floating) if the used lines are terminated.

7 Design Checklist Summary

This section summarizes the design recommendations discussed in this document with a space to check off each requirement as it is completed.

✓	Checklist
	Choose the pin assignments. Use Figure 1-1 in the *Technical Data* sheet.
	Determine the requirements for power supply, power sequencing, power planes, decoupling, PLL power supply filtering, and power consumption using **Section 2**, *Power,* on page 2.
	Determine reset configuration, including the boot mode and set the reset configuration pins: H8BIT, BM0, BM1, SWTE, HDSP, HDDS, and DBREQ as specified in **Section 3**, *Reset and Boot,* on page 5.
	Follow the DDR memory pin termination, voltage design, decoupling and routing guidelines as described in **Section 4**, *DDR Memory,* on page 8.
	Design the emulator interface (see **Section 5**, *OCE10/JTAG Interface,* on page 12).
	Follow signal termination guidelines (see **Section 6**, *Signal Connectivity and Terminations,* on page 13).

8 Related Reading

The reference materials listed in **Table 5** can be obtained at the web site listed on the back cover of this document. Visit the relevant product summary page or search by title or document identification number.

Table 5. Related Reading

Document Category	Document Title	Document ID
Data Sheet (Hardware Specifications)	*MSC711x Technical Data* sheet	MSC7110, MSC7112, MSC7113, MSC7115, MSC7116, MSC7118, MSC7119
Errata (device)	MSC711x Silicon Errata	Mask-specific
Manuals	*MSC711x Reference Manual*	MSC711xRM
	SC1000-Family Processor Core Reference Manual (StarCore manual that includes the SC140 core)	10180
	OCE10 On-Chip Emulator Reference Manual	10055
Application Notes	List available on the web site on the back cover of this document	
Reference Design	*MSC711x Application Development System Reference Manual*	MSC711xADSRM
	MSC711xEVM User's Guide	MSC711xEVM
JDEC Standard	JESD8 - Stub Series Terminated Logic for 2.5 Volts (STTL_2)	

9 Revision History

Table 6 provides a revision history for this application note.

Table 6. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	11/2004	Initial release.
1		
2		
3		
4	6/2006	Changed the unit of measure for trace lengths and widths from mm to mils.
5	3/2007	Removed the last sub-bullet from Section 6, "Signal Connectivity and Terminations." The text of the removed sub-bullet is as follows: Do not connect DBREQ to the host processor's DONE signal (as you would for the MSC8101 device). DONE can be connected to one of the EVNTx pins, and DBREQ can be connected to HRRQ.
6	4/2007	Removed a circuit from the Figure 1, " PLL Power Supply Filter Circuits." The circuit removed had V_{CCSYN} and V_{CCSYN1} at the output.
7	6/2008	Changed the resistor value in Figure 1 and the paragraph above it to 2 Ω from 20 Ω.

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