

Using a 32.768kHz Crystal to Generate System Clock and USB in i.MX

MC9328MX1, MC9328MXL, and MC9328MXS

by: **Walter Law**

1 Introduction

The USB modules in the MC9328MX1, MC9328MXL, and MC9328MXS (i.MX) processors accommodate a 32.768 kHz crystal used by both the MCU PLL and the System PLL for system clock generation. This document contains jitter measurement results using a 32.768 kHz crystal to generate not only the MCU PLL and System PLL system clock, but the 48 MHz USB clock as well.

The 48 MHz USB clock is usually generated by an external 16 MHz crystal input to the System PLL. However, to save space and cost, the 48 MHz USB clock can also be generated by a 32.768 kHz crystal.

The jitter generated by both inputs is measured independently and as of this publication date, the jitter measurement results meet *USB Specification* (Revision 1.1). The results show full speed jitter requirements using a 32.768 kHz crystal to generate the 48 MHz USB clock. The USB certification results are provided at the end of this document.

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2 Measurement Setup

The 48 MHz clock for the USB module in the i.MX processors is output to the CLKO pin by writing 0x010 to the CLKO_SEL bits [31:29] of the Clock Source Control Register. A Tektronix TDS7404 digital oscilloscope was used to measure the clock jitter from the CLKO pin on the i.MX Application Development System board (ADS).

The 48 MHz USB clock can be generated by either an external 16 MHz crystal input to System PLL, or by a 32.768 kHz crystal. Independent measurements of USB clock jitter were taken using an external 16 MHz crystal as the source and a 32.768 kHz crystal as the source to the System PLL.

The Clock Source Control Register settings that force output of the 48 MHz USB clock to CLKO pin and for selecting either a 32.768 kHz crystal or 16 MHz crystal for System PLL are shown in Table 1.

Table 1. Clock Source Control Register Settings

Crystal Source for System PLL	Register Value
32.786 kHz	0x4700AC03
16 MHz	0x4743AC03

3 Measurement Results

Table 2 and Table 3 show the jitter measurement results.

Table 2. 48 MHz USB Clock Cycle to Cycle Jitter (MC9328MX1)

MC9328MX1 Sample	32.768 kHz Crystal Input to System PLL		16 MHz Crystal Input to System PLL	
	Mean	Standard Deviation	Mean	Standard Deviation
Sample 1	78.577ps	78.061ps	53.180ps	62.871ps
Sample 2	42.265ps	46.839ps	44.647ps	54.500ps
Sample 3	37.854ps	45.054ps	50.21ps	68.534ps
Sample 4	37.247ps	47.666ps	57.488ps	68.098ps
Sample 5	36.751ps	43.071ps	37.961ps	46.288ps
Sample 6	59.435ps	69.435ps	63.224ps	68.27ps
Sample 7	41.756ps	49.371ps	40.353ps	50.153ps
Sample 8	33.747ps	39.792ps	37.749ps	50.972ps
Sample 9	44.191ps	53.187ps	47.298ps	54.892ps
Sample 10	67.917ps	70.497ps	68.339ps	67.360ps

Table 3. 48 MHz USB Clock Cycle to Cycle Jitter (MC9328MXL)

MC9328MXL Sample	32.768 kHz Crystal Input to System PLL		16 MHz Crystal Input to System PLL	
	Mean	Standard Deviation	Mean	Standard Deviation
Sample 1	51.248ps	77.737ps	44.985ps	62.388ps
Sample 2	57.679ps	80.717ps	58.09ps	77.656ps
Sample 3	61.789ps	86.31ps	56.239ps	84.976ps
Sample 4	90.048ps	75.384ps	53.653ps	70.263ps
Sample 5	111.07ps	86.314ps	93.813ps	78.693ps
Sample 6	54.392ps	75.725ps	51.183ps	70.409ps
Sample 7	94.043ps	61.543ps	64.125ps	91.549ps
Sample 8	87.243ps	78.685ps	83.926ps	77.376ps
Sample 9	126.37ps	92.748ps	64.923ps	92.584ps
Sample 10	63.332ps	92.516ps	62.27ps	90.343ps

Table 4. Cycle to Cycle Values (MC9328MX1/MC9328MXL)

MC9328MX1	32.768 kHz	16 MHz
Maximum cycle to cycle jitter mean value	78.577ps	68.339ps
Maximum cycle to cycle jitter standard deviation	78.061ps	68.534ps
MC9328MXL	32.768 kHz	16 MHz
Maximum cycle to cycle jitter mean value	126.37ps	93.813ps
Maximum cycle to cycle jitter standard deviation	92.748ps	92.584ps

4 USB Certification Results

The i.MX processor ADS can achieve USB certification using a 32.768 kHz crystal input to the MCU PLL and System PLL for generation of the system clock and the 48 MHz USB clock. As of this publication date, overall test results pass the current requirements. The USB certification results are provided at the end of this document. The Table 5 and Figure 1 on page 4 highlight the individual test results regarding signal quality.

Table 5. Jitter Measurement Results (Signal Quality and Eye Diagram)

Measurement Parameter	Pass/Fail
Signal eye:	Eye Passes
Measured signaling rate: 12.0028 MHz	Signal Rate Passes
E Receivers: reliable operation on tier 6	Receivers Pass

Conclusions

Table 5. Jitter Measurement Results (Signal Quality and Eye Diagram) (continued)

Measurement Parameter	Pass/Fail
Consecutive jitter range: -0.2ns to 0.3ns RMS jitter 0.2ns Paired JK jitter range: -0.1ns to 0.2ns, RMS jitter 0.1ns Paired KJ jitter range: -0.3ns to 0.2ns, RMS jitter 0.2ns	Jitter Passes
EOP width: 167.77ns	EOP Width Passes

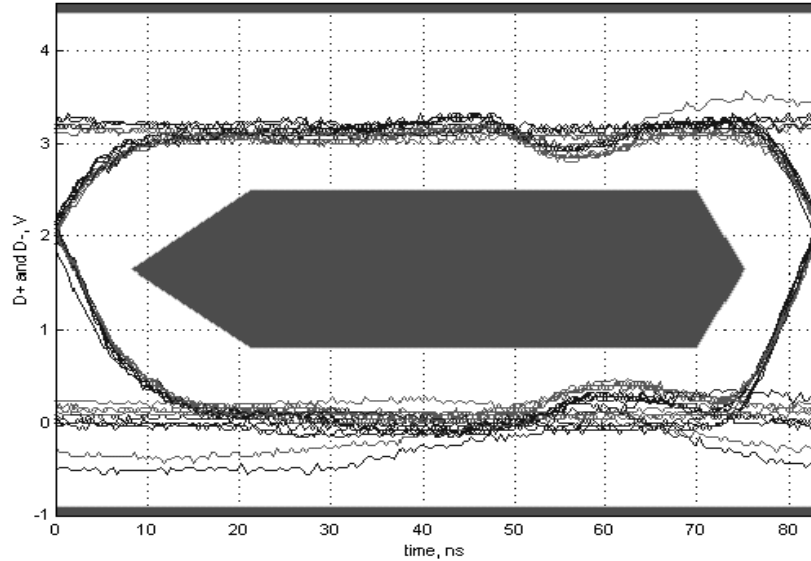


Figure 1. Jitter Measurement

5 Conclusions

1. There is no significant difference shown in jitter measurement results for the 48 MHz USB clock generated by either a 32.768 kHz crystal or a 16 MHz crystal.
2. With a 32.768 kHz crystal generating both system clock and 48 MHz USB clock, the i.MX processors pass the USB revision 1.1 requirements at full speed device test and can achieve USB certification.
3. In view of broad space saving and cost minimization issues, Freescale recommends using a 32.768 kHz crystal used by the MCU PLL and System PLL to generate both the system clock and the 48 MHz USB clock.

6 Appendix

Appendix attached: USB Certification Test Results

NOTES



NSTL Full & Low Speed Device Test Report

Company Name:	Freescale Semiconductors Hong Kong Ltd.
Model Name:	DragonBall MX-1 ADS
Device Type:	Non-hub device
Issue Date:	04/17/2003
Test Result:	PASS



Test Report

USB-IF Pretest Report

Company

Company Name: Freescale Semiconductors Hong Kong Ltd.
VID (Dec) 1061 The VID for the company who apply the USB-IF logo.

Technical Contact

Name: Roy Leung
Phone Number: (852) 2666 8934
E-Mail: royleung@freescale.com
FAX Number: (852) 2615 9214

Marketing Contact

Name: Walter Law
Phone Number: (852) 26668293
E-Mail: Walter.Law@freescale.com
FAX Number: (852) 2615 9214

Device Information:

- Retail Device Device Chipset
- Hi Power Low Power
- Bus Powered Self Powered Both
- Full Speed Low Speed
- Untethered B Tethered

Device Name: DragonBall MX-1 ADS Device Class: Full speed

Embedded Function: _____ Other: _____

VID: 1061 PID: 0001

Tested O.S. Win98SE Win2000 and/or WinXP (Standard test fee will cover 1 OS only.)

Tester: [Eric Chen](#)
Review: [James Ou](#)
Date: [04/17/2003](#)

Over All Test Result: Pass



Frameworks Test Result: Pass Fail

Chapter 9: Pass Fail HID View: Pass Fail N/A

Interface: 1 MAX Power: 2 mA Remote Wakeup: N/A

Chapter 11: Pass Fail N/A HUB Port #: _____

Power Current Test Result: Pass Fail

Operating Power: 0 mA **Unconfiguration Power: 0 mA (<100mA)**

(=< Max Power =< 100mA for Low Power)
(=< Max Power =< 500mA for High Power)

(=<Max Power =< 100mA)

Configuration Power: 0 mA

(=< Max Power =< 100mA for Low Power)
(=< Max Power =< 500mA for High Power)

Suspend Mode Power: 0 uA

(=< 2500uA for High Power /w Remote Wake Up)
(=< 500uA x Port# for HUB) (=< 500uA for others)

Interoperability Test Result: Pass Fail OS: 98SE W2k XP

UHCI Controller: Pass Fail OHCI Controller: Pass Fail

EHCI Controller: Pass Fail

Signal Quality Test Result: Pass Fail

Up Stream SQ: Pass Fail Inrush Current: Pass Fail
(=< 100mA and 200uA)

Down Stream SQ: Pass Warning N/A

Drop/ Droop Test Result: Pass Fail N/A

For Self Powered HUB:

V_{non-load}: _____ V V_{load}: _____ V V_{drop}: _____ V V_{droop}: _____ mV
(=<500mV) (=<330mV)

For BUS Powered HUB

V_{upstream}: _____ V V_{downstream}: _____ V V_{drop}: _____ V V_{droop}: _____ mV
(=<100mV or 350mV "Tethered") (=<330mV)

Back Voltage Test : Pass Fail

D+: 62mV/ 0V D-: 0/ 0 V V_{bus}: 52mV/ 58mV
(All values =< 400mV)

Using a 32.768kHz Crystal to Generate System Clock and USB in i.MX Application Note, Rev. 1



Test Report

More Detail Test Result:

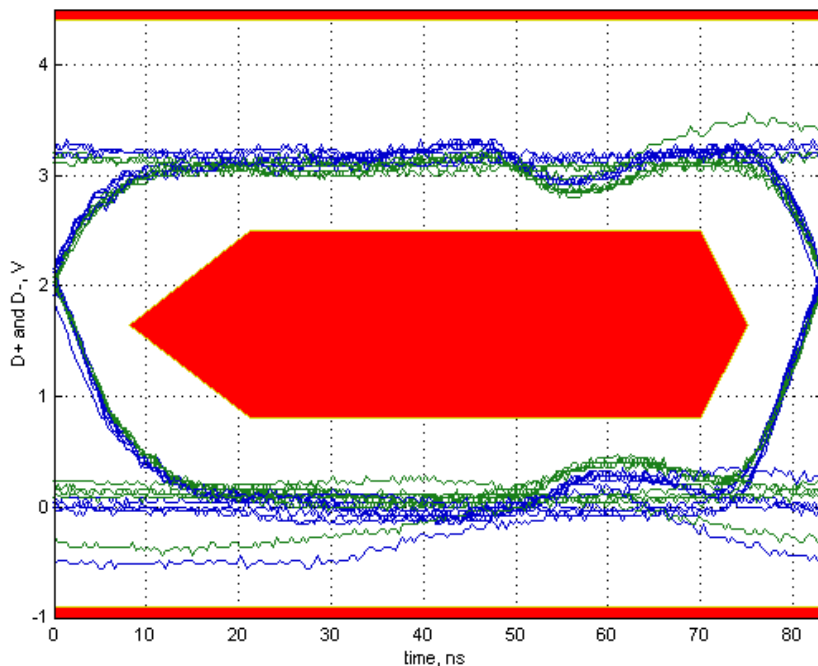
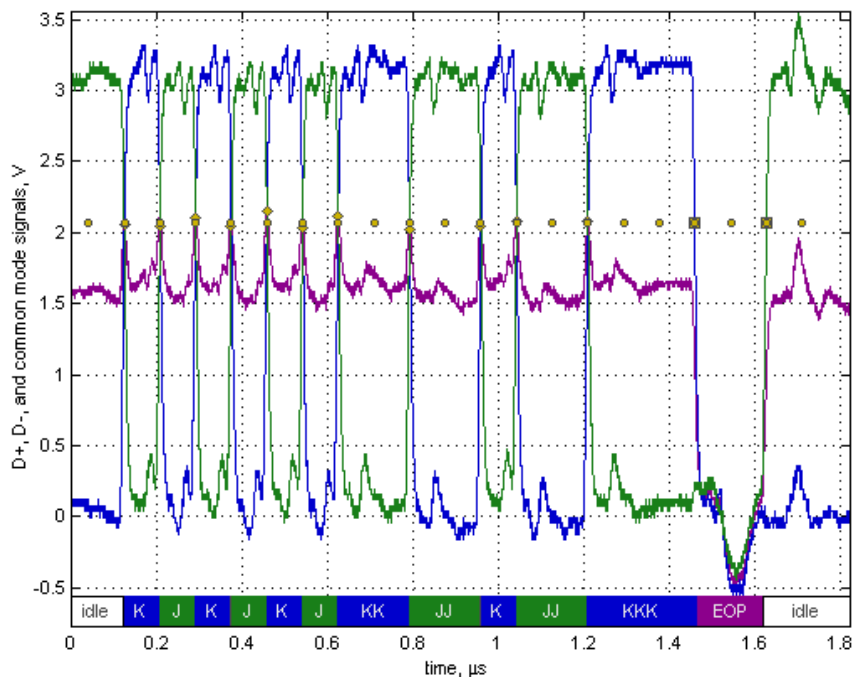
1. Note:

The VID of DUT is 0x425 on the system.

2. Full Speed Up Stream SQ: Pass with warning

- Overall result: pass!
- Signal eye:
eye passes
- EOP width: 167.77ns
EOP width passes
- Receivers: reliable operation on tier 6
receivers pass
- Measured signaling rate: 12.0028MHz
signal rate passes
- Crossover voltage range: 2.02V to 2.15V, mean crossover 2.07V
(first crossover at 2.06V, 10 other differential crossovers checked)
*** crossover voltage failure! *** (minimum 1.30V, maximum 2.00V)
*** waiver granted ***
- Consecutive jitter range: -0.2ns to 0.3ns, RMS jitter 0.2ns
Paired JK jitter range: -0.1ns to 0.2ns, RMS jitter 0.1ns
Paired KJ jitter range: -0.3ns to 0.2ns, RMS jitter 0.2ns
jitter passes

[Signal Data and Eye](#)



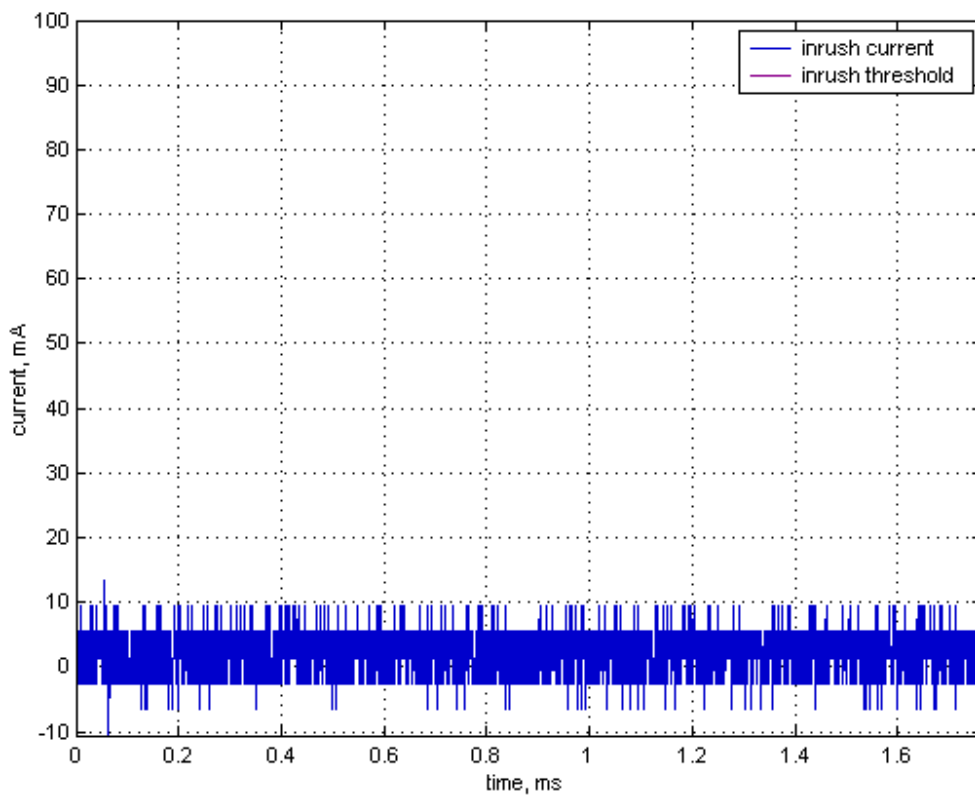


Test Report

3. Inrush Current: Pass

- Overall result: pass!
- Inrush at 5.150V: 0 μ C
inrush passes

Hot Plug (Attach) Current Draw



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