Freescale Semiconductor
Application Note

Document Number: AN2478
Rev. 5, 02/2007

Using the SDRAM Controller

MC9328MX1, MC9328MXL, and MC9328MXS

By: Michael Kjar

1 Introduction

This document provides a comprehensive discussion on how the Freescale Semiconductor's i.MX applications processors interface to different configurations of SDRAM memory devices and how to initialize these devices and their mode registers. By providing an overview of the i.MX SDRAM Controller and its address multiplexing scheme, systems designers will better understand how to interface their SDRAM memory with the i.MX processors. This document provides several examples of different SDRAM memory configurations and provides an overview of the SDRAM memory initialization scheme and mode register programming aimed to further increase system designer understanding on how to use the i.MX SDRAM Controller. The i.MX devices affected by this discussion are:

- MC9328MX1
- MC9328MXL
- MC9328MXS

The examples provided in this document assume that the number of rows and columns for each given SDRAM density follow the JEDEC standard. The SDRAM

Contents

Controller can interface to SDRAMS that do not follow the JEDEC standards for row and column sizes, however the user must ensure that the SDRAM Control Register bits ROW and COL are programmed to the appropriate number of rows and columns given in the SDRAM data sheet. These examples do not cover non-JEDEC standard SDRAMS.

2 Overview of the i.MX SDRAM Controller

The i.MX is an application processor targeted for low-power, portable applications. Part of the rich feature set of the i.MX processor includes the on-chip SDRAM controller. The i.MX SDRAM controller includes the following features:

- Supports 4 banks of 64, 128, or 256 Mbit synchronous DRAMs
- Includes 2 independent chip-selects
  - Up to 64 Mbytes per chip-select
  - Up to four banks simultaneously active per chip-select
  - JEDEC standard pinout/operation
- Supports Micron's SyncFlash SDRAM-interface burst flash memory
  - Boot capability from CSD1
- PC100 compliant interface
  - 100 MHz system clock achievable with "-8" option PC100 compliant memories
  - Single and fixed-length (8-word) word access
  - Typical access time of 8-1-1-1-1-1-1-1 at 100 MHz (8-word burst to match cache line fill)
  - Single clock cycle writes achieving same data throughput as burst writes
- Software configurable bus width, row, and column sizes and delays for differing system requirements
- Hardware supported self-refresh entry and exit which keeps data valid during system reset and low-power modes
- Auto-powerdown (clock suspend) timer

Figure 1 on page 3 shows a block diagram of the i.MX SDRAM Controller. This figure shows the mulitplexing configuration between the SDRAM controller internal signals to the external signals of the i.MX bus. Refer to the SDRAM Controller chapter of the appropriate i.MX reference manual for more details on the SDRAM Controller (See Section 3, "Reference Documents").

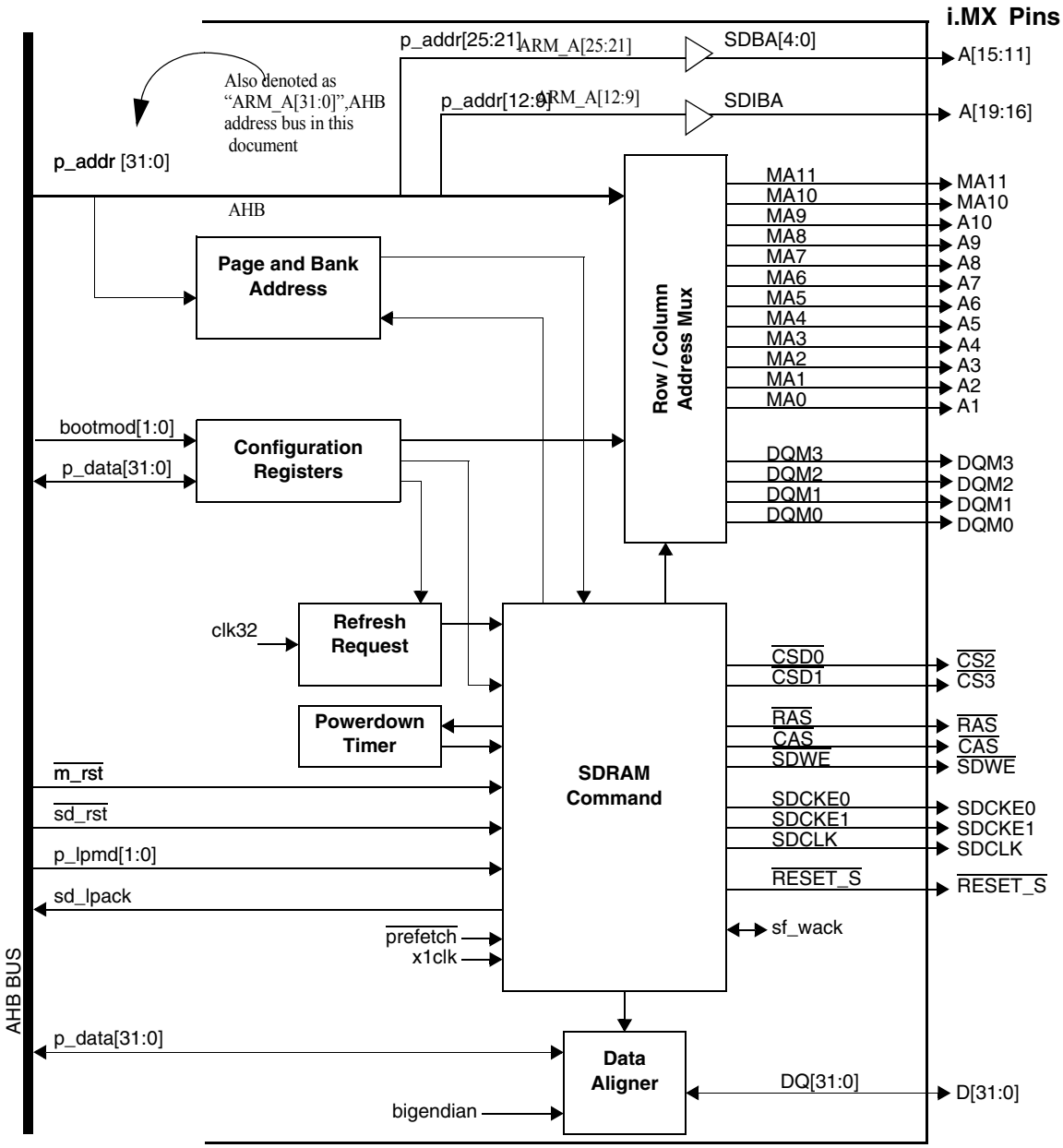

Figure 1. SDRAM Controller Block Diagram

2.1 i.MX SDRAM Control Register Overview

In the i.MX SDRAM Controller there are two SDRAM control registers, one for each of the two memory arrays.

1. SDCTL0 defines the operating characteristics for the SDRAM 0 region (selected by $\overline{\text{CSD0}}$ which is muxed with $\overline{\text{CS2}}$)
2. SDCTL1 does the same for the SDRAM 1 region (selected by $\overline{\text{CSD1}}$ which is muxed with $\overline{\text{CS3}}$).

Bit field assignments within the registers are identical. The following figure shows the SDRAM control register and Table 1 on page 6 shows the memory arrays associated with each register.

2.1.1 SDRAM Control Register (SDCTL0 and SDCTL1)

		Addr
SDCTL0	SDRAM 0 Control Register	**0x00221000**
SDCTL1	SDRAM 1 Control Register	**0x00221004**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SDE	SMODE			SP		ROW				COL		IAM		DSIZ	
TYPE	rw	rw	rw	rw	rw	r	rw	rw	r	r	rw	rw	rw	r	rw	rw
RESET	0*	0	0	0	0	0	0	1	0	0	0	0	0	0	0*	0*
	0x0100*															

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SREFR		CLKST		CI		SCL			SRP	SRCD			SRC		
TYPE	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	r	rw	rw	rw
RESET	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
	0x0300															

* For SDCTL1, the reset state is affected by bootmod [1:0]

The following list gives a brief overview of each bit field's function. Refer to the SDRAM chapter of the i.MX reference manual for further details of the SDCTL0 and SDCLT1 bit definitions.

- SDE (SDRAM Controller Enable), set to 1 to enable.
- SMODE (SDRAM Controller Operation Mode), set to various modes depending on the desired operation. The following list describes these bit settings:
  - 000 = Normal Read/Write
  - 001 = Precharge Command
  - 010 = Auto-Refresh Command
  - 011 = Set Mode Register Command
  - 100, 101 = Reserved
  - 110 = SyncFlash Load Command Register
  - 111 = SyncFlash Program Read/Write
- SP (Supervisor Protect), set to 0 to allow user mode accesses, or set to 1 to prohibit user mode accesses.
- ROW (Row Address Width), set to the number of row address bits given by the SDRAM memory data sheet:
  - 00 = 11 ROW addresses
  - 01 = 12 ROW addresses
  - 10 = 13 ROW addresses
  - 00 = Reserved
- COL (Column Address Width), set to the number of COL address bits given by the SDRAM memory data sheet:
  - 00 = 8 COL addresses
  - 01 = 9 COL addresses
  - 10 = 10 COL addresses
  - 11 = 11 COL addresses

- IAM (Bank Interleaved Address Mode), set to 0 for linear bank addressing, or set to 1 for interleaved bank addressing. The following section provides more detail on this function.
- DSIZ (Data Width), set to 00 for 16-bit memory residing on D[31:16], set to 01 for 16 bit memory residing on D[15:0], or 1x for 32-bit memory.
- SREFR (SDRAM Refresh Rate), set according to the refresh rate dictated by the SDRAM memory data sheet. Setting this bit field to 00 disables auto refresh. Setting this field to 01 will refresh one row every 32kHz clock edge for a total of 2048 rows refreshed every 64 ms. Setting this field to 10 will refresh two rows every 32kHz clock edge for a total of 4096 rows refreshed every 64 ms, and a setting of 11 will refresh four rows every 32kHz clock edge for a total of 8192 rows refresh every 64 ms. Multiple refresh cycles are separated by the row cycle delay given in the SRC field.
- CLKST (Clock Suspend Timeout)—Determines if and when the SDRAM will be placed in a clock suspend condition. If enabled, the SDRAM controller will disable the SDCLK and bring SDCKE low during times when the SDRAM is not being accessed, but will still issue auto refresh cycles at the specified rate given in SREFR. The count based time-outs do not force the SDRAM into idle mode. The bit settings for this field are:
  - 00 = Disabled
  - 01 = Any time banks are inactive
  - 10 = 64 clocks after completion of last access
  - 11 = 128 clocks after completion of last access
- CI (Cache Inhibit), set to 00 to disable cache inhibit. This function is not necessary and must be disabled in a system having an MMU which can mark the cache inhibit space itself.
- SCL (SDRAM CAS Latency), set to 01 for CAS of 1, set to 10 for CAS of 2, or set to 11 for CAS of 3 (ensure the SDRAM memory mode register is programmed with the same CAS latency).
- SRP (SDRAM Row Precharge Delay), set to 0 for 3 clocks or 1 for 2 clocks to be inserted between a precharge command and the next row activate.
- SRCD (SDRAM Row to Column Delay)—Determines the number of clocks to be inserted between a row activate command and a subsequent read or write command to the same bank.
  - 00 = 4 clocks inserted
  - 01 = 1 clock inserted
  - 10 = 2 clocks inserted
  - 11 = 3 clocks inserted
- SRC (SDRAM Row Cycle Delay)—Determines the number of clocks to be inserted between a refresh and any subsequent refresh or read/write access.
  - 000 = 8 clocks
  - 001 = 1 clock
  - 010 = 2 clocks
  - 011 = 3 clocks
  - 100 = 4 clocks
  - 101 = 5 clocks
  - 110 = 6 clocks
  - 111 = 7 clocks

The SDRAM arrays are mapped according to Table 1. For the examples listed in this app note, the SDRAM will reside on $\overline{CS2}$ with the base address of 0x08000000.

Table 1. SDRAM Area Memory Map

Address	Use	Access
0x0800 0000 – 0x0BFF FFFF	SDRAM 0 Memory array	R/W
0x0C00 0000 – 0x0FFF FFFF	SDRAM 1 Memory array	R/W

2.1.2 Bank Address Interleaving

Bank address interleaving is simply another way to control bank address alignment and takes advantage of keeping the same page open across multiple banks. In linear bank addressing (IAM = 0), the address field is such that the bank addresses are the most significant address bits, followed by the row and column address bits. Pictorially, this can be seen as:

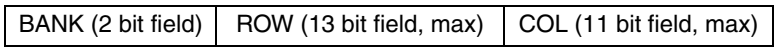

Figure 2. Linear Bank Address Field

Figure 2 shows the address field for linear bank addressing assuming the maximum ROW and COL bit settings of the i.MX. For interleaved bank addressing, the bank address bits are swapped with the row address bits, resulting in an interleaved memory map with the banks alternately striped through the memory region. The following figure shows this concept, again assuming the maximum ROW and COL bit settings of the i.MX.

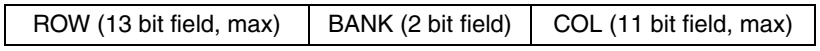

Figure 3. Interleaved Bank Address Field

Figure 4 further illustrates these bank address interleaving options.

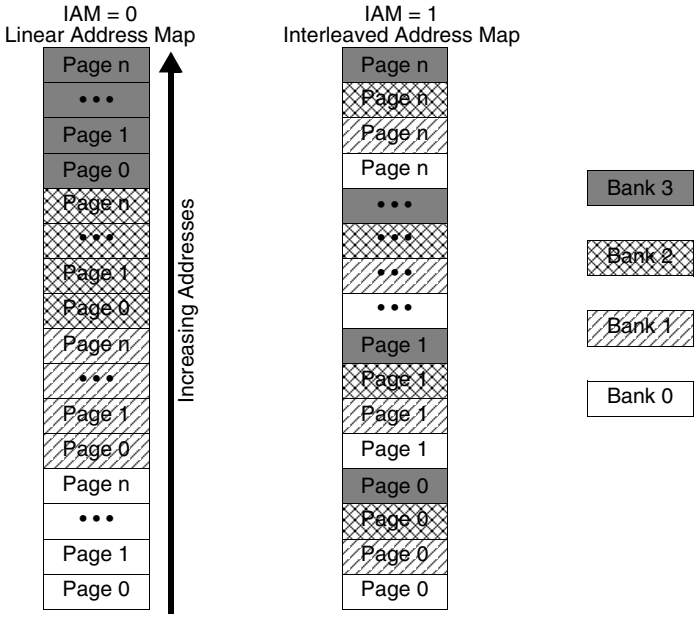

Figure 4. Memory Bank Interleaving Options

Take for example, a 256 Mbyte SDRAM configured as 4M x 16 x 4, has a page size (number of bits in a row) of 8192 or 1024 bytes. In linear bank addressing, the user is limited to this page size of 1024 bytes before issuing a Precharge and Active command to access another page within the same bank. Even using the minimum timing settings given in the SRP (Precharge to Activate) and SRCD (Active to Read) bit fields, this can still take up to 3 clock cycles. In bank interleaved addressing, the 1024 byte page can stay open in bank 0 and the same page can then be open in subsequent banks. Once an Active command has been given for each bank, the effective page size is 4096 bytes (1024 bytes x 4 banks), thereby increasing performance as this eliminates the minimum 3 clock cycle Precharge and Active command that linear bank addressing requires. The downside to interleaved bank addressing is the fact the all four banks would be active, which in turn draws more power than if only one bank was active. This point must also be considered when using low-power SDRAMs with Partial Array Self Refresh (PASR). With PASR, the user has the option to restrict self refresh operations from four to two or one banks, resulting in lower power consumption. However, those banks that are not refreshed will lose data. Since interleaved mode uses all four banks, restricting refresh operations to one or two banks will result in a loss of system data. Therefore, it is recommended when using low-power SDRAMs, that the user choose the linear bank addressing mode of operation.

2.1.3 SDRAM Controller Interface Signals

The Table 2 illustrates the SDRAM controller interface signals. Refer to Figure 1 and the i.MX reference manual for more details on these signals.

Table 2. SDRAM Controller Interface Signals

SDRAMC Signal Name	i.MX Pin Name	Function	Direction	Reset State
SDCLK	SDCLK	Clock to SDRAM	Output	Enabled
SDCKE0	SDCLKE0	Clock enable to SDRAM 0	Output	High
SDCKE1	SDCLKE1	Clock enable to SDRAM 1	Output	High
$\overline{\text{CSD0}}$	$\overline{\text{CS2}}$	Chip-select to SDRAM array 0	Output	High
$\overline{\text{CSD1}}$	$\overline{\text{CS3}}$	Chip-select to SDRAM array 1	Output	High
MA [11:10]	MA [11:10]	Multiplexed Address	Output	Low
MA [9:0]	A [10:1]	Multiplexed Address	Output	Low
SDBA [4:0] / A [25:21]	A [15:11]	Non-multiplexed Address	Output	Low
SDIBA [3:0] / A [12:9]	A [19:16]	Non-multiplexed Address	Output	Low
DQM3	DQM3	Data Qualifier Mask byte 3 (D [31:24])	Output	Low
DQM2	DQM2	Data Qualifier Mask byte 2 (D [23:16])	Output	Low
DQM1	DQM1	Data Qualifier Mask byte 1 (D [15:8])	Output	Low
DQM0	DQM0	Data Qualifier Mask byte 0 (D [7:0])	Output	Low
DQ[31:0]	D[31:0]	Data bus	I/O	High
$\overline{\text{SDWE}}$	$\overline{\text{SDWE}}$	Write Enable	Output	High
$\overline{\text{RAS}}$	$\overline{\text{RAS}}$	Row Address Strobe	Output	High
$\overline{\text{CAS}}$	$\overline{\text{CAS}}$	Column Address Strobe	Output	High
$\overline{\text{RESET\_SF}}$	$\overline{\text{RESET\_SF}}$	SyncFlash Reset/Powerdown	Output	Low

2.2 SDRAM Controller Address Muxing

All SDRAM memories incorporate address multiplexing between row and column address bits, allowing the row and column address bits to share the same address bus. To account for the address multiplexing, the SDRAM Controller uses a row/column Address Mux to properly align the i.MX ARM AHB address bits to the correct address bits of the SDRAM memory device. Figure 1 illustrates the row/column Address Mux, where the input to the row/column Address Mux is the internal AHB address bus and the outputs are the multiplexed addresses MA0 through MA11. The row and COL bit settings in the SDCTL0 and SDCTL1 register determine how the internal AHB address bus is aligned with the SDRAM Controller's multiplexed address bits MA0 through MA11. These multiplexed address bits are then brought out to the external address pins of the i.MX, as shown in Figure 1 on page 3. The figure shows that MA0 through MA9 are shared with the external address pins A1 through A10, where MA10 and MA11 are not shared with the external address bus but are directly brought out as MA10 and MA11. Table 3 also re-iterates this.

Table 3. SDRAM Controller Multiplexed Address Bus

SDRAMC Multiplexed Address Signal Name	i.MX Address Pin Name
MA0	A1
MA1	A2
MA2	A3
MA3	A4
MA4	A5
MA5	A6
MA6	A7
MA7	A8
MA8	A9
MA9	A10
MA10	MA10
MA11	MA11

The SDRAM Controller multiplexed address bus is aligned to the column addresses so that the internal AHB address line ARM-A1 always appears on pin MA0. With this alignment, the "folding point" in the address multiplexer is driven solely by the number of column address bits (COL in the SDCTL0/1 register), although interleave mode causes a two bit shift to account for the bank addresses.

The non-multiplexed address pins specify the SDRAM bank to which the current command is targeted. In some density/width configurations, these pins also supply the most significant bits of the row address. The most significant row address bits as well as the bank address bits are not sampled when the column addresses are being driven, and therefore do not need to be multiplexed. These address bits are muxed directly with the external address bus and do not go through the row/column Address Multiplexer seen in Figure 1. These address bits are used differently when the SDRAMC is configured for either linear addressing mode or bank-interleaved addressing mode. The Table 4 on page 9 illustrates the muxing of these address signals.

Table 4. Non-Multiplexed Address Bus

Bank Address Mode	Internal AHB Address Name	i.MX Address Pin Name
Bank Interleaved Address Mode (IAM = 1)	ARM_A9	A16
	ARM_A10	A17
	ARM_A11	A18
	ARM_A12	A19
Linear, Non-Bank Interleaved Address Mode (IAM = 0)	ARM_A21	A11
	ARM_A22	A12
	ARM_A23	A13
	ARM_A24	A14
	ARM_A25	A15

How the i.MX internal ARM AHB address bus is multiplexed with the SDRAMC multiplexed address bits is determined by the row and COL bit settings in the SDCTL0 and SDCTL1 registers. The SDRAM memory data sheet will provide the number of row and column address bits and these values must then be programmed into the row and COL bits of SDCTL0 or SDCTL1. These values, in conjugation with the data bus width, help determine the address folding point, or the point by which the column address bits end and the row (or BANK) address bits begin.

The examples in the following sections should help users better understand these concepts. Each example assumes the use of the SDCTL0 register and provides parameters that users can implement in their system for a variety of memory configurations. These examples can be divided into two main categories, one for interfacing to x32 memories, and the other for interfacing to x16 memories. Each example illustrates to the user how the i.MX SDRAM controller address signals are multiplexed to the external address bus and then how to interface these address signals to the SDRAM memory's address bus. These examples also provide a figure that illustrates the connection for all the address, data, and control signals from the i.MX to the SDRAM memory.

Examples of x16 and x32 data bus sizes are provided to assist the system designer's flexibility in choosing between the two data bus sizes. In terms of system cost, x32 devices are generally slightly more expensive than x16 devices, and in circumstances where x32 devices are not available in the desired memory density, using two x16 devices to form a x32 data bus is an option but will double the cost and draw more power as two devices and their I/Os are now being driven. However, a x32 data bus will have improved performance over that of a x16 data bus as two fetches will need to be made on a x16 data bus per each ARM 32-bit instruction, so the system designer must weigh the additional system cost and power with the increase in performance.

2.2.1 Example 1: 4Mx16x2 (128 Mbit) SDRAM Configuration, Linear Bank Addressing

This example shows how to interface the i.MX to a pair of SDRAM memory device configured as 4Mx16x2 using linear bank addressing. This configuration allows two x16 SDRAM memories to be

configured as one x32 SDRAM memory. The effective memory density of this configuration is 16 MByte or 128 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 8 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^8 x 32, which yields 8192 bits or 1024 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 5 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 5. 4Mx16x2 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	8	COL = 00
Data size	32	DSIZ = 1x
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Linear bank addressing	IAM = 0

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 6 illustrates the address translation steps.

Table 6. 4Mx16x2 IAM=0 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	BA1	BA0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A23	ARM_A22	ARM_A21	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A23	ARM_A22	ARM_A21	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1								
i.MX External Address Signals	A13	A12	A11	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2								
SDRAM Address Signals	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0								

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

The Figure 5 illustrates the interface between the i.MX and the SDRAM memory for 4Mx16x2 (128 Mbit) SDRAM configuration, linear bank addressing.

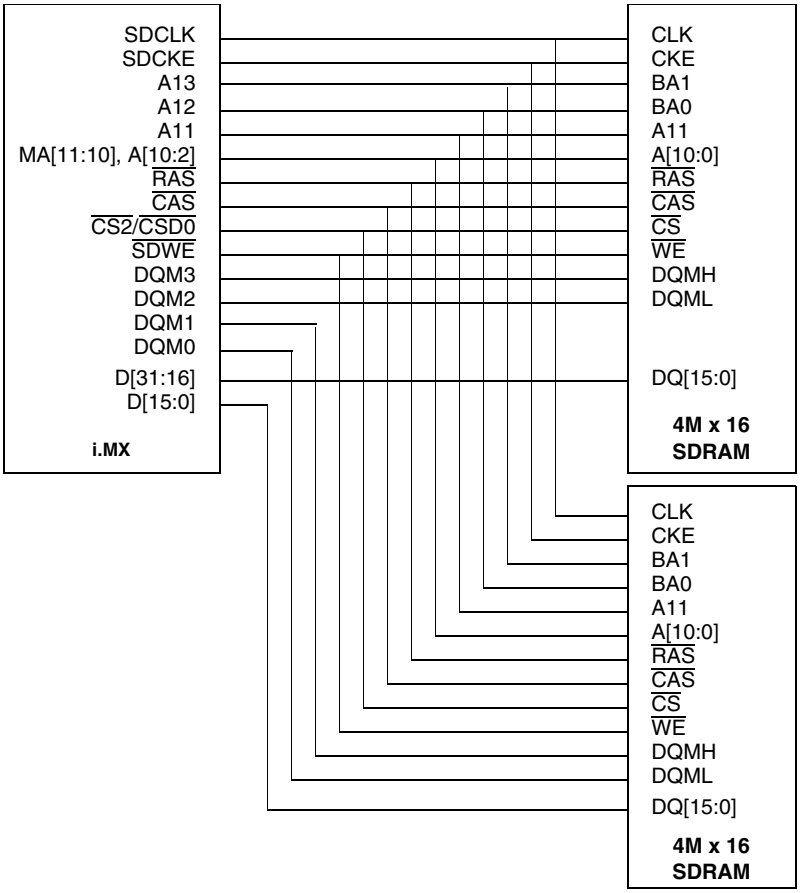

Figure 5. Dual 64 Mbit (4M x 16 x 2) Connection Diagram (IAM = 0)

2.2.2 Example 2: 4Mx16x2 (128 Mbit) SDRAM Configuration, Interleaved Bank Addressing

This example shows how to interface the i.MX to a pair of SDRAM memory device configured as 4Mx16x2 using interleaved bank addressing. This configuration allows two x16 SDRAM memories to be configured as one x32 SDRAM memory. The effective memory density of this configuration is 16 MByte or 128 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 8 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^8 x 32, which yields 8192 bits or 1024 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 7 on page 12 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 7. 4Mx16x2 SDRAM Interleaved Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	8	COL = 00
Data size	32	DSIZ = 1x
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Interleaved bank addressing	IAM = 1

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 8 illustrates the address translation steps.

Table 8. 4Mx16x2 IAM=1 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	BA1	BA0	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A23	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A11	ARM_A10	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A23	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A11	ARM_A10								
i.MX External Address Signals	A13	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A18	A17								
SDRAM Address Signals	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0								

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Figure 6 on page 13 illustrates the interface between the i.MX and the SDRAM memory for 4Mx16x2 (128 Mbit) SDRAM configuration, interleaved bank addressing.

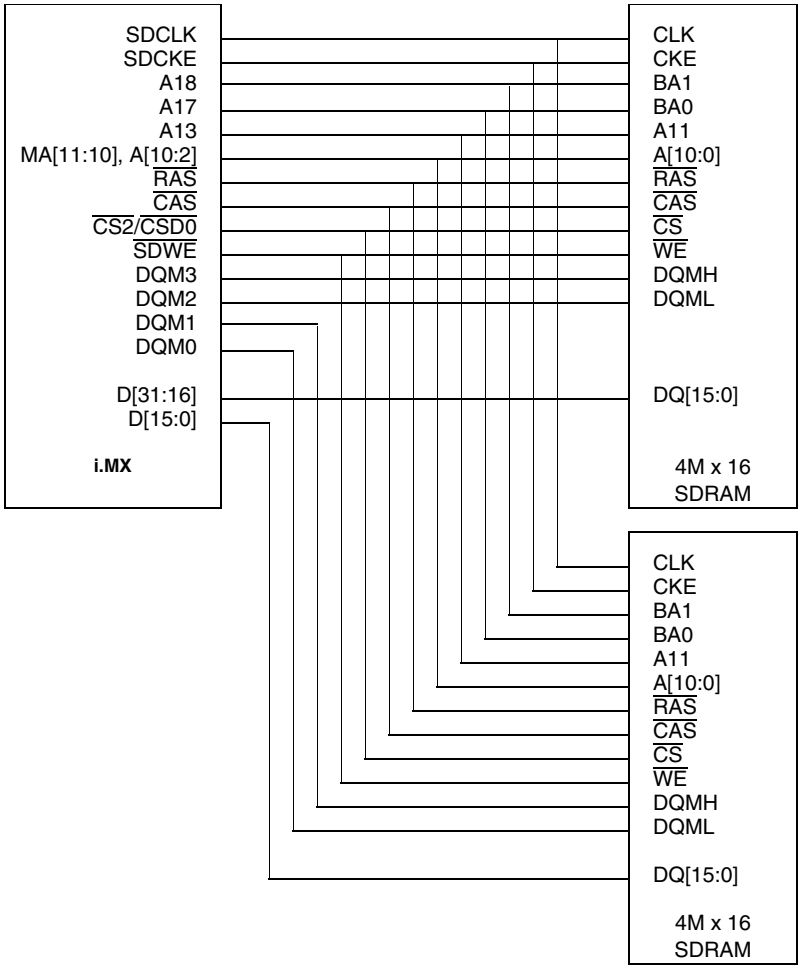

Figure 6. Dual 64 Mbit (4M x 16 x 2) Connection Diagram (IAM = 1)

2.2.3 Example 3: 8Mx16x2 (256 Mbit) SDRAM Configuration, Linear Bank Addressing

This example shows how to interface the i.MX to a pair of SDRAM memory device configured as 8Mx16x2 using linear bank addressing. This configuration allows two x16 SDRAM memories to be configured as one x32 SDRAM memory. The effective memory density of this configuration is 32 MByte or 256 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 9 on page 14 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 9. 8Mx16x2 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	9	COL = 01
Data size	32	DSIZ = 1x
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Linear bank addressing	IAM = 0

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 10 illustrates the address translation steps.

Table 10. 8Mx16x2 IAM=0 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	BA1	BA0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	C8	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A23	ARM_A22	ARM_A21	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A24	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1										
i.MX External Address Signals	A14	A13	A12	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2										
SDRAM Address Signals	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0										

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Figure 7 on page 15 illustrates the interface between the i.MX and the SDRAM memory for 8Mx16x2 (256 Mbit) SDRAM configuration, linear bank addressing.

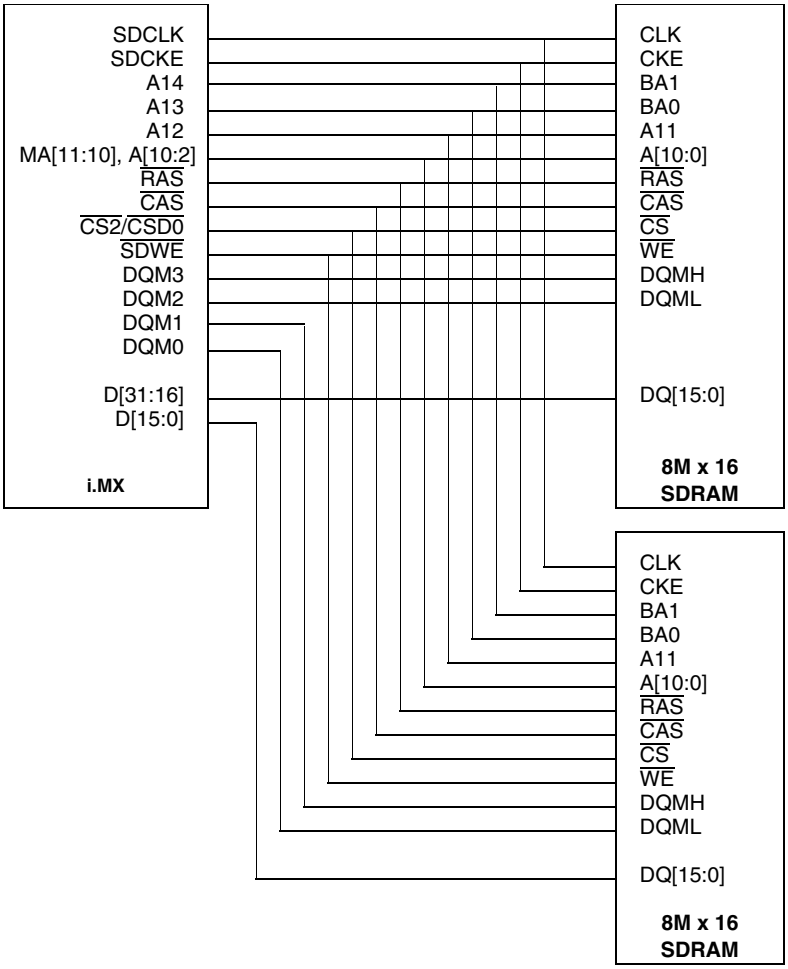

Figure 7. Dual 128 Mbit (8M x 16 x 2) Connection Diagram (IAM = 0)

2.2.4 Example 4: 8Mx16x2 (256 Mbit) SDRAM Configuration, Interleaved Bank Addressing

This example shows how to interface the i.MX to a pair of SDRAM memory device configured as 8Mx16x2 using interleaved bank addressing. This configuration allows two x16 SDRAM memories to be configured as one x32 SDRAM memory. The effective memory density of this configuration is 32 MByte or 256 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 11 on page 16 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 11. 8Mx16x2 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	9	COL = 01
Data size	32	DSIZ = 1x
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Interleaved bank addressing	IAM = 1

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 12 illustrates the address translation steps.

Table 12. 8Mx16x2 IAM=1 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	BA1	BA0	C8	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A24	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A12	ARM_A11	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A24	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	BA1	BA0									
i.MX External Address Signals	A14	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A19	A18									
SDRAM Address Signals	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0									

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Table 8 on page 17 illustrates the interface between the i.MX and the SDRAM memory for 8Mx16x2 (256 Mbit) SDRAM configuration, interleaved bank addressing.

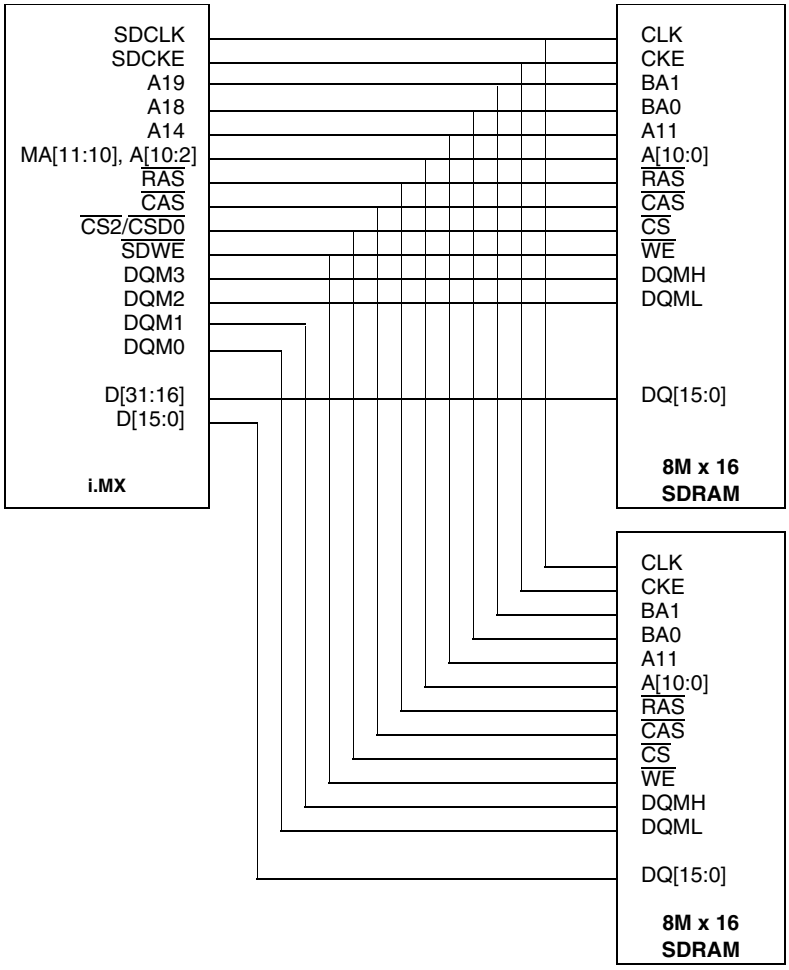

Figure 8. Dual 128 Mbit (8M x 16 x 2) Connection Diagram (IAM = 1)

2.2.5 Example 5: 16Mx16x2 (512 Mbit) SDRAM Configuration, Linear Bank Addressing

This example shows how to interface the i.MX to a pair of SDRAM memory device configured as 16Mx16x2 using linear bank addressing. This configuration allows two x16 SDRAM memories to be configured as one x32 SDRAM memory. The effective memory density of this configuration is 64 MByte or 512 Mbit. The JEDEC standard for this SDRAM memory requires 13 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{13} or 8192 rows to be refreshed every 64 ms. Table 13 on page 18 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 13. 16Mx16x2 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	13	ROW = 10
COLUMN address bits	9	COL = 01
Data size	32	DSIZ = 1x
Refresh rate	8192 rows/64 ms	SREFR = 11
Bank address mode	Linear bank addressing	IAM = 0

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 14 illustrates the address translation steps.

Table 14. 16Mx16x2 IAM=0 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A25	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	BA1	BA0	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	C8	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A25	ARM_A24	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A25	ARM_A24	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1										
i.MX External Address Signals	A15	A14	A13	A12	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2										
SDRAM Address Signals	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0										

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Figure 9 on page 19 illustrates the interface between the i.MX and the SDRAM memory for 16Mx16x2 (512 Mbit) SDRAM configuration, linear bank addressing.

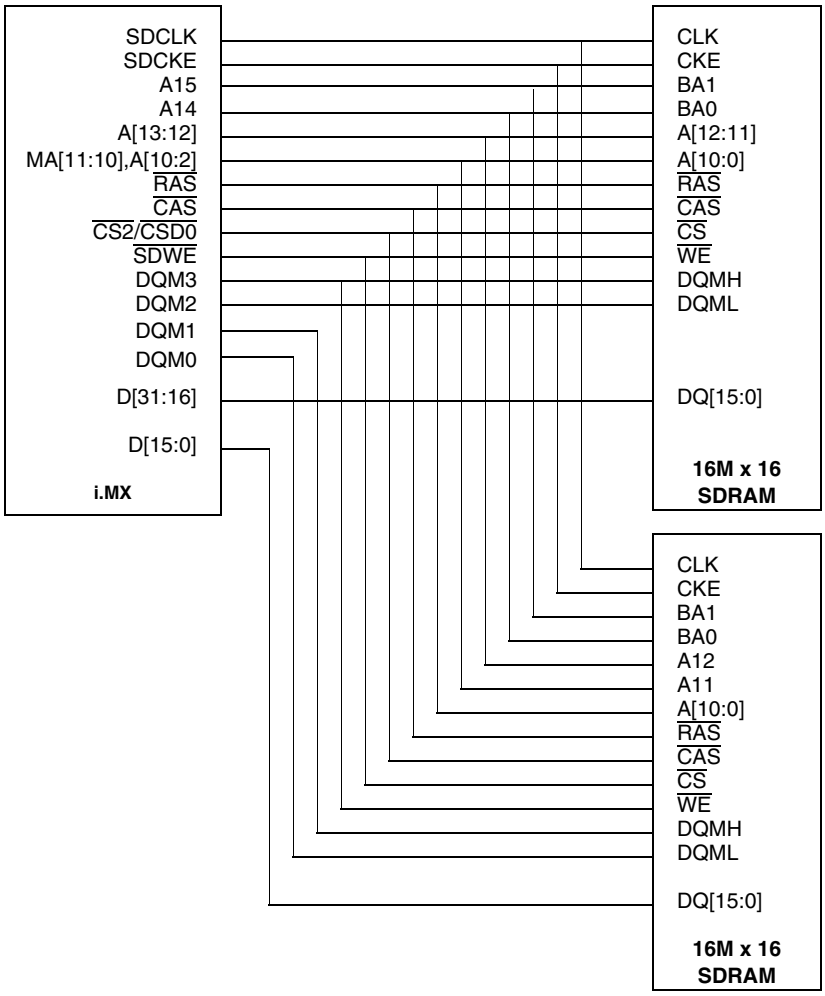

Figure 9. Dual 256 Mbit (16M x 16 x 2) Connection Diagram (IAM = 0)

2.2.6 Example 6: 16Mx16x2 (512 Mbit) SDRAM Configuration, Interleaved Bank Addressing

This example shows how to interface the i.MX to a pair of SDRAM memory device configured as 16Mx16x2 using interleaved bank addressing. This configuration allows two x16 SDRAM memories to be configured as one x32 SDRAM memory. The effective memory density of this configuration is 64 MByte or 512 Mbit. The JEDEC standard for this SDRAM memory requires 13 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{13} or 8192 rows to be refreshed every 64 ms. Table 15 on page 20 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 15. 16Mx16x2 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	13	ROW = 10
COLUMN address bits	9	COL = 01
Data size	32	DSIZ = 1x
Refresh rate	8192 rows/64 ms	SREFR = 11
Bank address mode	Interleaved bank addressing	IAM = 1

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 16 illustrates the address translation steps.

Table 16. 16Mx16x2 IAM=1 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A25	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	BA1	BA0	C8	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A25	ARM_A24	MA11	M110	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A12	ARM_A11	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A25	ARM_A24	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	BA1	BA0										
i.MX External Address Signals	A15	A14	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A19	A18										
SDRAM Address Signals	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0										

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM Interface

Figure 10 on page 21 illustrates the interface between the i.MX and the SDRAM memory for 16Mx16x2 (512 Mbit) SDRAM configuration, interleaved bank addressing.

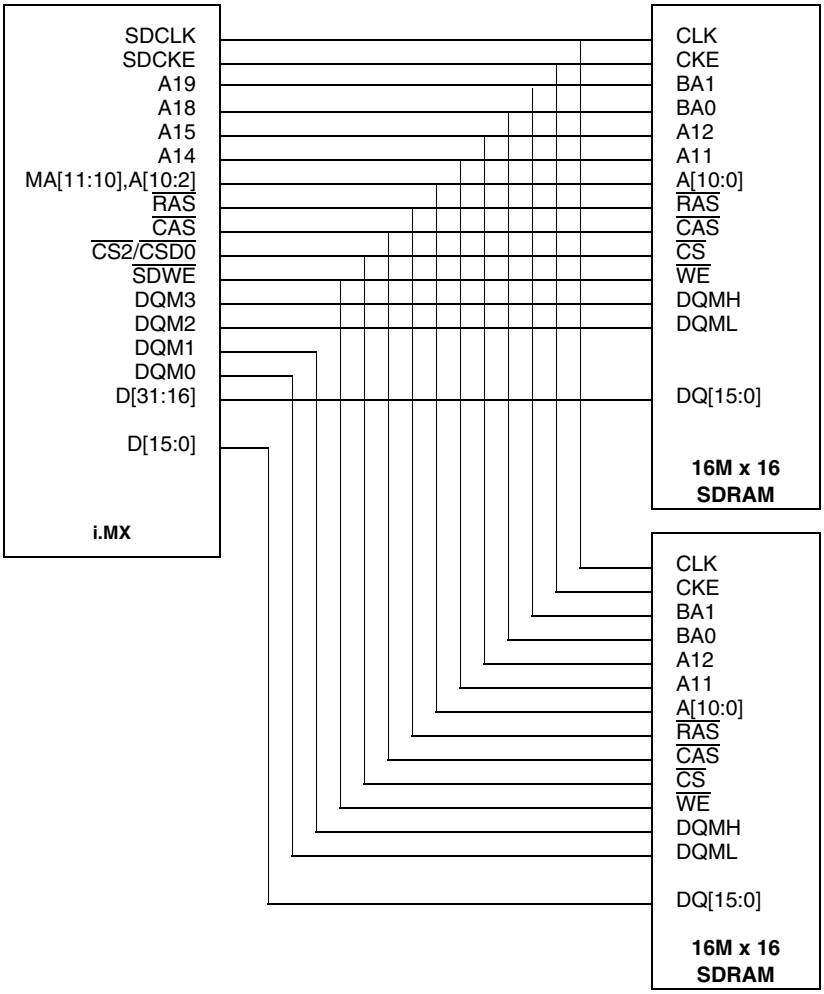

Figure 10. Dual 256 Mbit (16M x 16 x 2) Connection Diagram (IAM = 1)

2.2.7 Example 7: 2Mx32 (64 Mbit) SDRAM Configuration, Linear Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 2Mx32 using linear bank addressing. The effective memory density of this configuration is 8 MByte or 64 Mbit. The JEDEC standard for this SDRAM memory requires 11 row address bits and 8 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^8 x 32, which yields 8192 bits or 1024 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 17 on page 22 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 17. 2Mx32 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	11	ROW = 00
COLUMN address bits	8	COL = 00
Data size	32	DSIZ = 1x
Refresh rate	2048 rows/64 ms	SREFR = 01
Bank address mode	Linear bank addressing	IAM = 0

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 18 illustrates the address translation steps.

Table 18. 2Mx32 IAM=0 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	BA1	BA0	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A22	ARM_A21	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A22	ARM_A21	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1								
i.MX External Address Signals	A12	A11	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2								
SDRAM Address Signals	BA1	BA0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0								

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Figure 11 on page 23 illustrates the interface between the i.MX and the SDRAM memory for 2Mx32 (64 Mbit) SDRAM configuration, linear bank addressing.

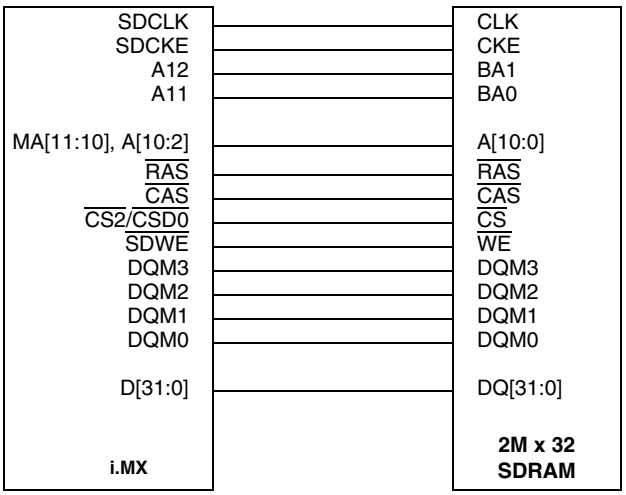

Figure 11. Single 64 Mbit (2M x 32) Connection Diagram (IAM = 0)

2.2.8 Example 8: 2Mx32 (64 Mbit) SDRAM Configuration, Interleaved Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 2Mx32 using interleaved bank addressing. The effective memory density of this configuration is 8 MByte or 64 Mbit. The JEDEC standard for this SDRAM memory requires 11 row address bits and 8 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^8 x 32, which yields 8192 bits or 1024 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 19 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 19. 2Mx32 SDRAM Interleaved Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	11	ROW = 00
COLUMN address bits	8	COL = 00
Data size	32	DSIZ = 1x
Refresh rate	2048 rows/64 ms	SREFR = 01
Bank address mode	Interleaved bank addressing	IAM = 1

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 20 on page 24 illustrates the address translation steps.

Table 20. 2Mx32 IAM=1 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	BA1	BA0	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A11	ARM_A10	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A11	ARM_A10								
i.MX External Address Signals	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A18	A17								
SDRAM Address Signals	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0								

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Figure 12 illustrates the interface between the i.MX and the SDRAM memory for 2Mx32 (64 Mbit) SDRAM configuration, interleaved bank addressing.

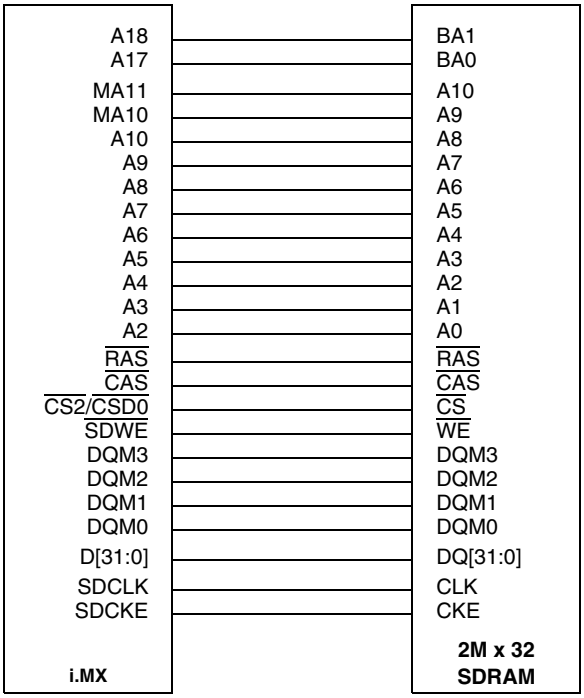

Figure 12. Single 64 Mbit (2M x 32) Connection Diagram (IAM = 1)

2.2.9 Example 9: 4Mx32 (128 Mbit) SDRAM Configuration, Linear Bank Addressing

This example shows how to interface the i.MX to a single SDRAM memory device configured as 4Mx32 using linear bank addressing. The effective memory density of this configuration is 16 MByte or 128 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 8 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^8 x 32, which yields 8192 bits or 1024 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 21 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 21. 4Mx32 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	8	COL = 00
Data size	32	DSIZ = 1x
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Linear bank addressing	IAM = 0

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 22 illustrates the address translation steps.

Table 22. 4Mx32 IAM=0 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	BA1	BA0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A23	ARM_A22	ARM_A21	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A23	ARM_A22	ARM_A21	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1								
i.MX External Address Signals	A13	A12	A11	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2								
SDRAM Address Signals	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0								

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Figure 13 illustrates the interface between the i.MX and the SDRAM memory for 4Mx32 (128 Mbit) SDRAM configuration, linear bank addressing.

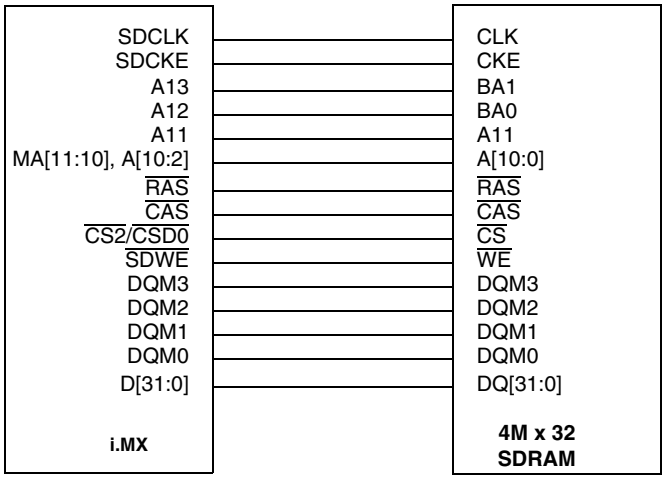

Figure 13. Single 128 Mbit (4M x 32) Connection Diagram (IAM = 0)

2.2.10 Example 10: 4Mx32 (128 Mbit) SDRAM Configuration, Interleaved Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 4Mx32 in interleaved bank addressing. The effective memory density of this configuration is 16 MByte or 128 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 8 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^8 x 32, which yields 8192 bits or 1024 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 23 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 23. 4Mx32 SDRAM Interleaved Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	8	COL = 00
Data size	32	DSIZ = 1x
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Interleaved Bank Addressing	IAM = 1

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 24 illustrates the address translation steps.

Table 24. 4Mx32 IAM=1 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	BA1	BA0	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A23	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A11	ARM_A10	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A23	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A11	ARM_A10								
i.MX External Address Signals	A13	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A18	A17								
SDRAM Address Signals	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0								

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Figure 14 on page 27 illustrates the interface between the i.MX and the SDRAM memory for 4Mx32 (128 Mbit) SDRAM configuration, interleaved bank addressing.

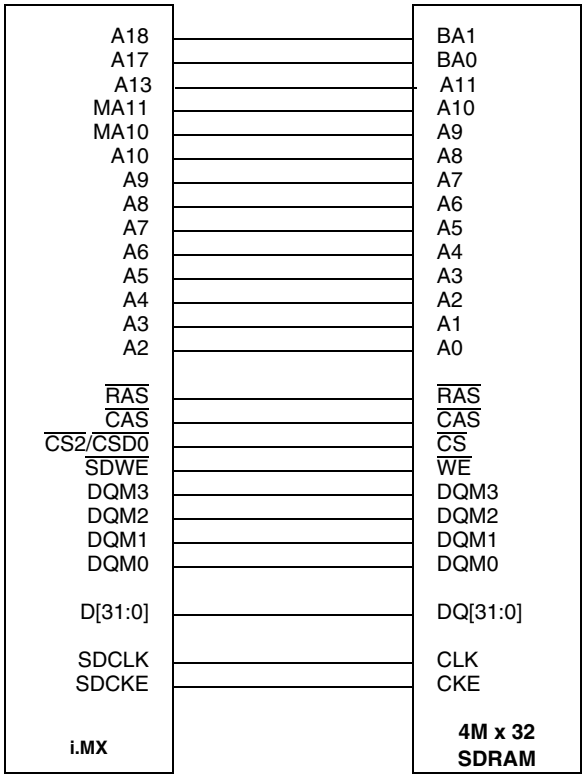

Figure 14. Single 128 Mbit (4M x 32) Connection Diagram (IAM = 1)

2.2.11 Example 11: 8Mx32 (256 Mbit) SDRAM Configuration, Linear Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 8Mx32 using linear bank addressing. The effective memory density of this configuration is 32 MByte or 256 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16,384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 25 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 25. 8Mx32 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	9	COL = 01
Data size	32	DSIZ = 1x
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Linear bank addressing	IAM = 0

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 26 illustrates the address translation steps.

Table 26. 8Mx32 IAM=0 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	BA1	BA0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	C8	C7	C6	C5	C4	C3	C2	C1	C0		
SDRAM Controller Muxing Scheme	ARM_A24	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1		
SDRAM Controller row/column Address Muxing	ARM_A24	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1											
i.MX External Address Signals	A14	A13	A12	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2											
SDRAM Address Signals	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0											

Rotate columns bits around row/column folding point

i.MX to SDRAM interface

Figure 15 illustrates the interface between the i.MX and the SDRAM memory for 8Mx32 (256 Mbit) SDRAM Configuration, Linear Bank Addressing.

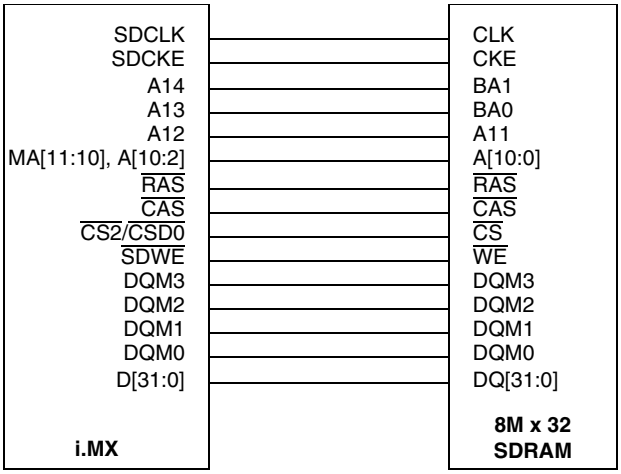

Figure 15. Single 256 Mbit (8M x 32) Connection Diagram (IAM = 0)

2.2.12 Example 12: 8Mx32 (256 Mbit) SDRAM Configuration, Interleaved Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 8Mx32 using interleaved bank addressing. The effective memory density of this configuration is 32 MByte or 256 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 9column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16,384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 27 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 27. 8Mx32 SDRAM Interleaved Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	9	COL = 01
Data size	32	DSIZ = 1x
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Interleaved bank addressing	IAM = 1

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 28 illustrates the address translation steps.

Table 28. 8Mx32 IAM=1 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2
Bank, Row, Column	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	BA1	BA0	C8	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A24	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A12	ARM_A11	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
SDRAM Controller row/column Address Muxing	ARM_A24	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	ARM_A12	ARM_A11									
i.MX External Address Signals	A14	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A19	A18									
SDRAM Address Signals	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0									

Rotate columns bits around row/column folding point

i.MX to SDRAM interface

Figure 16 illustrates the interface between the i.MX and the SDRAM memory for 8Mx32 (256 Mbit) SDRAM Configuration, Interleaved Bank Addressing.

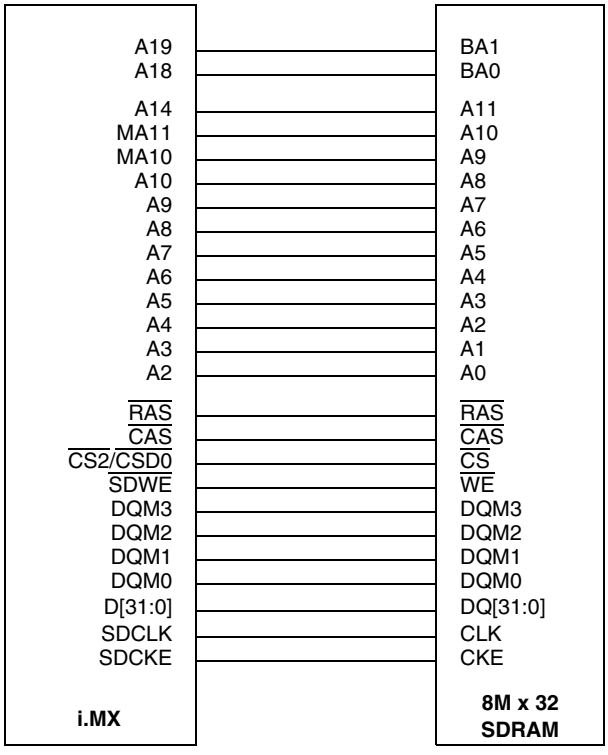

Figure 16. Single 256 Mbit (8M x 32) Connection Diagram (IAM = 1)

2.2.13 Example 13: 8Mx16x1 (128 Mbit) SDRAM Configuration, Linear Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 8Mx16x1 using linear bank addressing. The effective memory density of this configuration is 16 MByte or 128 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 29 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 29. 8Mx16x1 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	9	COL = 01
Data size	16	DSIZ = 00 for D[31:16] or 01 for D[15:0]
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Linear bank addressing	IAM = 0

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 30 illustrates the address translation steps.

Table 30. 8Mx16x1 IAM=0 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2	ARM_A1
Bank, Row, Column	BA1	BA0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	C8	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
SDRAM Controller row/column Address Muxing	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	Rotate columns bits around row/column folding point									
	SDRAM controller address bus to i.MX external address bus translation																							
i.MX External Address Signals	A13	A12	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	i.MX to SDRAM interface									
SDRAM Address Signals	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0										

Figure 17 illustrates the interface between the i.MX and the SDRAM memory for 8Mx16x1 (128 Mbit) SDRAM configuration using linear bank addressing.

NOTE:

The example shown above assumes that the lower data bus is used (D[15:0]). In conjunction with the lower data bus, the data qualifier masks DQM0 and DQM1 are used. If the upper data bus D[31:16] is used, then the data qualifier mask signals DQM2 and DQM3 would be used.

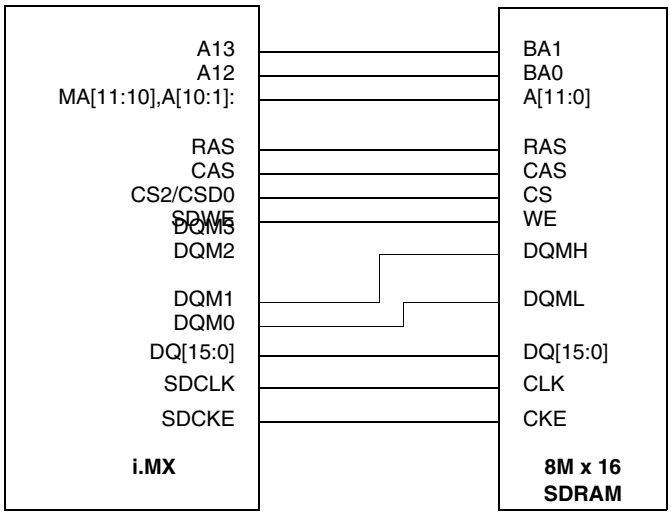

Figure 17. Single 128 Mbit (8M x 16) Connection Diagram (IAM = 0)

2.2.14 Example 14: 8Mx16x1 (128 Mbit) SDRAM Configuration, Interleaved Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 8Mx16x1 using interleaved bank addressing. The effective memory density of this configuration is 16 MByte or 128 Mbit. The JEDEC standard for this SDRAM memory requires 12 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{12} or 4096 rows to be refreshed every 64 ms. Table 31 on page 32 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 31. 8Mx16x1 SDRAM Interleaved Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	12	ROW = 01
COLUMN address bits	9	COL = 01
Data size	16	DSIZ = 00 for D[31:16] or 01 for D[15:0]
Refresh rate	4096 rows/64 ms	SREFR = 10
Bank address mode	Interleaved bank addressing	IAM = 1

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 32 illustrates the address translation steps.

Table 32. 8Mx16x1 IAM=1 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2	ARM_A1
Bank, Row, Column	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	BA1	BA0	C8	C7	C6	C5	C4	C3	C2	C1	C0	
SDRAM Controller Muxing Scheme	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	ARM_A11	ARM_A10	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	
SDRAM Controller row/column Address Muxing	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	ARM_A11	ARM_A10	Rotate columns bits around row/column folding point									
i.MX External Address Signals	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A18	A17	i.MX to SDRAM interface									
SDRAM Address Signals	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0										

SDRAM controller address bus to i.MX external address bus translation

Figure 18 on page 34 illustrates the interface between the i.MX and the SDRAM memory for 8Mx16x1 (128 Mbit) SDRAM configuration using interleaved bank addressing.

NOTE:

The example shown above assumes that the lower data bus is used (D[15:0]). In conjunction with the lower data bus, the data qualifier masks DQM0 and DQM1 are used. If the upper data bus D[31:16] is used, then the data qualifier mask signals DQM2 and DQM3 would be used.

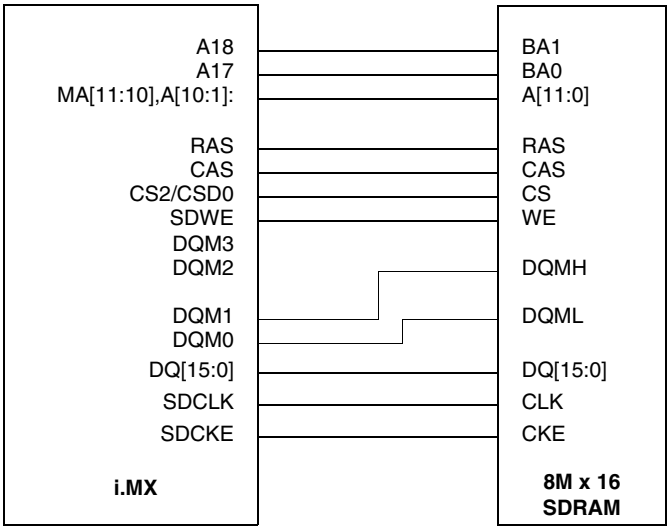

Figure 18. Single 128 Mbit (8M x 16) Connection Diagram (IAM = 1)

2.2.15 Example 15: 16Mx16x1 (256 Mbit) SDRAM Configuration, Linear Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 16Mx16x1 using linear bank addressing. The effective memory density of this configuration is 32 MByte or 256 Mbit. The JEDEC standard for this SDRAM memory requires 13 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{13} or 8192 rows to be refreshed every 64 ms. Table 33 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 33. 16Mx16x1 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	13	ROW = 10
COLUMN address bits	9	COL = 01
Data size	16	DSIZ = 00 for D[31:16] or 01 for D[15:0]
Refresh rate	8192 rows/64 ms	SREFR = 11
Bank address mode	Linear bank addressing	IAM = 0

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 34 on page 35 illustrates the address translation steps.

Table 34. 16Mx16x1 IAM=0 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2	ARM_A1
Bank, Row, Column	BA1	BA0	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	C8	C7	C6	C5	C4	C3	C2	C1	C0
SDRAM Controller Muxing Scheme	ARM_A24	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
SDRAM Controller row/column Address Muxing	ARM_A24	ARM_A23	ARM_A22	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0										
i.MX External Address Signals	A14	A13	A12	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1										
SDRAM Address Signals	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0										

Rotate columns bits around row/column folding point

SDRAM controller address bus to i.MX external address bus translation

i.MX to SDRAM interface

Figure 19 illustrates the interface between the i.MX and the SDRAM memory for 16Mx16x1 (256 Mbit) SDRAM configuration using linear bank addressing.

NOTE:

The example shown above assumes that the lower data bus is used (D[15:0]). In conjunction with the lower data bus, the data qualifier masks DQM0 and DQM1 are used. If the upper data bus D[31:16] is used, then the data qualifier mask signals DQM2 and DQM3 would be used.

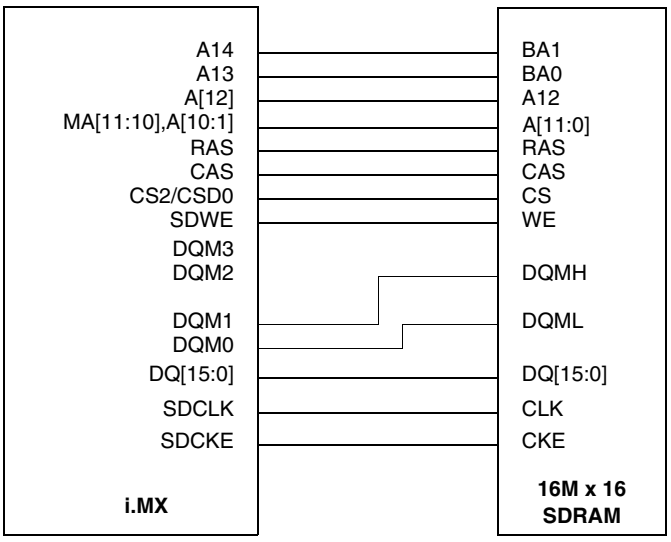

Figure 19. Single 256 Mbit (16M x 16) Connection Diagram (IAM = 0)

2.2.16 Example 16: 16Mx16x1 (256 Mbit) SDRAM Configuration, Interleaved Bank Addressing

This example shows how to interface the i.MX to one SDRAM memory device configured as 16Mx16x1 using interleaved bank addressing. The effective memory density of this configuration is 32 MByte or 256 Mbit. The JEDEC standard for this SDRAM memory requires 13 row address bits and 9 column address bits. The page size is calculated as the number of columns in the SDRAM memory times the number of data bits, or 2^9 x 32, which yields 16384 bits or 2048 bytes. The refresh rate is determined by the calculating the number of rows per bank of the SDRAM memory device that must be refreshed every 64 ms. In this example there are 2^{13} or 8192 rows to be refreshed every 64 ms. Table 35 summarizes the parameters from the SDRAM memory data sheet that must be programmed into the SDCTL0 register. Refer to the SDRAM memory data sheet for specifics on CAS timings, as well as t_{RP}, t_{RCD}, and t_{RC} timings.

Table 35. 16Mx16x1 SDRAM Linear Bank Addressing Parameters

Parameter	Value	SDCTL0 Register Settings
ROW address bits	13	ROW = 10
COLUMN address bits	9	COL = 01
Data size	16	DSIZ = 00 for D[31:16] or 01 for D[15:0]
Refresh rate	8192 rows/64 ms	SREFR = 11
Bank address mode	Interleaved bank addressing	IAM = 1

Once the parameters have been determined, the next step is to determine the address translation from the internal address bus to SDRAM Controller multiplexed address signals. Table 36 illustrates the address translation steps.

Table 36. 16Mx16x1 IAM=1 SDRAM Address Translation Table

i.MX AHB Address Bus (denoted as ARM_Axx)	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9	ARM_A8	ARM_A7	ARM_A6	ARM_A5	ARM_A4	ARM_A3	ARM_A2	ARM_A1
Bank, Row, Column	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	BA1	BA0	C8	C7	C6	C5	C4	C3	C2	C1	C0	
SDRAM Controller Muxing Scheme	ARM_A24	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	ARM_A11	ARM_A10	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	
SDRAM Controller row/column Address Muxing	ARM_A24	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	ARM_A11	ARM_A10	Rotate columns bits around row/column folding point									
																SDRAM controller address bus to i.MX external address bus translation									
i.MX External Address Signals	A14	MA11	MA10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A18	A17	i.MX to SDRAM interface									
SDRAM Address Signals	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0										

Figure 20 illustrates the interface between the i.MX and the SDRAM memory for 16Mx16x1 using interleaved bank addressing.

NOTE:

The example shown above assumes that the lower data bus is used (D[15:0]). In conjunction with the lower data bus, the data qualifier masks DQM0 and DQM1 are used. If the upper data bus D[31:16] is used, then the data qualifier mask signals DQM2 and DQM3 would be used.

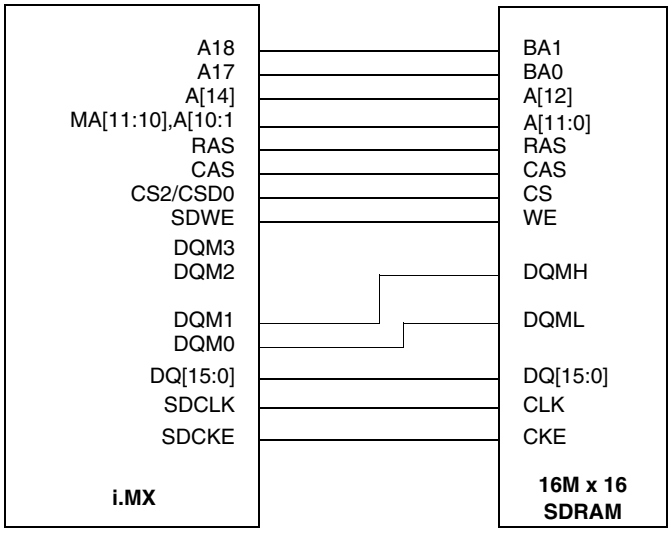

Figure 20. Single 256 Mbit (16M x 16) Connection Diagram (IAM = 1)

2.2.17 Example Configuring the SDCTL0 SRP, SRCD, and SRC Bits

The examples given to this point assume maximum settings for the values SRP, SRCD, and SRC bits in the SDCTL0 register. To increase performance, the system designer may wish to "tweak" these settings to the lowest possible. To do so requires using the timing requirements in the SDRAM data sheet.

For example, take the Micron 256Mb SDRAM data sheet and refer to the electrical characteristics given for the "-7E" option. Also, assume that the system speed of the MC9328MX1 (which is the same as the SDRAM SDCLK) is 96MHz. For the SRP, which is the timing for the ROW precharge delay, the Micron data sheet states this as t_{RP} = 15ns. So the minimum value for SRP is 96MHz x 15ns = 1.44 clocks, which rounding up to the nearest integer, equals 2 clocks.

For the SRCD, which is the ROW to COL delay, the Micron data sheet states this as t_{RCD} = 15ns. So the minimum value for SRCD is 96MHz x 15ns = 1.44 clocks, which rounding up to the nearest integer, equals 2 clocks.

For the SRC, which is the SDRAM ROW cycle delay or the time between a refresh and subsequent refresh or read/write access, the Micron data sheet states this as t_{RFC} = 66ns. So the minimum value for SRC is 96MHz x 66ns = 6.336clocks, which rounding up to the nearest integer, equals 7 clocks.

2.3 SDRAM Initialization and Operation

When the SDRAM is first powered on, it must follow a defined initialization sequence. First, power must be supplied to the SDRAM, followed by starting the SDCLK clock signal. Then stable power, clock, and NOP conditions must be maintained for 200us. The i.MX SDRAM controller ensures this part of the power up sequence, however, it is left up to the user to perform the following initialization sequences.

After proper power up, a PRECHARGE ALL command must be sent, followed by issuing 8 or more AUTO REFRESH commands. Once the AUTO REFRESH cycles are complete, a MODE REGISTER SET command must be sent to initialize the SDRAM memory's mode register. After the mode register has been initialize, the SDRAM memory is ready for normal operation.

The following is an example of an initialization sequence for an SDRAM configured as 6Mx16x2 in linear bank addressing mode. Code Example 1 provides an example following the ARM AXD debugger command format and assumes a CAS latency of 3. This exapmle can easily be translated into ARM assembly code or C code.

Code Example 1. SDRAM Initialization, 16Mx16x2, Linear Bank Addressing (ARM AXD Debugger Format)

```
comment Init SDRAM 16Mx16x2 IAM0, CS2, CAS3
comment ### Set Precharge Command
setmem 0x221000 0x92120300, 32
comment ### Issue Precharge all Command (assert SDRAM memory A10)
mem    0x08200000, +4 32
comment ### Set AutoRefresh Command
setmem 0x221000 0xA2120300, 32
comment ### Issue AutoRefresh Command
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
comment ### Set Mode Register
setmem 0x221000 0xB2120300, 32
comment ### Issue Mode Register Command, Burst length = 8, CAS = 3
mem    0x08119800, +4 32
comment ### Set to Normal Mode,row:13,col:9,IAM:0,SREFR:8192,CAS:3
setmem 0x221000 0x8212C300, 32
```

2.3.1 SDRAM Mode Register Programming

The mode register of the SDRAM memory is used to set its operating characteristics such as CAS latency, burst length, burst mode, and write data length. The settings depend on system characteristics including the operating frequency, memory device type, burst buffer/cache line length, and bus width. Operating characteristics vary by device type, so the data sheet must be consulted to determine the actual value to be written. For the i.MX, the SDRAM memory burst length should be set to 8 to match the i.MX cache line fill, the burst mode should be set for sequential, and the write burst mode should be set to single location access.

The data written to the SDRAM memory mode register is transferred over the SDRAM address bus. Thus the i.MX SDRAM controller must be in the Set Mode Register mode of operation. This is accomplished by simply writing the value 011 to the SMODE bits of the SDCTL0/1 register. Once the SDRAM controller is in the Set Mode Register mode, any access following will generate the Set Mode Register command on the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$ lines and the value given on the address bus will be written to the SDRAM memory mode register, assuming the SDRAM is idle. For different SDRAM memory configurations, this address value may differ. Refer to the i.MX for more information on the SDRAM controller modes of operation.

Table 37 on page 39 and Table 38 on page 40 illustrate the position of the mode register bits relative to the SDRAM memory address pins and the i.MX internal address bus. The SDRAM configurations follow the configurations given in this document. Table 37 illustrates this for SDRAM memories configured for a x16 data bus, whereas Table 38 illustrates this for a x32 data bus.

Table 37. SDRAM Mode Register Bits Relative to the i.MX Internal Address Bus for x16 Configurations

		i.MX Internal Address Bus (denoted as ARM_Axx)																							
Memory Configuration	**IAM**	**ARM_A31**	**ARM_A30**	**ARM_A29**	**ARM_A28**	**ARM_A27**	**ARM_A26**	**ARM_A25**	**ARM_A24**	**ARM_A23**	**ARM_A22**	**ARM_A21**	**ARM_A20**	**ARM_A19**	**ARM_A18**	**ARM_A17**	**ARM_A16**	**ARM_A15**	**ARM_A14**	**ARM_A13**	**ARM_A12**	**ARM_A11**	**ARM_A10**	**ARM_A9**
8Mx16x1	0	0	0	0	0	x	x	0	0	BA1[M13]	BA0[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	0
16MByte	1	0	0	0	0	x	x	0	0	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	BA1[M13]	BA0[M12]	0
16Mx16x1	0	0	0	0	0	x	x	0	BA1[M14]	BA0[M13]	A12[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	0
32MByte	1	0	0	0	0	x	x	0	A12[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	BA1[M14]	BA0[M13]	0
1Mx16x1	0	0	0	0	0	x	x	0	0	0	0	BA[M11]	NC	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]
		i.MX CSDx Base						SDRAM Memory Address and Mode Register Bits																

Table 38. SDRAM Mode Register Bits Relative to the i.MX Internal Address Bus for x32 Configurations

		i.MX Internal Address Bus (denoted as ARM_Axx)																						
Memory Configuration	**IAM**	**ARM_A31**	**ARM_A30**	**ARM_A29**	**ARM_A28**	**ARM_A27**	**ARM_A26**	**ARM_A25**	**ARM_A24**	**ARM_A23**	**ARM_A22**	**ARM_A21**	**ARM_A20**	**ARM_A19**	**ARM_A18**	**ARM_A17**	**ARM_A16**	**ARM_A15**	**ARM_A14**	**ARM_A13**	**ARM_A12**	**ARM_A11**	**ARM_A10**	**ARM_A9**
4Mx16x2	0	0	0	0	0	x	x	0	0	BA1[M13]	BA0[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	0
16MByte	1	0	0	0	0	x	x	0	0	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	BA1[M13]	BA0[M12]	0
8Mx16x2	0	0	0	0	0	x	x	0	BA1[M13]	BA0[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	0	0
32MByte	1	0	0	0	0	x	x	0	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	BA1[M13]	BA0[M12]	0	0
16Mx16x2	0	0	0	0	0	x	x	BA1[M14]	BA0[M13]	A12[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	0	0
64MByte	1	0	0	0	0	x	x	A12[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	BA1[M14]	BA0[M13]	0	0
2Mx32x1	0	0	0	0	0	x	x	0	0	0	BA1[M12]	BA0[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	0
8MByte	1	0	0	0	0	x	x	0	0	0	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	BA1[M12]	BA0[M11]	0
4Mx32x1	0	0	0	0	0	x	x	0	0	BA1[M13]	BA0[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	0
16MByte	1	0	0	0	0	x	x	0	0	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	BA1[M13]	BA0[M12]	0
8Mx32x1	0	0	0	0	0	x	x	0	BA1[M13]	BA0[M12]	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	0	0
32MByte	1	0	0	0	0	x	x	0	A11[M11]	A10[M10]	A9[M9]	A8[M8]	A7[M7]	A6[M6]	A5[M5]	A4[M4]	A3[M3]	A2[M2]	A1[M1]	A0[M0]	BA1[M13]	BA0[M12]	0	0
		i.MX CSDx Base						**SDRAM Memory Address and Mode Register Bits**																

To illustrate how to use these tables, take for example the initialization example given above for the 16Mx16x2 SDRAM configuration in linear bank addressing mode. Using the CAS 3 example and placing the other values in the mode register yields the SDRAM mode register and values shown in Table 39.

Table 39. 16M x 16 SDRAM Mode Register

SDRAM Address	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register Bit	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
Content	Reserved			WB	Reserved		CAS latency			BT	Burst length		
Values	0	0	0	1	0	0	0	1	1	0	0	1	1

Placing these values into Table 39 and using the $\overline{CS2}$ address space yields the results in Table 40.

Table 40. 16Mx16x2 SDRAM Mode Register Example

		i.MX Internal Address Bus (denoted as ARM_Axx)																						
Memory Configuration	IAM	ARM_A31	ARM_A30	ARM_A29	ARM_A28	ARM_A27	ARM_A26	ARM_A25	ARM_A24	ARM_A23	ARM_A22	ARM_A21	ARM_A20	ARM_A19	ARM_A18	ARM_A17	ARM_A16	ARM_A15	ARM_A14	ARM_A13	ARM_A12	ARM_A11	ARM_A10	ARM_A9
16Mx16x2	0	0	0	0	0	1	0	BA1[0]	BA0[0]	A12[0]	A11[0]	A10[0]	A9[1]	A8[0]	A7[0]	A6[0]	A5[1]	A4[1]	A3[0]	A2[0]	A1[1]	A0[1]	0	0

Thus the address (in hexadecimal) generated by the Table 40 yields: 0x08119800, which matches the address value for programming the mode register given in Code Example 1. Note that in these tables, the bank addresses are shown with corresponding mode register bits. Not all SDRAMs utilize these bits, but they are shown for future expansion and are often use for low-power SDRAMs when distinguishing between the mode register and extended mode register. This is explained more in the next section.

2.3.2 Extended Mode Registers in Low-Power SDRAMs

The previous section touch upon the SDRAM bank addresses mapping to mode register bits for low-power SDRAM devices. These devices usually incorporate two mode registers, one called the “mode register” and the other called the “extended mode register”. The mode register was describe in detail in the previous section. The extended mode register controls the functions beyond those controlled by the mode register. These additional functions usually control the Temperature Compensated Self Refresh (TCSR) and the Partial Array Self Refresh (PASR). TCSR controls the refresh interval during self refresh mode according tot he case temperature of the low-power SDRAM, where PASR allows the user to shut off refresh cycles to certain banks during self refresh for further power savings, however data in those banks will be lost. Programming the mode register and extended mode register is distinguished by writing to the bank address bits of the SDRAM device.

Take for example the Micron 128Mb Mobile SDRAM. Below are the two mode registers for the Mobile SDRAM, the first represents the mode register, the second represents the extended mode register.

Table 41. Micron 128Mb: x16 Mobile SDRAM Mode Register

SDRAM Address Bus	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
Bit Functions	0	0	reserved		WB	Op Mode		CAS Latency			BT	Burst Length		

Table 42. Micron 128Mb: x16 Mobile SDRAM Extended Mode Register

SDRAM Address Bus	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Extended Mode Register	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
Bit Functions	1	0	All must be set to 0							TCSR		PASR		

The desired settings can be applied to these registers via the SDRAM address bus following the example in Section 2.3.1, “SDRAM Mode Register Programming.” In this case, once the SMODE bits of SDCTL0 have been set to 001, two SDRAM memory access must be performed. The first access should place the mode register value onto the address bus and the second access should place the extended mode register value onto the address bus. Below is an example of setting the mode register and the extended mode register for an 8Mx16x2 configuration given in an initialization file written for the ARM AXD debugger. The example provides several TCSR and PASR combinations to choose from. Refer to Table 38 on page 40 for the address bit settings of the 8Mx16x2 IAM=0 SDRAM relative to the i.MX internal address bus. For more information on the mode register and extended mode register, refer to Micron’s Mobile SDRAM data sheet.

Code Example 2. Micron 8Mx16 Mobile SDRAM ARM AXD Initialization Example

```
comment ### SDRAM Init, linear-bank mode, IAM=0
comment ### assuming 8Mx16x2 configuration
comment ### Set Precharge Command
setmem 0x221000 0x91120300, 32
comment ### Issue Precharge all Command (assert SDRAM memory A10)
mem    0x08200000, +4 32
comment ### Set AutoRefresh Command
setmem 0x221000 0xA1120300, 32
comment ### Issue AutoRefresh Command
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
mem    0x08000000, +4 32
comment ### Set Mode Register
setmem 0x221000 0xB1120300, 32
comment ### Issue "Regular" Mode Register Command, Burst length = 8, CAS =3
mem    0x08119800, +4 32
comment ### Issue "Extended" Mode Register Command
comment ### TCSR '11' = 85, PASR '001' = 2 BANKS
comment mem    0x0900C800, +4 32
comment ### TCSR '11' = 85, PASR '000' = 4 BANKS
comment mem    0x0900C000, +4 32
comment ### TCSR '11' = 85, PASR '010' = 1 BANK
comment mem    0x0900D000, +4 32
comment ### TCSR '10' = 15, PASR '010' = 1 BANK
comment mem    0x09009000, +4 32
comment ### TCSR '10' = 15, PASR '000' = 4 BANK
comment mem    0x09008000, +4 32
comment ### TCSR '00' = 70, PASR '000' = 4 BANK
mem    0x09000000, +4 32
comment ### TCSR '01' = 45, PASR '000' = 4 BANK
comment mem    0x09004000, +4 32
comment ### Set to Normal Mode,row:12,col:9,IAM:0,SREFR:4096,CAS:3
setmem 0x221000 0x81128300, 32
```

3 Reference Documents

The following documents are helpful when used in conjunction with this application note.

MC9328MX1 Reference Manual (order number MC9328MX1RM)

MC9328MXL Reference Manual (order number MC9328MXLRM)

MC9328MXS Reference Manual (order number MC9328MXSRM)

Freescale documents are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered.

4 Document Revision History

Table 43 summarizes revisions to this document since the previous release (Rev. 4).

Table 43. Revision History

Location	Revision
Table 15 on page 20”	Changed ROW address Value from 12 to 13, and SDCTL0 Register Setting from ROW=01 to ROW=10.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: AN2478
Rev. 5
02/2007

freescale™ semiconductor