

Potential Signal Race in the CMOS Sensor Interface Module

MC9328MX1, MC9328MXL, and MC9328MXS

by: Cliff Wong

1 Abstract

This document describes the potential signal race situation in the CMOS Sensor Interface (CSI) module of the i.MX processors. The signal race occurs between the HSYNC signal and the PIXCLK signal when there is poor routing in the PCB layout. When the signal race situation is triggered, an invalid pixel clock edge goes into the internal logic and results in dummy pixel data being received by the RxFIFO. The side effect is loss of frame sync and mis-alignment of lines.

The situation only occurs in gated-clock mode with the sensor running a continuous pixel clock.

This document applies to the following i.MX devices, collectively called i.MX throughout:

- MC9328MX1
- MC9328MXL
- MC9328MXS

Contents

1 Abstract	1
2 Normal Operation	2
3 Potential Race Situation	2
4 How to Avoid Race Situation	3
5 Revision History	3



2 Normal Operation

Figure 1 illustrates the normal operation of gated-clock mode.

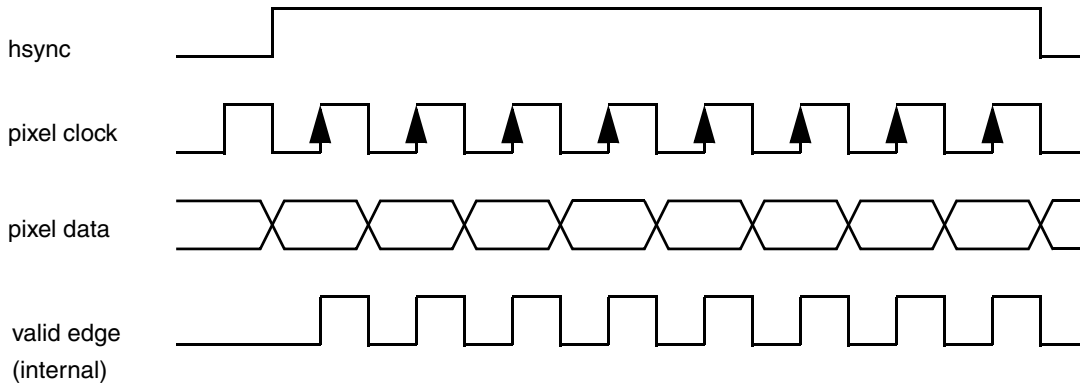


Figure 1. Correct Valid Edge Generation

The pixel clock from the i.MX processor’s CSI module is continuous. The pixel clock signal is synchronized with the HSYNC signal. HSYNC = 1 indicates the pixel clock is valid. Inside the i.MX processor, these two signals are ANDed to generate valid pixel clock edges. Data is latched into the Rx FIFO at the valid pixel clock edges.

3 Potential Race Situation

Figure 2 illustrates the scenario that causes the race situation.

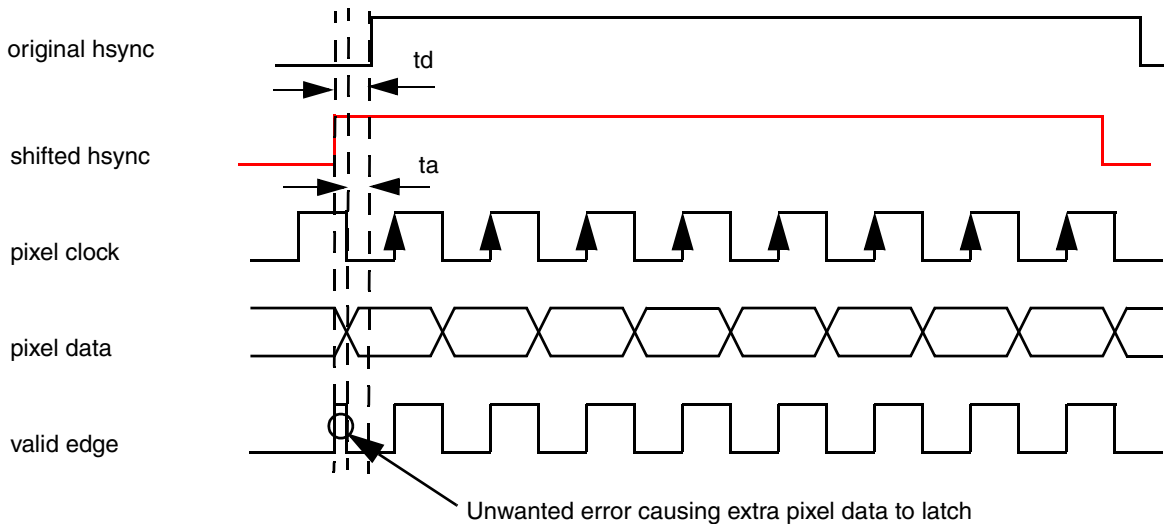


Figure 2. Incorrect Valid Edge Generation

Depending on the PCB design, the HSYNC signal will skew ahead of the PIXCLK signal. If the skew is great enough, for example, a half pixel clock cycle, the HSYNC signal overlaps the previous pixel clock signal. This generates an error to the valid pixel clock signal used by the internal logic to latch data.

If the skew is small, however, the situation will not happen. The maximum amount of drift (t_d) allowed is dependent on the sensor, not the i.MX processor. There are two factors affecting the amount of drift allowed:

- Relative timing position of HSYNC to PIXCLK.
Theoretically there is at most $\frac{1}{2}$ PIXCLK period allowed for the drift.
- Frequency of PIXCLK. Higher frequency results in a smaller margin.

A printed circuit board design in which the routing for the PIXCLK signal is longer than that of the HSYNC signal, allows a delay to be inserted to the PIXCLK signal. Delay in PIXCLK is equivalent to a backward drift in HSYNC and results in the signal race situation.

4 How to Avoid Race Situation

The key to avoid the signal race situation is to ensure that HSYNC never overlaps with the previous pixel clock. Here are suggested solutions:

1. Restrict the routing of PIXCLK not to exceed that of HSYNC.
2. Insert a buffer/inverter to the HSYNC signal when the measured delay on PIXCLK is too long. This compensates for the delay on PIXCLK.
3. Gate PIXCLK with HSYNC. To accomplish, feed PIXCLK and HSYNC to an AND gate located close to the sensor output. The output of the AND gate then feeds the PIXCLK input of the i.MX processor. This inhibits PIXCLK when HSYNC is low and is a more robust solution than either solution 1 or 2. For high data rates, a similar AND gate may be needed in the pixel data path to compensate for the added propagation delay in the PIXCLK path.

5 Revision History

Table 1 details the document revision history.

Table 1. Revision History

Revision Number	Notes
2	Editorial review, clarification to title and text. Applied new Freescale template.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. ARM and the ARM POWERED logo are the registered trademarks of ARM Limited. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2005. All rights reserved.