

## **Freescale Semiconductor**

# Design Concept Expanding Interrupts on the 68302

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Recent integrated processors in the 68000 family add individual interrupt request lines to the processor. For instance, the MC68302 adds seven interrupt lines. However, if more are required, the 68302 can provide up to 19 interrupt lines with no additional glue logic. This is accomplished by using other features of the MC68302 not originally intended to be used as interrupt request lines.

The seven traditional interrupt request sources are the three IRQ lines at interrupt levels 1, 6, and 7, plus four Port B parallel I/O lines with falling-edge interrupt capability. The seven pins are IRQ1\*, IRQ6\*, IRQ7\*, PB8, PB9, PB10, and PB11. These are shown in figure 1.

The first two additional sources the TIN1 and TIN2 pins of Timer 1 and Timer 2. These pins have an ability to perform a capture operation on the timer. A capture operation can generate a timer interrupt on a falling, rising, or any change in the TIN signal. The "capture" interrupt will capture the current timer value into the capture register (which can be disregarded). In any case, the capture operation will be signified in the timer event register (TER). One advantage of using the TIN1 and TIN2 pins is that this interrupt can continue to function even if the timer is being used for another interrupting timer function, so long as the timer clock source is internally generated.

The next source is the DREQ\* pin on the Independent DMA controller (IDMA). If the IDMA is not being used, an interrupt can be generated by a falling edge of the DREQ\* pin, and will be recorded in the IDMA channel status register (CSR). The IDMA is set up to perform a one word move operation, and then to complete with an interrupt to the CPU. The only disadantage to this approach is an additional 12 or so clocks latency before the interrupt request is presented to the core, and 8 clocks of bus bandwidth used.

The next 6 sources are available, if any of the following pins are not needed on a given on-chip serial communications controller (SCC): CD1\*, CTS1\*, CD2\*, CTS2\*, CD3\*, or CTS3\* pins. The CD\* pin is a valid interrupt source if the SCC ENR bit is set, and the receive clock is running. The CTS\* pin is a valid interrupt source if the SCC ENT bit is set, and the transmit

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clock is running. Any change in state of the CD\* or CTS\* pin will generate an interrupt from that particular SCC and be recorded in the SCCE register. The clocks may be generated from the SCC's internal baud rate generator, or brought in externally to the RCLK or TCLK pins. The current state of the CD\* or CTS\* pin may be read in the SCCS register.

The last 3 sources are the RXD1, RXD2, and RXD3 pins. These are available for an interrupt request, if the corresponding receive half of the SCC is not used for a protocol. If the SCC is programmed into HDLC mode, then the RXD pin can be used to sense the "idle" condition of the line. The idle condition is entered if 15 or more ones are sensed on the RXD pin, while the idle condition is exited after a single zero is sensed on the RXD pin. The SCC can be enabled (the ENR bit is set by the user) to provide an interrupt on any change of state of the idle condition as long as the receive SCC clock is running. This is recorded in the SCCE register. Thus, any change of state in RXD will cause an interrupt, as long as it stays high for at least 15 serial clocks. The receiver can be clocked at high speed, to reduce the minimum high-time requirement if that happens to be a system issue.

## 

BASE EQU \$0700000 ; This is the base value programmed into BAR

* Common	ly used Registers and Parameters
BAR EQU	\$0F2 ; Base Address Register
PACNT	EQU BASE+\$081E ; Port A Control Register
PBCNT	EQU BASE+\$0824 ; Port B Control Register
GIMR	EQU BASE+\$0812 ; Global Interrupt Mode Register
IPR EQU	BASE+\$0814 ; Interrupt Pending Register
IMR EQU	BASE+\$0816 ; Interrupt Mask Register
ISR EQU	BASE+\$0818 ; In-Service Register
*Timers	
TMR1	EQU BASE+\$0840 ; Timer 1 Mode Register
TER1 EQU	BASE+\$0849 ; Timer 1 Event Register
TMR2	EQU BASE+\$0850 ; Timer 2 Mode Register
TER2 EQU	BASE+\$0859 ; Timer 2 Event Register
* IDMA	
CMR EQU	BASE+\$0802 ; Channel Status Register
SAPR	EQU BASE+\$0804 ; Source Address Pointer Register
DAPR	EQU BASE+\$0808 ; Destination Address Pointer Register
BCR EQU	BASE+\$080C ; Byte Count Register



FCR EQU	BASE+\$0810	; Function Code Register		
CSR EQU	BASE+\$080E	; Channel Status Register		
* SCC1				
SCON1	EQU	BASE+\$0882 ; SCC1 Configuration Register		
SCM1	EQU	BASE+\$0884 ; SCC1 Mode Register		
SCCE1	EQU	BASE+\$0888 ; SCC1 Event Register		
SCCM1	EQU	BASE+\$088A ; SCC1 Mask Register		
SCCS1	EQU	BASE+\$088C ; SCC1 Status Register		
* SCC2				
SCON2	EQU	BASE+\$0892 ; SCC2 Configuration Register		
SCM2	EQU	BASE+\$0894 ; SCC2 Mode Register		
SCCE2	EQU	BASE+\$0898 ; SCC2 Event Register		
SCCM2	EQU	BASE+\$089A ; SCC2 Mask Register		
SCCS2	EQU	BASE+\$089C ; SCC2 Status Register		
* SCC3				
SCON3	EQU	BASE+\$08A2 ; SCC3 Configuration Register		
SCM3	EQU	BASE+\$08A4 ; SCC3 Mode Register		
SCCE3	EQU	BASE+\$08A8 ; SCC3 Event Register		
SCCM3	EQU	BASE+\$08AA ; SCC3 Mask Register		
SCCS3	EQU	BASE+\$08AC ; SCC3 Status Register		

\*\*\* SCC BD Table Entries \*\*\*

BASE+\$0400	; RX BD 0 in SCC1
BASE+\$0500	; RX BD 0 in SCC2
BASE+\$0600	; RX BD 0 in SCC3
BASE+\$0440	; TX BD 0 in SCC1
BASE+\$0540	; TX BD 0 in SCC2
BASE+\$0640	; TX BD 0 in SCC2
	BASE+\$0500 BASE+\$0600 BASE+\$0440 BASE+\$0540

ORG \$4000 MOVE.W #\$2700,SR ; SR=2700, mask off interrupts

\* Set Base Address = \$700000

\* Now all 68302 on-chip peripherals begin at address \$700xxx

MOVE.W #\$0700,BAR ; BAR=0700

\*\*\* Enable all expanded interrupt request pins instead of parallel I/O \*\*\* \*\*\* This is not required for RXD1, CD1, CTS1, CD3, and CTS3. \*\*\*

MOVE.W #\$2151,PACNT ; RXD2, CD2, CTS2, RXD3, DREQ\* MOVE.W #\$0028,PBCNT ; TIN1, TIN2

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\*\*\* Initial interrupt controller setups \*\*\*
MOVE.W #\$00A0,GIMR ; Normal mode, v7-v5=3
MOVE.W #\$0000,IMR ; Mask off all for now
MOVE.W #\$FFFF,IPR ; Clear IPR

\*\*\* Initialize TIN1 and TIN2 to generate interrupts on any change in \*\*\* \*\*\* the level of these pins. \*\*\*

MOVE.L	<pre>#vector,\$02A4 ; Setup desired Timer 1 interrupt vector</pre>
	; where vector is defined to be an address
	; where the interrupt routine should start
MOVE.B	#\$FF,TER1 ; Clear out event register
ANDI.W	#\$0200,IMR ; Enable Timer 1 interrupts
MOVE.W	#\$08C3,TMR1 ; TIN1 enabled for interrupts
MOVE.L	<pre>#vector,\$0298 ; Setup desired Timer 2 interrupt vector</pre>
MOVE.B	#\$FF,TER2 ; Clear out event register
ANDI.W	#\$0040,IMR ; Enable Timer 2 interrupts
MOVE.W	#\$083C,TMR2 ; TIN2 enabled for interrupts

\*\*\* Initialize DREQ\* to generate an interrupt on a falling edge. \*\*\*

MOVE.L	#\$00700000,SAPR ; Start address is \$700000
MOVE.L	#\$00700000,DAPR ; Destination is \$700000
MOVE.W	#\$0001,BCR ; Only 1 byte is transferred
MOVE.W	#\$0088,FCR ; Function codes initialized to 000.
MOVE.L	#vector, \$02AC ; Setup desired IDMA interrupt vector
MOVE.B	#\$FF,CSR ; Clear out event register
ANDI.W	#\$0800,IMR ; Enable IDMA interupts
MOVE.W	#\$3C31,CMR ; DREQ* falling edge begins transfer

\*\*\* Initialize SCC1 to generate interrupts on any change in CD1\* \*\*\*

	MOVE.L MOVE.W	<pre>#vector,\$02B4 ; Initialize SCC1 interrupt vector #\$0020,SCON1 ; Baud rate generator on SCC1 used</pre>
	MOVE.W	#\$0000,RXBD_01 ; Disable reception via first Rx BD
	MOVE.B	#\$FF,SCCE1 ; Clear out SCC1 event register
	ANDI.B	#\$40,SCCM1 ; Enable CD interrupt
	MOVE.W	#\$0038,SCM1 ; HDLC Mode with receiver enabled
***	Enable SCC1	interrupt on any change in CTS1* ***
	ANDI.B	#\$80,SCCM1 ; Enable CTS interrupt



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; Disable transmission via first Tx MOVE.W #\$0000,TXBD 01 BD ANDI.W #\$0004,SCM1 ; Enable ENT bit of SCC1 \*\*\* Enable SCC1 interrupt on idle status change \*\*\* ; Enable RXD1 interrupt ANDI.B #\$20,SCCM1 ANDI.B #\$2000,IMR ; Enable SCC1 interrupts \*\*\* Initialize SCC2 to generate interrupts on any change in CD2\* \*\*\* MOVE.L #vector,\$02A8 ; Initialize SCC2 interrupt vector ; Baud rate generator on SCC2 used #\$0020,SCON2 MOVE.W MOVE.W #\$0000,RXBD 02 ; Disable reception via first Rx BD MOVE.B #\$FF.SCCE2 ; Clear out SCC2 event register : Enable CD interrupt ANDI.B #\$40,SCCM2 ; HDLC Mode with receiver enabled MOVE.W #\$0038,SCM2 \*\*\* Enable SCC2 interrupt on any change in CTS2\* \*\*\* #\$80,SCCM2 ; Enable CTS interrupt ANDI.B #\$0000,TXBD 02 ; Disable transmission via first Tx MOVE.W BD #\$0004,SCM2 : Enable ENT bit of SCC2 ANDI.W \*\*\* Enable SCC2 interrupt on idle status change \*\*\* #\$20,SCCM2 ; Enable RXD2 interrupt ANDI.B #\$0400,IMR ; Enable SCC2 interrupts ANDI.B \*\*\* Initialize SCC3 to generate interrupts on any change in CD3\* \*\*\* MOVE.L #vector,\$02A0 ; Initialize SCC3 interrupt vector MOVE.W #\$0020.SCON3 ; Baud rate generator on SCC3 used ; Disable reception via first Rx BD #\$0000,RXBD 03 MOVE.W #\$FF.SCCE3 ; Clear out SCC3 event register MOVE.B ANDI.B #\$40.SCCM3 ; Enable CD interrupt MOVE.W #\$0038,SCM3 ; HDLC Mode with receiver enabled \*\*\* Enable SCC1 interrupt on any change in CTS3\* \*\*\* #\$80,SCCM3 ; Enable CTS interrupt ANDI.B : Disable transmission via first Tx MOVE.W #\$0000,TXBD 03 BD #\$0004,SCM3 ; Enable ENT bit of SCC3 ANDI.W \*\*\* Enable SCC3 interrupt on idle status change \*\*\* : Enable RXD3 interrupt ANDI.B #\$20.SCCM3 ; Enable SCC3 interrupts ANDI.B #\$0100,IMR

\*\*\* Enable interrupts to the M68000 core MOVE.W #\$2000,SR ; Unmask interrupts

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