AN13237

TJA1102A dual/single PHY for automotive Ethernet

Rev. 2 — 27 October 2022 **Application note**

Document information

Information	Content
Keywords	Automotive Ethernet, IEEE 100BASE-T1, PHY, Dual-port, TJA1102A
Abstract	The TJA1102A is an IEEE 100BASE-T1 compliant dual-port Ethernet PHY optimized for automotive use cases. The device provides 100 Mbit/s transmit and receive capability over two unshielded twisted pair cables, supporting a cable length of at least 15 m. Optimized for automotive use cases like IP camera links, driver assistance systems and back-bone networks, the TJA1102A has been designed for automotive robustness, while minimizing power consumption and system costs. This document describes the application aspects of the TJA1102A in more detail.

Revision history

Rev	Date	Description
v.1	20211103	Initial version
v.2	20221027	• Section 4.8.1 "POLARITY_DETECT (bit 25.6)" – Added note • Section 5.8 "Mode transitions" – Added paragraph: "In case the TC10 sleep/wakeup functionality is not used..." – Added Table 7 "Recommended setting if TC10 sleep/wakeup functionality is not used" • Added Section 6.1 "Default register settings for compliance testing" • Added Section 6.2 "Configuration for EMC testing"

1 Introduction

The TJA1101A is a 100BASE-T1 compliant dual-port Ethernet PHY optimized for automotive use cases such as IP camera links, driver assistance systems and back-bone networks. It has been designed for automotive robustness, while minimizing power consumption and system costs.

2 100BASE-T1 basics

As a 100BASE-T1 compliant dual-port Ethernet PHY, the TJA1101A provides 100 Mbit/s transmit and receive capability over two unshielded twisted pair cables, supporting a cable length of at least 15 m with a bit error rate less than or equal to 1E-10. It is optimized for capacitive signal coupling to the twisted pair lines. To comply with automotive EMC requirements, a common mode choke is typically inserted into the signal path. The connection to the Media Access Control (MAC) unit is realized by either the standard MII or the RMII.

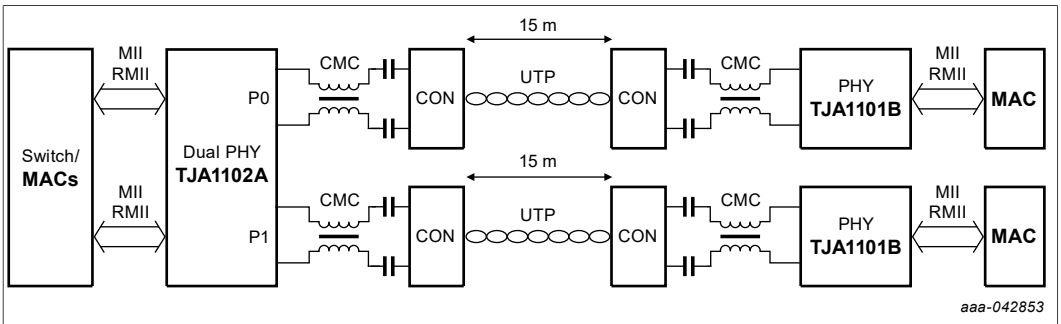


Figure 1. TJA1101A system diagram

2.1 Link startup

Link startup is governed by the PHY control state machine defined in the IEEE 802.3bw standard [1] and illustrated in Figure 2.

Bit LINK_CONTROL in the Extended control register (SMI address: 0x11) must be set to 1 before a link can be established. This holds for both the Master and Slave PHYs. Once this bit is set, the Master PHY initiates the training phase by transmitting an idle pattern (tx_mode = SEND_I). As soon as the receiver in the Slave PHY has been synchronized to the idle pattern, it also enters the training state and starts transmitting an idle pattern. When the minwait_timer expires, the Slave PHY switches to SEND_IDLE state. Now the Master PHY receives an idle pattern from the Slave PHY. As soon as the receiver in the Master PHY has been synchronized (loc_rcvr_status = OK and rem_rcvr_status = OK), it enters the SEND IDLE OR DATA state. Once the Slave PHY detects that the receiver status of the Master PHY is OK (rem_rcvr_status = OK), it also enters the SEND IDLE OR DATA state. From that point onwards, the bidirectional link is established and normal data communication is possible.

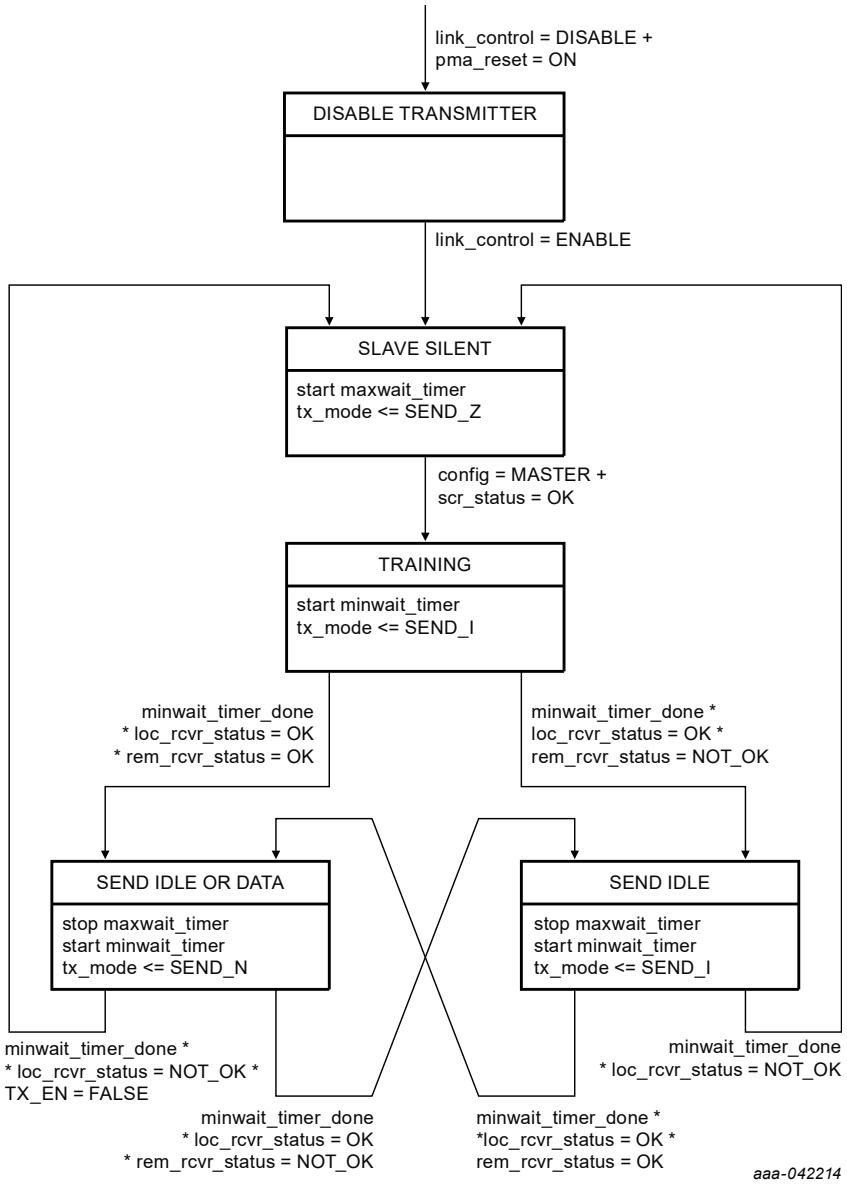


Figure 2. PHY control state machine from the IEEE 802.3bw standard

Following a transition to Normal mode, the next step is to start up the PHY link. After a 2 ms timeout, the link must be enabled by setting LINK_CONTROL to 1 (this happens autonomously when AUTO_OP=1. Since link startup takes some time, the current link status should be checked.

LINK stable is defined as:

LOC_RCVR_STATUS = 1 (local receiver OK)
REM_RCVR_STATUS = 1 (remote receiver OK)
SCR_LOCKED = 1 (descrambler locked)
LINK_UP = 1 (link OK)

These four flags, located in the Communication status register (SMI address: 23), must be set to 1 before communication is allowed. Therefore, they should be checked

to ensure that the link is stable before attempting to start communication. The LINK_STATUS_UP interrupt can be used to indicate when the LINK_UP bit is set.

If a link has not been established within 100 ms after enabling link control, the link diagnosis process could be started to check for an open or short in the Ethernet channel etc. The timing could be adapted if Master and Slave have different startup timing characteristics. Also, a longer startup time may be needed when waiting for the link partner.

If a TRAINING_FAILED interrupt is generated, it indicates that the maxwait_timer has expired and the link was not established in time. The startup procedure is repeated automatically, but the interrupt indicates that there may be an issue establishing a link.

When configured as Slave, and depending on the needs of the application, the POLARITY_DETECT bit could be read to determine if an MDI polarity inversion has been detected and corrected. A wrong polarity is not critical; the link will normally still start up (polarity correction) but a polarity inversion (POLARITY_DETECT = 1) could indicate that the cable polarity has been swapped.

For a better understanding of link startup, a simplified startup timing diagram is shown in Figure 3. It illustrates the procedure followed from the Master startup training until a full link has been established.

Note: *The Master/Slave setting is only relevant for startup and clock recovery; it does not play a role in the actual communication. 100BASE-T1 is full-duplex communication.*

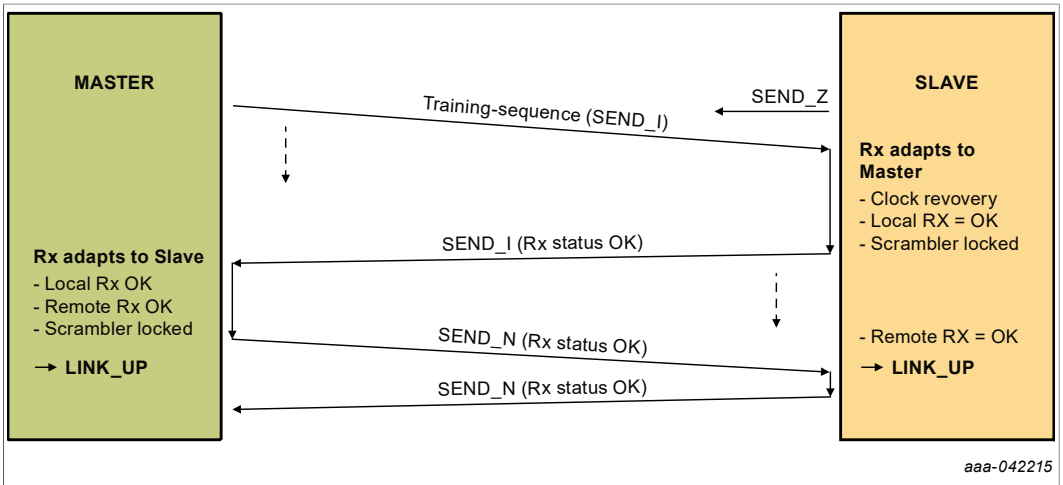


Figure 3. Simplified link startup

3 Hardware application

3.1 Overview

Typical 4-port switch solutions, with and without an external 1.8 V supply, are shown in Figure 4 and Figure 5. The 100BASE-T1 physical layer ports are realized using two TJA1102A devices. They connect to the switch (SJA1105 in these examples) via MII or RMII. Control and status information is exchanged with the host controller via an SMI interface. The INH control outputs of the dual PHYs can be used to switch off the main voltage regulator once all ports have been switched to Sleep mode.

Only a small number of additional components are needed, underlining the ease-of-use of the TJA1101A. The illustrated use cases assume a capacitive coupling to the twisted-

pair wires. To comply with EMC requirements, a common-mode choke should be inserted into the signal path. It is recommended to place the coupling capacitors between the common mode choke and the connector.

When the TJA1101A is used in a switch application with several PHY ports, it may prove more efficient to use an external SMPS to provide the 1.8 V supply. To facilitate this, the TJA1101A provides an option to switch off the internal 1.8 V LDO (a typical application with an external 1.8 V supply is shown in Figure 4).

The 1.8 V power supply mode (internal or external LDO) is determined by pin SEL_1V8, which is evaluated during power-up (via pin strapping).

More detailed application information is provided in the following sections.

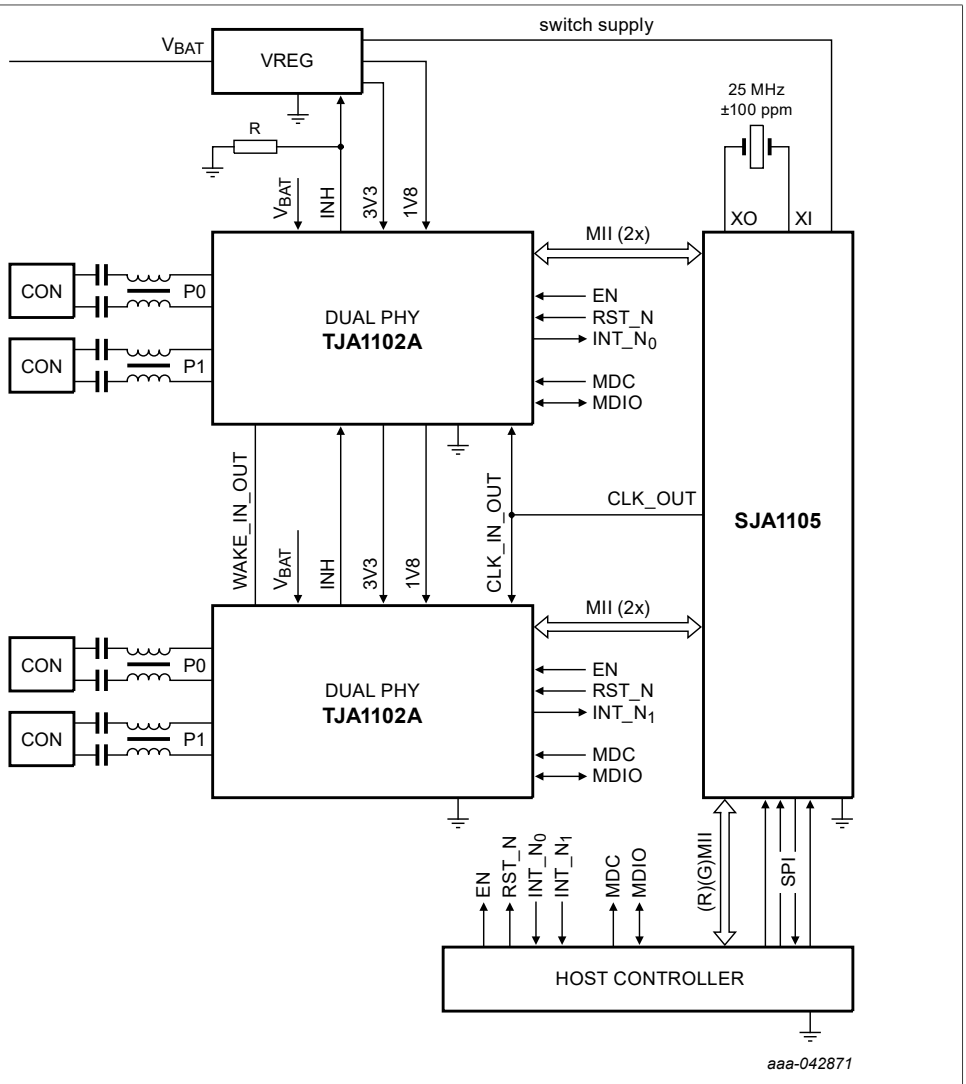


Figure 4. Typical application of the TJA1101A in a Switch application with SJA1105: external 1.8 V LDO.

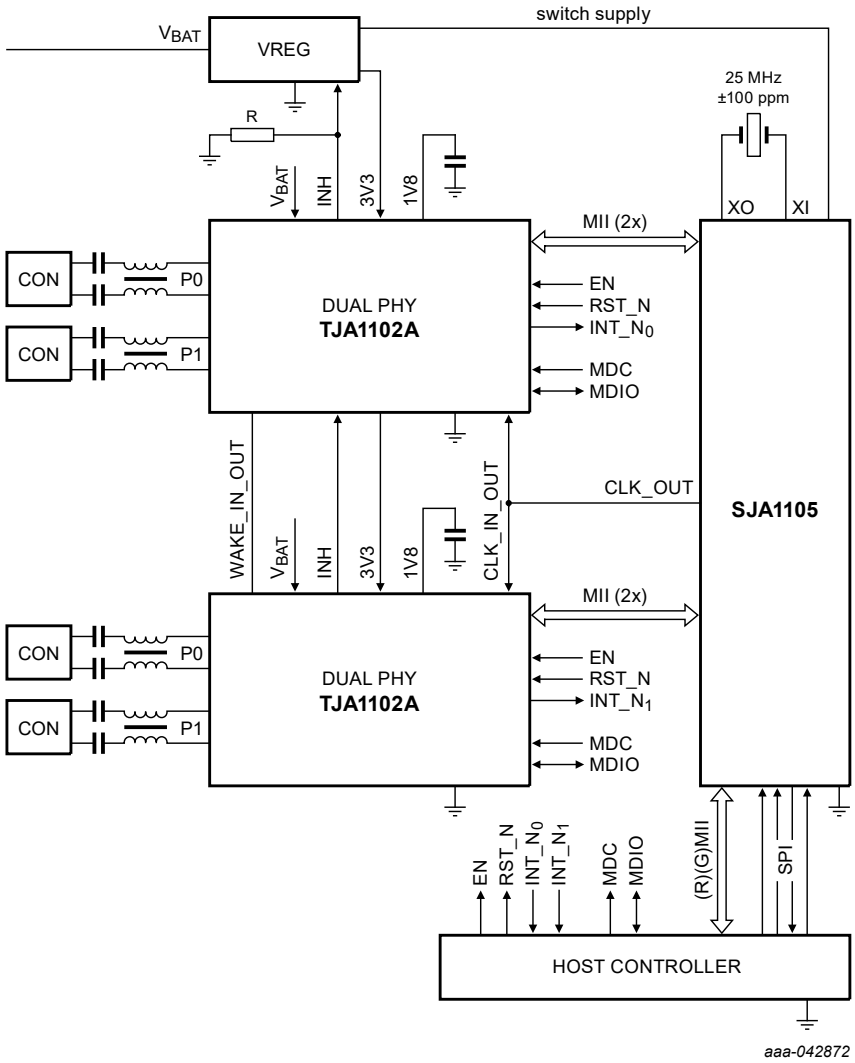


Figure 5. Typical application of the TJA1101A in a Switch application with SJA1105: internal 1.8 V LDO.

3.2 MII/RMII interface

The connections between the PHY and the MAC for MII communication are shown in more detail in Figure 6. MII transmit and receive data is exchanged via 4-bit wide data nibbles on TXD[3:0] and RXD[3:0] and is synchronized with the transmit (TXC) and receive (RXC) clocks. Both clock signals are provided by the PHY and are typically derived from an external crystal running at a nominal 25 MHz (±100 ppm). Normal data transmission is initiated with a HIGH level on TXEN, while a HIGH level on RXDV indicates normal data reception.

RMII transmit and receive data is exchanged via 2-bit wide data nibbles on TXD[1:0] and RXD[1:0], as illustrated in Figure 7. To achieve the same data rate as MII, the interface is clocked at a nominal 50 MHz. A single clock signal, REF_CLK, is provided by the PHY for both transmit and receive data. This clock signal is typically derived from an external 25 MHz (±100 ppm) crystal as illustrated. As for MII signaling, normal data transmission is initiated with a HIGH level on TXEN, while a HIGH level on CRSDV indicates normal data reception.

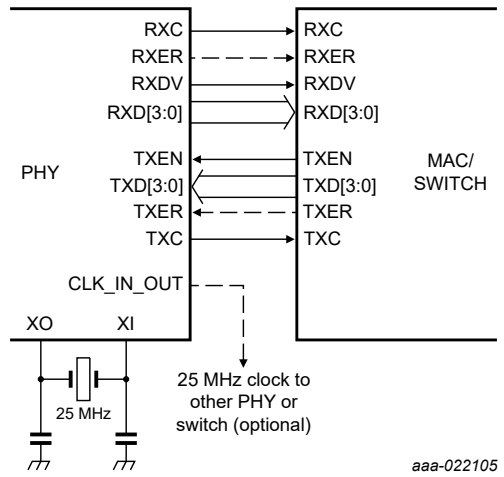


Figure 6. MII signaling using an external XTAL, with an optional 25 MHz-clock output

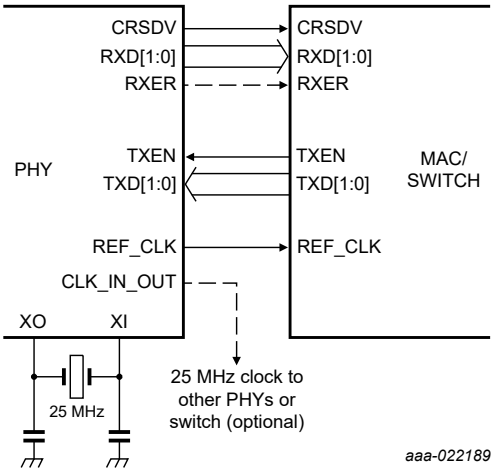


Figure 7. RMII signaling using an external XTAL, with an optional 25 MHz-clock output

The trace length between PHY and MAC should be kept short to ensure a capacitive load at the fast switching pins (input capacitance of MAC plus PCB trace) of less than 15 pF. The PCB trace impedance should be at least 50 Ω with a line delay of less than 1 ns. To allow for further EMC fine tuning, series resistors of around 20 Ω can be added.

If the capacitive load can be kept below 7.5 pF and the connection between PHY and MAC is short, the MII and RMII output driver slew rate may be reduced for improved EME performance by setting configuration bit MII_DRIVER to 1. It is expected that the timing for this setting will be checked with the available IBIS model or through measurements.

When the TJA1101A is in crystal mode, it can be configured to output the 25 MHz clock signal on pin CLK_IN_OUT via the SMI interface (CLK_MODE = 01) or via pin stapping. See Section 3.9 "Pin strapping".

Examples of the PHY being driven from an external 25 MHz clock source are shown in Figure 8 and Figure 9. The REF_CLK signal in Figure 9 can be from PHY to MAC or MAC to PHY, depending on the PHY/MAC configuration. Note that the frequency tolerance of the external clock source must be within ±100 ppm. Pin XI should be connected to ground and pin XO should be left open when using an external clock.

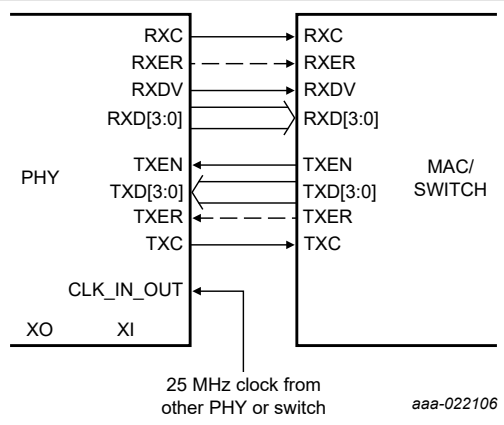


Figure 8. MII signaling using an externally generated 25 MHz reference clock

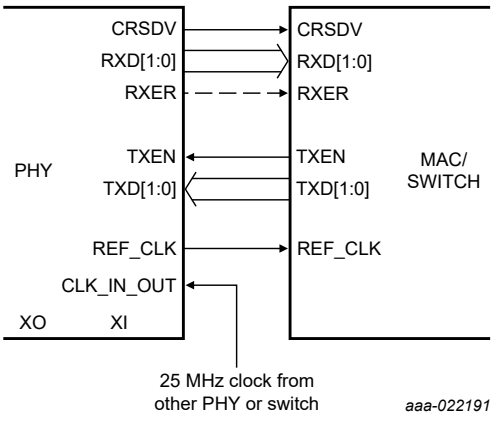


Figure 9. RMII signaling using an externally generated 25 MHz reference clock

For RMII, the clock signal for both PHY and MAC can be provided by an external 50 MHz oscillator as illustrated in Figure 10. The frequency tolerance of the external oscillator must be within ±50 ppm. Pin XI should be connected to ground and pin XO should be left open.

The ±50 ppm frequency tolerance of the external 50 MHz clock input is necessary since it will be used as the recovered clock in the TJA1101A, and there will be a ppm difference between the 50 MHz REF_CLK received from the MAC and the recovered clock. No clock will be available on the CLK_IN_OUT pin.

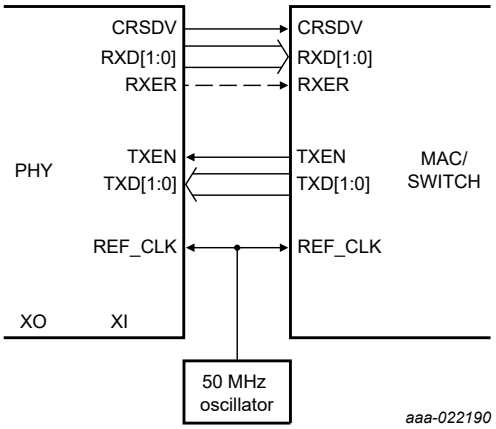


Figure 10. Fig 9. RMII signaling with 50 MHz oscillator reference clock

3.2.1 Unused MII pins

When optional MII pins are not used, input pins should be pulled LOW while output pins can be left open.

For RMII, unused pins (e.g. RXD2, RXD3) can be left open, unless they are used for pin strapping.

3.3 SMI interface

The SMI (Serial Management Interface) serial bus, defined in the IEEE802.3 clause 22 standard, provides access to the control and status registers.

3.3.1 SMI pins

The SMI interface uses two signals:

- MDC (Management Data Clock): driven by the MAC to the PHY. The MDC can be clocked at up to 2.5 MHz, corresponding to a minimum clock period of 400 ns.
- MDIO (Management Data Input/Output): bidirectional, driven by the MAC to the PHY during a write transaction. For a read transaction, the PHY takes over the MDIO line during the turnaround bit times, supplies the MAC with the register data requested, and then releases the MDIO line.

To allow for further EMC fine tuning, a series resistor of around 20 Ω can be connected to the MDC line. The MDIO needs a pull-up resistor (of about 10 kΩ) to V_{DDIO}. The pull-up can be integrated into the MAC. Make sure that only one 10 kΩ pull-up resistor is connected to the MDIO bus.

The only valid SMI operations in Sleep mode are reading the POWER_MODE status bits in the Extended control register and issuing a Standby mode command. PHY status information is not valid in Sleep mode.

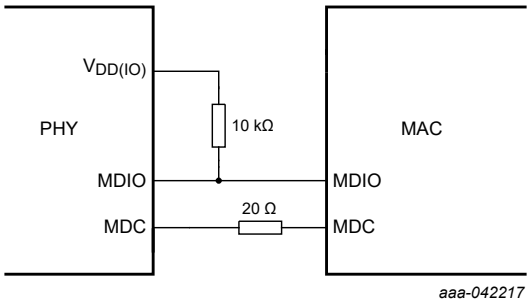


Figure 11. SMI interface

3.3.2 SMI frame structure and bus timing

The SMI interface supports a single MAC as Master, and can have up to 32 PHY slaves. Frames transmitted on the SMI interface should have the frame structure shown in Table 1. The order of bit transmission is from left to right.

Table 1. SMI frame format

Preamble		Start of frame	Operation code	PHY address	Register address	Turnaround	Data	Idle
read	1.... 1	01	10	AAAAA	RRRRR	Z0	D... D	Z
write	1.... 1	01	01	AAAAA	RRRRR	10	D... D	Z

Preamble: At the beginning of each transaction, the MAC sends a sequence of 32 continuous logic 1 bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization.

Start of frame: The start of frame is indicated by a <01> pattern.

Operation code: <10> for a read transaction; <01> for a write operation.

PHY address: The PHY address is 5 bits long. The first PHY address bit transmitted and received is the MSB of the address. Refer to bits PHYAD[4:0] in Configuration register 2 for the TJA1101A PHY address.

Register address: The Register address is 5 bits long. The first register address bit transmitted and received is the MSB of the address.

Turnaround: The turnaround time is a 2-bit delay between between the register address and data field transmission.

Data: The data field is 16 bits long.

Idle: The idle condition on MDIO is a high-impedance state. The pull-up resistor pulls MDIO to logic 1.

An example of an SMI write/read transaction is shown in Figure 12. Bit sampling is performed on the rising edge of the clock MDC.

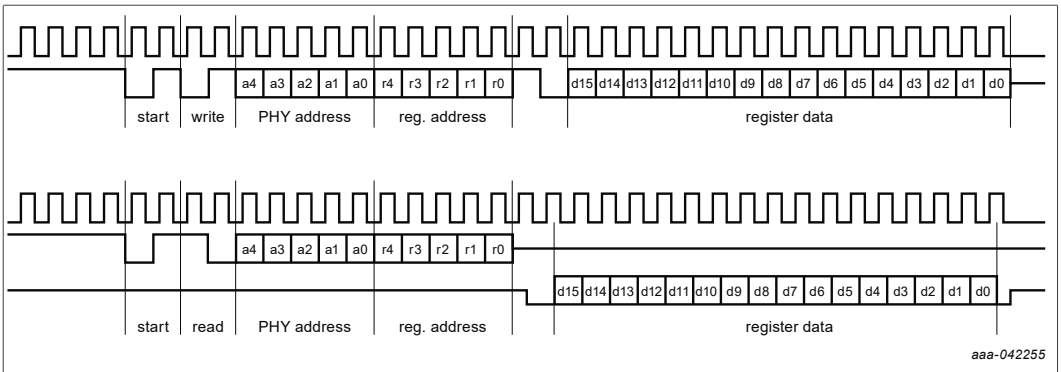


Figure 12. Example of SMI write/read transaction

3.4 MDI interface

The MDI circuitry shown in Figure 13 can be used at each PHY port. The common mode termination can vary, depending on OEM requirements.

The common mode choke is expected to be compliant with the OPEN Alliance CMC specification [2]. The tolerance of the 100 nF capacitors should be within ±10 % with max rating ≥50 V.

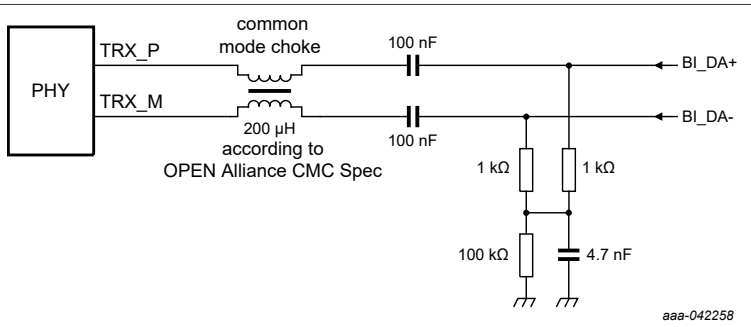


Figure 13. MDI circuit without external ESD diodes

The TJA1101A features high ESD robustness at the IC pins (see [3]). For greater ESD robustness, external ESD protection diodes can be added, as shown in Figure 14.

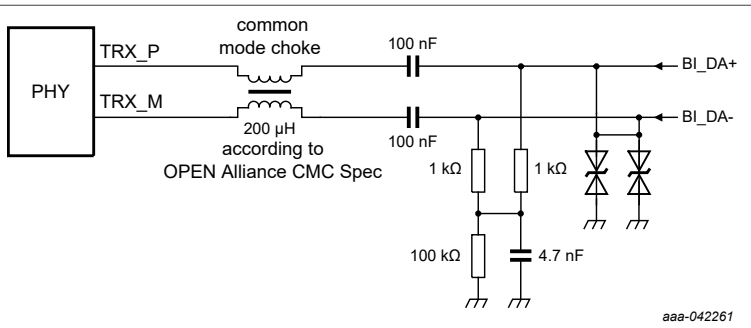


Figure 14. MDI circuit with external ESD diodes

3.4.1 Common-mode choke

The common-mode choke provides the common-mode rejection needed to handle typical common-mode noise in an automotive environment. While it helps to get rid of common-mode noise over a broad frequency range, the choke may appear to be a major source of differential noise due to common-to-differential-mode conversion. Therefore, only high-quality symmetrical chokes should be used. The most important requirements for chokes are defined in [2].

3.4.2 AC coupling

AC coupling is realized by using 100 nF coupling capacitors to form a high-pass filter together with the 50 Ω termination on each line (see Figure 13). The tolerance of the capacitors should be within ±10 % with max rating ≥50 V.

3.4.3 Low-pass filter

External low-pass filtering is not needed for the TJA1101A as effective low-pass filtering has been integrated into the PHY, for both the transmit and receive signal paths.

3.4.4 Common-mode termination

For common-mode termination, a split termination consisting of two 1 kΩ resistors and a 4.7 nF capacitor, with a 100 kΩ resistor to GND, can be connected to the signal lines between the coupling capacitors and the connector. For reasons of symmetry, the tolerance of the two 1 kΩ resistors should be within ±1 %. The power rating should be higher than 0.4 W (anti-surge) in order to survive EMI disturbances. Please check implementation details and other requirements with the customer (OEM). No specific power rating is specified for the 100 kΩ resistor and 4.7 nF capacitor, but components should be rated max ≥50 V.

3.4.5 ESD protection diodes

If extended ESD robustness is needed and external ESD protection is being used, the ESD components should be compliant with the OPEN Alliance ESD specification [4]. Please check with the ESD diode vendors regarding the corresponding test report. It can be a single device for both MDI lines or two separate devices, one per line.

3.4.6 Differential signal layout

The differential signal pair TRX_P/TRX_M should be routed close together with a controlled impedance of 100 Ω. Since symmetry is critical for EMC performance, the two differential pair traces should be as close to identical as possible. To increase the effectiveness of the choke or transformer at higher frequencies and to minimize parasitic capacitances, also consider a cut-out of the ground plane beneath the differential signal path from the PHY to the connector. The choke should be placed close to the PHY.

The insertion loss in the path from the PHY to the connector should be less than 2 dB at all frequencies from 1 MHz to 33 MHz. The return loss limit is defined in the IEEE 802.3bw standard [1].

Note that the symmetry requirements for MDI mode conversion must remain within the limits defined in the OPEN Alliance Automotive Ethernet ECU Test Specification [5].

Please note that the min., typ. and max., values specified for the integrated termination resistor should be used in the PCB simulation.

3.4.7 Communication channel

The channel used needs to fulfill the channel requirements described in [1]. Furthermore, to ensure echo is fully canceled, it is recommended to use a channel with a total cable propagation delay of less than 110 ns including the PCB track. This means that, if the cable propagation delay is greater than 5 ns/m, the maximum cable length of 15 m will need to be reduced accordingly.

3.5 Supply

Schematics showing V_{BAT} supplied from an external 3.3 V regulator and from the battery are shown in Figure 15 and Figure 16. Figure 17 shows $V_{DDD(1V8)}$ supplied from an external 1.8 V LDO.

For supply rails connected to more than one pin (e.g. V_{DDIO}), the capacitors shown the the schematic diagrams are needed on each pin. The buffer capacitors should be placed as close as possible to the pins. For pins $V_{Px\_DDA(TX)}$ and $V_{DDD(1V8)}$ in particular, it is important to have low-impedance connections and closed loops to GND.

For supply pins $V_{P0\_DDA(TX)}$ and $V_{P1\_DDA(TX)}$, a common low-impedance capacitor can be placed on the bottom side with 2x2 vias to the supply pins on top. The capacitor should be connected directly to the GND plane underneath the exposed die pad.

An additional (optional) 10 nF capacitor on $V_{DDD(1V8)}$ and 1 nF on V_{BAT} (shown in Figure 15) would improve the emission performance of those supply lines.

The PCB should allow for the possibility to connect ferrite beads to $V_{P0\_DDA(TX)}$, $V_{P1\_DDA(TX)}$, $V_{DDA(3V3)}$, $V_{DDD(3V3)}$ and $V_{DD(IO)}$. For initial testing, 0 Ω resistors can be used. To what extent the ferrite beads are needed depends on the EMC results. The 22 µF electrolytic capacitor connected to the output of the voltage regulator only takes into account the buffering needs of the PHY. A higher value may be needed when also considering the buffering needs of the microcontroller.

As shown in Figure 16, V_{BAT} can also be supplied directly from the battery. This option is intended to be used mainly for wake-up support. It is recommended to place a series resistor of e.g. 1 kΩ into the battery supply line to the PHY for enhanced protection against automotive transients. A capacitor of e.g. 100 nF, closely connected to V_{BAT} and forming a low-pass filter in conjunction with the series resistor, can be added for enhanced transient protection.

Note that the maximum slew rate on V_{BAT} should be limited to below 10 V/µs for rising edge and 1 V/µs for falling edge above 2 V(p-p) amplitude.

The TJA1101A has been designed so that it does not need to follow a dedicated power-up/down supply sequence. It does not matter whether the 3.3 V pins are supplied before the V_{BAT} pin, and vice versa.

Being optimized for automotive use cases, the TJA1101A can also handle a wide range of slow and fast ramping supply conditions.

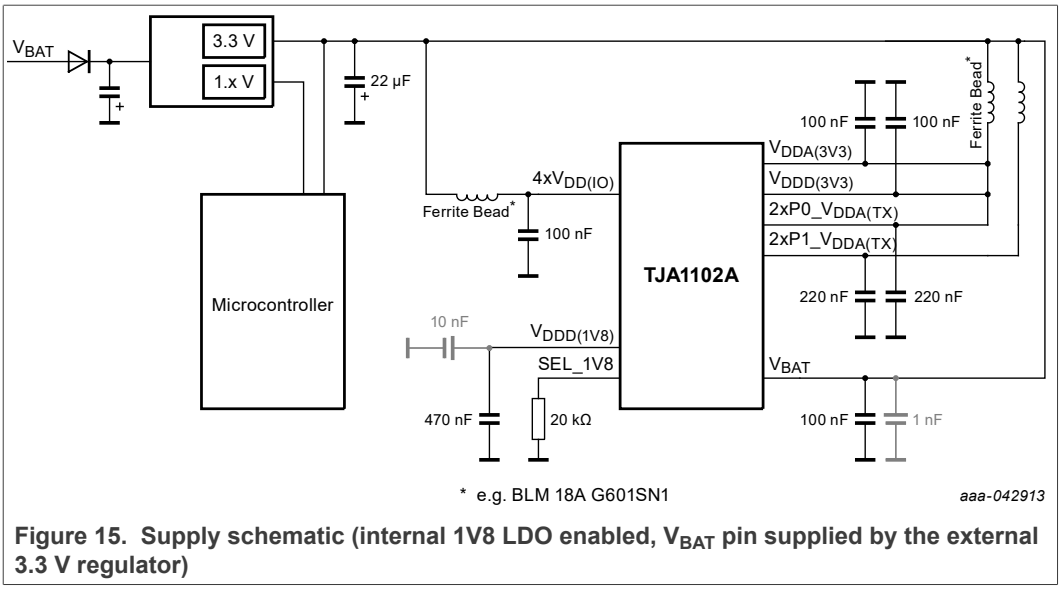


Figure 15. Supply schematic (internal 1V8 LDO enabled, V_{BAT} pin supplied by the external 3.3 V regulator)

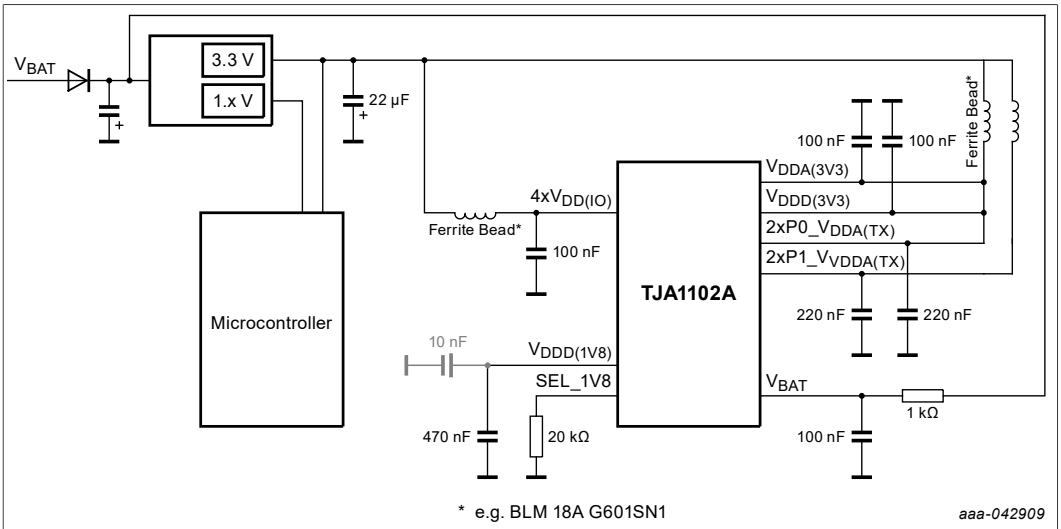


Figure 16. Supply schematic (internal 1V8 LDO enabled, V_{BAT} pin supplied by the battery)

When $V_{DDD(1V8)}$ is supplied externally, pin SEL_1V8 should be held HIGH. No further changes to the circuitry are needed (see Figure 17)

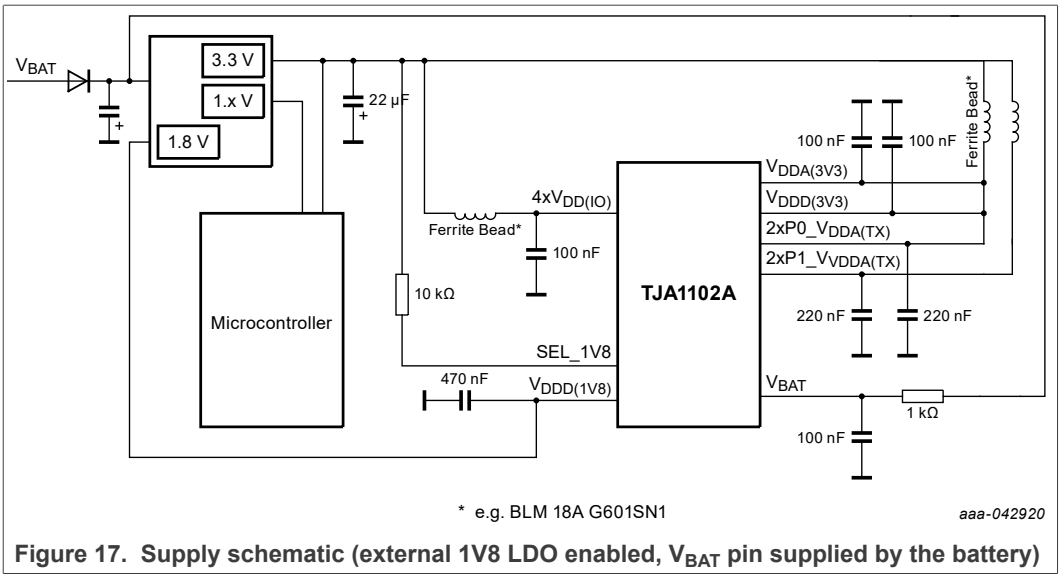


Figure 17. Supply schematic (external 1V8 LDO enabled, V_{BAT} pin supplied by the battery)

3.6 Host interface (RST_N, INT_N, EN)

RST_N and EN are input signals to the PHY and are typically driven by GPIO pins on the microcontroller, while INT_N is an input signal to the microcontroller.

INT_N is an open collector output, allowing several PHYs to be connected in parallel to a single interrupt input to the microcontroller. An external pull-up (approx. 10 kΩ) is needed. No further components are needed.

For EN and RST_N, a pull-up or pull-down can be connected if a certain level is expected by default (EN has a weak pull-down; RST_N has a weak internal pull-up). The value (e.g. 10 kΩ) should be chosen to guarantee a proper HIGH/LOW level (taking into account other resistance sources on the line, e.g. in the microcontroller).

When the EN or RST_N pins are not used, they should be connected to $V_{DD(IO)}$. INT_N can be left open when not used.

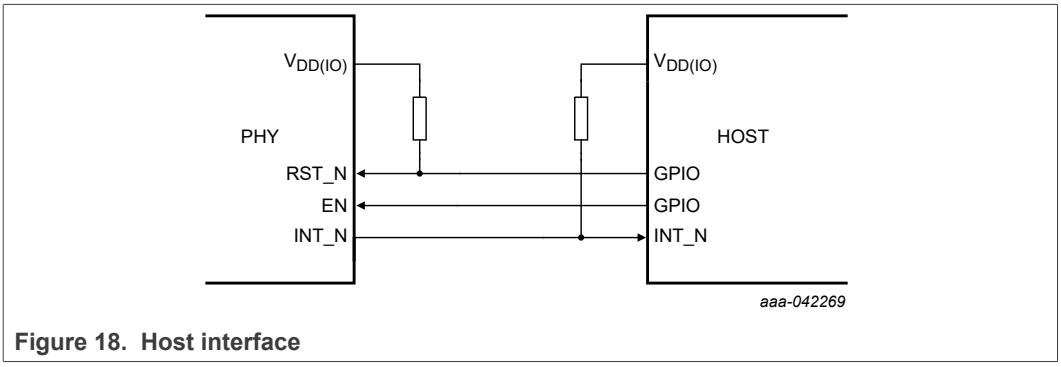


Figure 18. Host interface

At startup, when EN is LOW, the PHY will first enter Standby mode before reacting to the LOW level on EN and switching to Disable mode.

3.7 WAKE_IN_OUT pin

WAKE_IN_OUT is a bidirectional pin that can be used as a local wake-up input or forwarded as a wake-up output.

If configuration bit LOCWUPHY is set to 1, the WAKE_IN_OUT pin acts as a local wake-up input. A programmable timeout, configured via the bit LOC_WU_TIM, is provided to support different wake-up concepts (e.g. wake-up line). The duration of the wake-up pulse (t_p) is also determined by LOC_WU_TIM. Note that wake-up is triggered on the rising edge of the local wake-up pulse.

The WAKE_IN_OUT pin can also be configured as a wake-up forwarding output by setting bits FWDPHYLOC and REMWUPHY to 1. The WAKE_IN_OUT pin will be switched to the V_{BAT} level for the duration of the wake-up pulse (t_p) after a remote wake-up has been triggered at the PHY. Otherwise this pin will be floating.

3.8 INH pin

The INH pin is intended to be used to control one or more voltage regulators in the ECU. In the application examples shown in Figure 4 and Figure 5, the voltage regulator for the Switch and the PHY is controlled via the INH output.

Pin INH is a battery-related open-drain output. It is floating when the device is in Sleep or Disable mode (configurable). Since the inhibit pin on common voltage regulators typically features an internal pull-down to ground, the resulting LOW level disables them in these modes. In all other operating modes, the pin INH is actively pulled HIGH to V_{BAT}, enabling the voltage regulator(s). In cases where there is no internal pull-down on the inhibit input of the voltage regulator, an external pull-down resistor (5 kΩ to 20 kΩ) is needed (as illustrated in Figure 4 and Figure 5).

It is recommended not to drive more than 1 mA out of the INH pin when it is active. In contrast, pin INH provides up to 15 mA current when switching from floating (LOW) to active (HIGH). The maximum load resistance at pin INH can be calculated accordingly. The INH pin can be left open if it is not used.

3.9 Pin strapping

The TJA1101A allows for some hardware configuration via pin strapping during power-on. Pin strapping is implemented using the CONFIGx, PHYADx and SEL_1V8 pins [3]. A pull-up is coded as logic 1, a pull-down as logic 0. Pull-up/pull-down resistor values should be between 5 kΩ and 20 kΩ. The value should be high as possible to limit the impact on the data signal, but low enough to guarantee the correct pin strapping value (e.g. to overrule the reset behavior of µC pins).

Pin strapping is performed when the PHY enters Standby mode after power-on. It will be repeated after a hardware reset via the RST_N pin.

All pre-configuration pin strapping settings (except for the PHY address) can be overwritten via SMI commands.

Table 2. Hardware configuration via pin strapping[1]

Symbol	Pin	Value	Description
MASTER_SLAVE/ PHY_EN	34 (CONFIG3) 33 (CONFIG2) 32 (CONFIG1)	000[2]	P0 disabled, P1 Master
		001	P0 disabled, P1 Slave
		010	P0 Master, P1 disabled
		011	P0 Master, P1 Master
		100	P0 Master, P1 Slave
		101	P0 Slave, P1 disabled
		110	P0 Slave, P1 Master
		111	P0 Slave, P1 Slave
AUTO_OP	55 (CONFIG0)	0	managed operation
		1	autonomous operation
PHYAD[3:1]			PHY Address strapping for P0 even values 0 through 14 PHY Address strapping for P1 odd values 1 through 15
	37 (PHYAD3)	000	bit 3 of PHY address used for the SMI
	36 (PHYAD2)	- - -	bit 2 of PHY address used for the SMI
	35 (PHYAD1)	111	bit 1 of PHY address used for the SMI
MII_CONFIG	1 (CONFIG5) 56 (CONFIG4)	00[3]	MII mode enabled for both PHYs
		01[4]	RMII mode enabled for both PHYs
		10[3]	Reverse MII mode P0; MII mode P1, internal MII
		11[3]	Reverse MII mode P0; MII mode P1; external MII
CLK_MODE	3 (CONFIG7) 2 (CONFIG6)	00	25 MHz XTAL; no clock at CLK_IN_OUT
		01	25 MHz XTAL; 25 MHz at CLK_IN_OUT
		10	25 MHz external clock at CLK_IN_OUT
		11	50 MHz input at REF_CLK; RMII mode only; no XTAL; no clock at CLK_IN_OUT
LDO_MODE	15 (SEL_1V8)	0	internal 1.8 V LDO enabled
		1	external 1.8 V supply

[1] Pin strapping functionality relating to PHY1 is not relevant to the TJA1102AS, since P1 is permanently disabled.
[2] Ordered from MSB to LSB; for value 011 for example, pin 34 = 0, pin 33 = 1 and pin 32 = 1. Note that PHY1 is always disabled in the TJA1102AS, regardless of the value level of on these pins during pin strapping.
[3] CLK_MODE = 00, 01 or 10.
[4] All clock modes (CLK_MODE = xx).

The behavior of the µC in reset should be considered to ensure proper pin strapping levels. Pin-strapping by means of pull-up/pull-down resistors will not work if the microcontroller drives a fixed level on these pins during power-on. In this case, it is recommended to hold the PHY in Reset mode (pin RST_N LOW) during power-on. Once the microcontroller has been initialized, it can drive the pin-strapping pins to the required levels via software before releasing the PHY reset.

Figure 19 shows the points at which the EN, RST_N and pin-strapping pins are sampled during the power-on and hardware reset phases, with the 1V8 LDO enabled. Standby Init is an intermediate state between Power-on/Reset modes and Standby mode.

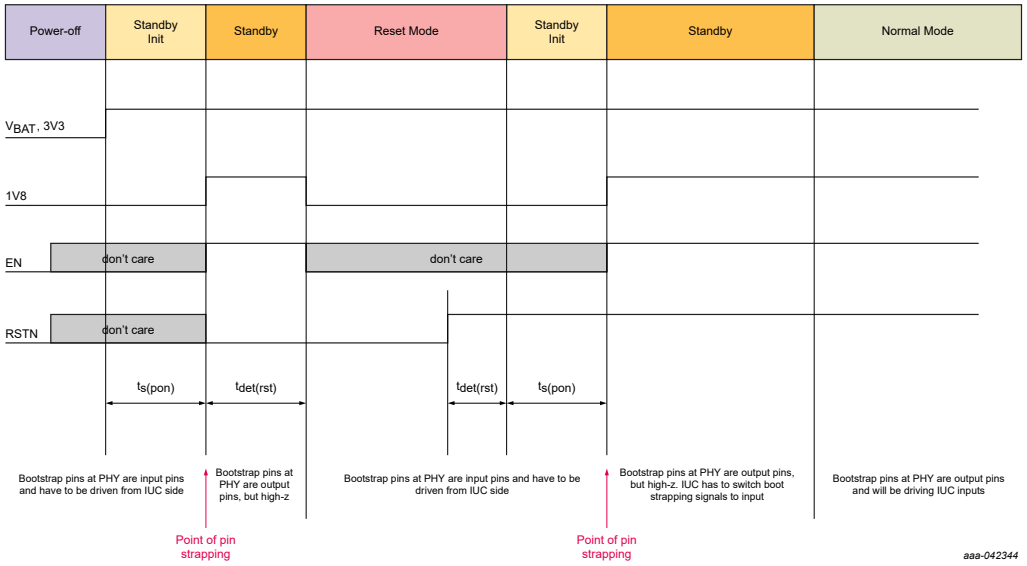


Figure 19. Fig 18. EN/RST_N/pin-strapping sample times during power-on/reset phases

3.10 Clocking (XTAL)

A 25 MHz crystal can be used to clock the TJA1101A and, for RMII, a 50 MHz clock on REF_CLK can be used as an alternative. When a crystal is used, it should fulfill the requirements listed in Table 3.

Table 3. XTAL requirements for TJA1101A clock

Parameter	Required value
Frequency	25 MHz
Tolerance	100 ppm (including all relevant external factors; e.g. aging, temperature etc.)
ESR	100 Ω (max)
Load capacitance	≅10 pF; see Section 3.11
Drive level	≥100 µW

3.11 Load capacitance

The trimming of the XTAL must be taken into account when calculating load capacitance. Details will be provided by the XTAL supplier. The capacitor mounted on the PCB should meet this requirement and satisfy the ppm requirements. The input capacitance on pin XO is typically 2 pF, and 3.5 pF on XI.

3.12 CLK_IN_OUT_clocking

Clocking via the CLK_IN_OUT pin is configured via the SMI (CLK_MODE = 10) or pin strapping.

Table 4. XTAL requirements for TJA1101A clock

Parameter	Required value
Frequency	25 MHz
Tolerance	MII/RMII: 100 ppm
Jitter	≤30 ps,RMS (12 kHz to 20 MHz)
Rise/fall time	≤6 ns (20 % to 80 %)
Duty cycle	40 % to 60 %

4 Control and status registers

This section provides a more detailed view on the most important registers used to control the TJA1101A It adds to, but is not a replacement for, the description in the data sheet [3].

4.1 Basic control register (Address 0)

For basic PHY applications, the TJA1101A provides a number of standard control features such as reset, loopback control, power-down, PHY isolation and unidirectional enable. These features can be accessed via the Basic control register (register address 0x00) as defined in clause 22 of IEEE802.3. Note that control bits 13, 12, 9, 8, 7 and 6 are not applicable to 100BASE-T1 PHYs and are, therefore, not functional in the TJA1101A.

While the TJA1101A can be controlled via the Basic control register, it is recommended to use the Extended control register instead to make use of the full feature set.

4.1.1 Reset (bit 0.15)

A soft reset of the PHY core (internal state machines, filter coefficients etc.) can be triggered by setting this bit to 1. The PHY restarts automatically after the reset (if it is activated via LINK_CONTROL). This facility can be useful when the link fails to start up properly.

The reset bit does not affect device configuration or register bit values; the RSTN pin is used for a hard reset (resetting all register bits).

4.2 Basic status register (Address 1)

Basic status information on jabber detect, link status and remote fault conditions are provided via the Basic status register (via bits 1, 2 and 4 respectively; remaining register bits are not applicable to 100BASE-T1 PHYs).

4.3 Extended control register (Address 17)

The Extended control register allows access to TJA1101A control features not available in the Basic control register. These extended control features are described in detail in the following sections. It is recommended to configure the TJA1101A via the extended control register.

4.3.1 LINK_CONTROL (bit 17.15)

In managed operation, link control must be enabled (LINK_CONTROL = 1) before a link can be established. This holds for both the Master and Slave PHYs. Once this bit has been set, the Master PHY initiates the training phase by sending idle patterns. As soon as the Slave PHY has been synchronized, it responds by also sending idle patterns. Bit LINK_CONTROL must be reset to 0 to disable a link. A mode transition from Normal to Standby, Disable or Reset automatically resets the LINK_CONTROL bit (disabling link control).

For autonomous operation, LINK_CONTROL is set to 1 automatically on entering Normal mode. As a result, a link start-up will be performed automatically after power-on.

4.3.2 POWER_MODE (bits 17.14:11)

The TJA1101A supports three primary operating modes: Normal, Standby and Sleep (Request). The operating mode is selected via bits POWER_MODE (provided bit POWER_DOWN in the Basic control register is set to 0 for normal operation).

The operating modes are described in Section 5 "Operating modes" and in [3].

4.3.3 TRAINING_RESTART (bit 17.9)

If the receiver cannot be synchronized within a defined period (maxwait_timer, see Figure 2; no LINK_UP) during training, the TJA1101A aborts the current training phase. After the receiver has been reset, a new training phase starts automatically. A TRAINING_FAILED interrupt indicates a failed training phase.

Since training restarts automatically, there is no need to set this bit. It is provided to allow training to be restarted manually.

4.3.4 CONFIG_EN (bit 17.2)

Write access to the configuration registers (registers 18, 19, 27 and 28) is disabled by default for safety reasons. To change the configuration, write access to the configuration register must be enabled by setting CONFIG_EN to 1. It is expected that the configuration will be performed after power-on as part of the initialization routine; however reconfiguration of the PHY is possible at any time. Before reconfiguration of PHY-related setting (e.g. Master/Slave change), it is recommended to first stop the link and enter Standby mode. After changing the configuration, it is recommended to disable write access again.

4.3.5 WAKE_REQUEST (bit 17.0)

This bit forms part of the wake/sleep process. A link-partner in Sleep mode must be activated before a link can be re-established. For this reason, the node requesting the link can issue a wake request by transmitting idle patterns over the link. The link partner will detect the idle activity and respond by waking up.

In Master mode, enabling link control by setting LINK_CONTROL to 1 will cause a wake-up pulse (WUP) to be generated automatically when the PHY starts transmitting idle patterns (training)

In Slave mode, idle pattern transmission will not start until data has been received. Therefore, a dedicated wake request is needed. Setting bit WAKE_REQUEST with link control disabled will generate a wake-up pulse (WUP). LINK_CONTOL can then be set

to 1 in the subsequent SMI access, which activates the PHY directly after the WUP has ended.

Setting WAKE_REQUEST with link control enabled will trigger the transmission of a wake-up request (WUR), used for wake forwarding.

Note that the WAKE_REQUEST bit is self-clearing, meaning that it will be 0 once the wake request has been executed. If it remains set to 1, the PHY will wait for the right conditions before executing the request, e.g. if LINK_CONTROL is set, a link must be up before the WUR can be sent.

4.4 Configuration register 2 (Address 19)

4.4.1 SQI_AVERAGING (bits 19.10:9)

The SQI value is already averaged and changing this parameter has no impact. It is recommended not to change the default value.

4.4.2 SQI_FAILLIMIT (bit 19.5:3)

If an SQI fail limit is defined, the link is reported as failed (LINK_UP = 0/LINK_STATUS = 0) when the SQI reaches this limit. Note that the link itself will be maintained and link status (LINK_UP =1/LINK_STATUS =1) will be set to 'link OK' once the SQI value rises above the fail limit threshold.

4.4.3 JUMBO_ENABLE (bit 19.2)

The JUMBO_ENABLE setting determines the timeout time for jabber detection (via bit 1.1 in the Basic status register); see parameter $t_{to(PCS\text{-}RX)}$ in [3].

4.5 Interrupt source register (Address 21)

4.5.1 PWON (bit 21.15)

This bit is set to indicate that the device was previously in Power-off mode due to undervoltage on V_{BAT}. As a result, all configuration settings are reset to default values (including pin strapping) and must be (re-)configured.

4.5.2 PHY_INIT_FAIL (bit 21.11)

This bit is set to signal a PHY initialization failure (usually due to external events; e.g. PLL not locked). If a PHY_INIT_FAIL interrupt is generated, check the General and External status registers. If no issue has been reported, reset the PHY.

4.5.3 LINK_STATUS_FAIL/LINK_STATUS_UP (bits 21.10/9)

A LINK_STATUS_FAIL interrupt is generated when bit LINK_UP is changed from 1 to 0 to indicate a link failure. A LINK_STATUS_UP interrupt is generated when bit LINK_UP is changed from 0 to 1 to indicate that link status is now OK.

Since these bits are latched, it is possible that both bits could be set at the same time. This would happen if the link went down and then up again since the last time the Interrupt source register was read. Always use the LINK-UP bit in the communication status register to determine the current link status.

4.5.4 TRAINING_FAILED (bit 21.7)

A TRAINING_FAILED interrupt is generated if the link fails to start up within maxwait_timer (200 ms; see Figure 2). Since training restarts automatically, no action is needed. Nevertheless, this interrupt can indicate a potential fault - if the link partner is up and external conditions are OK the link should come up within 100 ms.

4.5.5 CONTROL_ERR (bit 21.5)

Two conditions will generate a CONTROL_ERR interrupt:

- If bits POWER_DOWN and ISOLATE in the Basic control register (bits 0.11 and 0.10) are set at the same time, a control error will be reported. Note that if one of these bits is set, it should be reset in one SMI access before the other bit is set via another SMI access.
- If an invalid value is written to bits POWER_MODE in the Extended control register (bits 17.14:11), a control error will be reported.

When a CONTROL_ERR interrupt is generated, the Basic and Extended control registers should be checked to ensure that the correct values have been written.

4.5.6 UV_ERR/UV_RECOVERY (bits 21.3/2)

A UV_ERR interrupt is generated when an undervoltage condition is detected. A UV_RECOVERY interrupt is generated when the device recovers from an undervoltage condition.

Since these bits are latched, it is possible that both bits could be set at the same time. This would happen if the devices suffered and recovered from an undervoltage since the last time the Interrupt source register was read. Always use the corresponding bits in the external status register to determine the current UV status.

4.6 Communication status register (Address 23)

4.6.1 LINK_UP/LOC_RCVR_STATUS/REM_RCVR_STATUS/SCR_LOCKED (bits 23.15/12/11/10)

These bits provide information about the status of the link, the descrambler and the local and remote receivers.

4.6.2 SSD_ERR/ESD_ERR (bits 23.9/8)

These bits are set to indicate that an SSD or ESD error has been detected.

4.6.3 PHY_STATE (bits 23.2:0)

These bits provide information on the status or the PHY core. This information might help with failure analysis. The most relevant settings are:

PHY Idle

The PHY core is operational but not activated, e.g. LINK_CONTROL= 0 or in Standby mode.

PHY Initializing

After enabling the PHY, an initialization period is needed to configure the PHY core to its default state. The time is very short and this status is normally not read.

When the PHY gets stuck in this mode, in most cases the PLL is missing. If all external conditions are OK and the PHY remains in this state, a reset should be be initiated.

PHY Active

This is the PHY operating mode. The PHY must be in this mode to establish a link.

PHY Isolate

Indicates if the PHY is isolated (via bit ISOLATE bit in the Basic control register).

PHY Cable test

The PHY will be in this state while it is actively running the cable test (CABLE_TEST = 1). Once the cable test is finished, it switches back to the previous state.

PHY Test mode

Indicates that the PHY is running in a test mode. If a test mode has been configured but the expected output on MDI is not recognized, check that a test mode has been activated. If not, the procedure for entering the test mode should be re-activated.

4.7 General status register (Address 24)

4.7.1 PLL_LOCKED (bit 24.14)

PLL locked is a pre-condition for activating the PHY. If the PLL is not locked, the clock source as well as clock settings should be checked.

4.7.2 EN_STATUS (bit 24.10)

The EN pin can be used by the host or another external device to disable the PHY. The SMI registers are not accessible when EN is LOW. As soon as EN goes HIGH again, bit EN_STATUS is set to 0 to report that the device has been disabled since the last register read operation. This can be useful information when checking functionality and in case of failures, e.g. if EN was unintentionally forced LOW.

4.7.3 RESET_STATUS (bit 24.9)

This bit is set to indicate that a reset via pin RSTN pin has been detected. Register values (including pin strapping) are reset to default values and might need to be (re-)configured.

4.8 External status register (Address 25)

4.8.1 POLARITY_DETECT (bit 25.6)

Polarity detection is available in Slave mode and will automatically correct the order of the MDI pins in case they are swapped on the channel. No action is needed while the link is coming up; however it might be necessary to report to a higher software layer if a swapped polarity is not expected. This helps with failure diagnosis.

Note: *Polarity detection/correction is always on. If polarity correction is not wanted, the software could monitor POLARITY_DETECT in the External status register (bit 25.6) to disable LINK_CONTROL (bit 17.15) for aborting a link with wrong polarity.*

4.8.2 INTERLEAVE_DETECT (bit 25.5)

In the IEEE specification [1], the order of the ternary symbols (An, Bn) is not defined; it may be (An, Bn) or (Bn, An). The receiver is able to correct the order automatically and this bit indicates if this has been done. No action is needed when this bit is set.

4.9 Common configuration register (Address 27)

4.9.1 AUTO_OP (bit 27.15)

When autonomous operation is selected via pin strapping (on pin 21), bit AUTO_OP should be set to 0 if the host needs to take control. Otherwise a conflict may occur.

4.9.2 CLK_MODE (bits 27.13:12)

The clock mode is selected via bits CLK_MODE. A 25 MHz XTAL is expected by default.

The clock mode is valid for both PHY ports; a mixed clocking is not possible.

4.9.3 CLK_HOLD (bit 27.9)

The clock hold function is intended to be used when the PHY provides the clock for another device (e.g. another PHY) via the CLK_IN_OUT pin. When CLK_HOLD = 1, the internal crystal oscilator and the clock signal on CLK_IN_OUT remain active when the PHY core is in Sleep mode. The oscillator (and the clock signal on CLK_IN_OUT) can be switched off by setting bit FORCE_SLEEP in Configuration register 3 to 1.

4.9.4 CONFIG_WAKE (bit 27.6)

The WAKE_IN_OUT pin allows for operation with $V_{DD(IO)}$ or V_{BAT} related wake sources. It is important to adapt the local wake configuration accordingly via CONFIG_WAKE.

4.10 Configuration register 3 (Address 28)

4.10.1 MDI_POL (bit 28.2)

In case the order of the MDI signals as defined in [1] does not match the connector requirements, the polarity can be swapped to prevent crossed routing on the PCB. The change can be made per SMI access. With MDI_POL = 0, the polarity is as given in the pinning table; with MDI_POL = 1 the polarity is swapped. The polarity setting is retained in Sleep mode and will be reset to the default value after a power-on reset or if pin RST_N is pulled LOW.

4.10.2 FORCE_SLEEP (bit 28.1)

When CLK_HOLD = 1, the clock signal remains active even when the PHY core is in Sleep mode. The FORCE_SLEEP parameter is intended to force the device into Sleep mode (with the clock signal disabled).

If the PHY port is switched to Sleep mode manually (without TC10 sleep handshake as described in Section 5.8.1 "Link transition to Sleep"), it is recommended to issue a Standby command followed by a Sleep request command.

4.10.3 PHY_EN (bit 28.0)

If one of the PHY ports is (temporarily) not needed, it can be switched off via PHY_EN. When a port is disabled, it behaves as in Sleep mode but without wake-up capability.

5 Operating modes

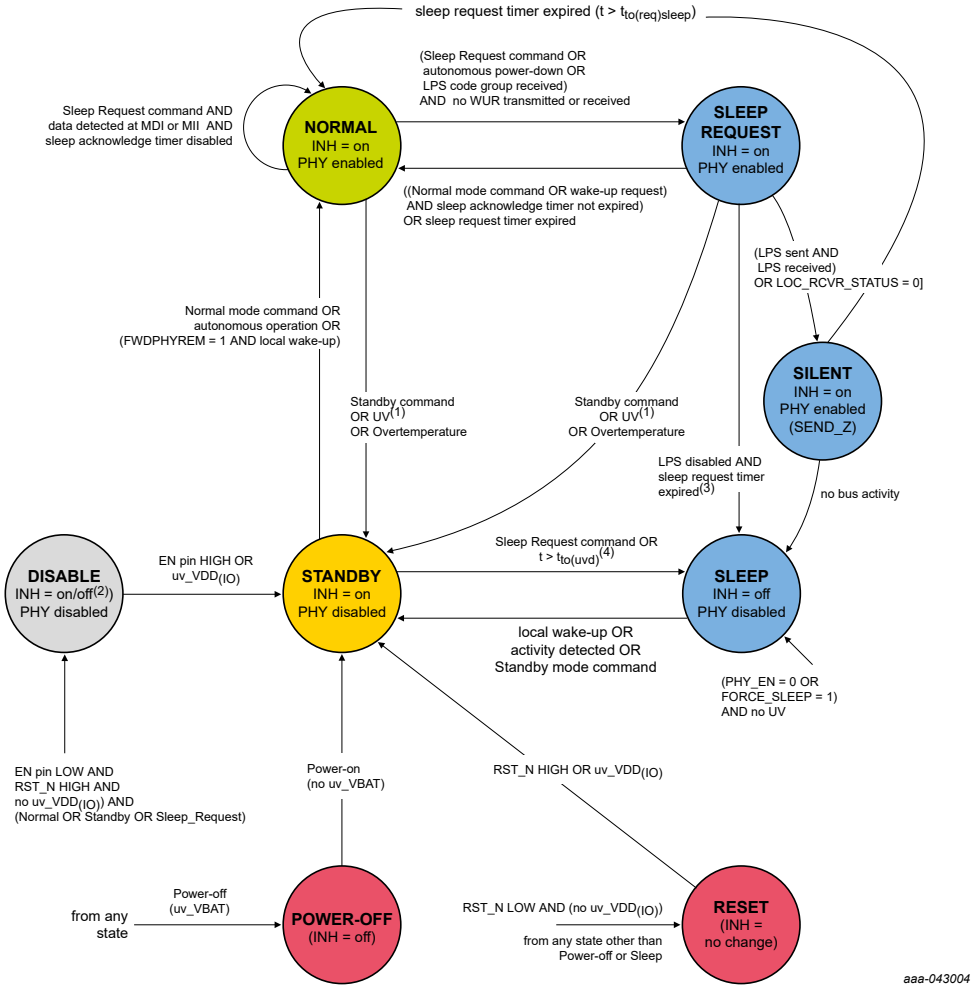
One of the key features of the TJA1101A is the possibility to put a link and the associated node into a Sleep state, while still allowing the node to be woken up in response to activity on the Ethernet bus. In this way, nodes whose functionality is temporarily not needed can be switched to Sleep mode to minimize power consumption.

The mode transition diagram is shown in Figure 20. Abbreviations used in the mode transition diagram are defined in Table 5, with references to the OPEN Alliance TC10 Sleep and Wakeup specification. The three main TJA1101A operating modes are Normal, Standby and Sleep. Sleep Request and Silent modes can be regarded as intermediate states in a transition to Sleep mode. Additional Reset and Disable modes are supported. TJA1101A modes are discussed in more details in the following sections in relation to the TC10 Sleep and Wakeup use case.

Note that operating mode transitions in a port are independent of the other port. The device will be inactive when both PHYs are disabled or in Sleep mode. If the clock signal on CLK_IN_OUT is provided to other devices and needs to continue running when both PHYs are in Sleep mode, the default clock status can be overruled by setting bit CLK_HOLD = 1 (register 27, bit 9). When the clock is no longer needed, setting bit FORCE_SLEEP to 1 (register 28, bit 1) will force the device to system sleep state, disabling the clock.

Table 5. Simplified state diagram legend

Transition	Abbreviation	Description	OPEN TC10
Silent to Normal	sleep request timer expired	$t > t_{to(req)sleep}$	sleep_req_timer_done
Normal to Sleep Request	Sleep Request command	POWER_MODE = 1011	loc_sleep_req = true
	autonomous power-down	no frame transmission or reception for longer than $t_{to(pd)autn}$ AND AUTO_PWD = 1	loc_sleep_req = true
	LPS code group received	LPS_RECEIVED = 1 AND $t > t_{to(req)sleep}$ AND LPS_ACTIVE = 1	loc_recv = true AND en_sleep_cap = true
Sleep Request to Normal	Normal mode command	POWER_MODE = 0011	loc_sleep_abort = true
	wake-up request	(FWDPHYREM = 1 and WAKEUP = 1) OR WUR symbols received at the bus pins	loc_sleep_abort = true
	sleep request timer expired	$t > t_{to(req)sleep}$	sleep_req_timer_done
Sleep Request to Silent	LPS sent	sent out minimum number of LPS to MDI	tx_lps_done = true



1. UV means undervoltage on one of the power supply pins $V_{DD(IO)}$, $V_{DDA(3V3)}$, $V_{DDD(1V8)}$, $V_{DDD(3V3)}$.
2. INH can be configured to be on or off.
3. The PHY will not be in Sleep mode, and cannot be woken up, until the timeout associated with the transition has expired (after $t_{to(req)sleep}$).
4. At power-on, after a transition from Power-off to Standby mode, undervoltage detection timeout is enabled once all supply voltages are available. When an undervoltage is detected, the TJA1101A switches to Sleep mode after $t_{to(uvd)}$.

Figure 20. Mode transition diagram

5.1 Standby mode

After power-on (no undervoltage on V_{BAT}), the TJA1101A enters Standby mode and the INH control output (pin 10) is activated. This battery-related control signal may be used to activate the main supply to the ECU. Once the 3.3 V and the 1.8 V supply voltages are available (1.8 V may be supplied externally or via the internal 1.8 V regulator that will be activated once the 3.3 V supply is available), the PHY is configured according to the pin strapping implemented on the associated configuration and PHY-address pins. No SMI access will take place during this initialization period of max. 2 ms.

From and operating point of view, Standby mode corresponds to the IEEE802.3 Power-Down mode, with transmit and receive functions disabled. Standby mode also acts as

a fail-silent mode and is entered when an undervoltage condition is detected on pin $V_{DDA(3V3)}$, $V_{DDD(3V3)}$, $V_{DDD(1V8)}$ or $V_{DD(IO)}$.

5.2 Normal mode

The TJA1101A must be switched to Normal mode via an SMI command before a communication link can be established. On entering Normal mode, the internal PLL starts running and the transmit and receive functions are enabled. After a stabilization period of 2 ms, the TJA1101A is ready to set up a link. Once bit LINK_CONTROL is set to 1, the PHY configured as Master initiates the training sequence by sending idle pulses. See Section 2.1 "Link startup" for a description of the link startup process.

While this procedure is valid for host-controlled operation (AUTO_OP = 0 in Configuration register 1), for autonomous operation (AUTO_OP = 1) the TJA1101A enters Normal mode automatically on power-on and activates the link.

5.3 Sleep mode

If the ECU or network management in a node decides to withdraw from the network because the functions of the node are temporarily not needed, it may power down the entire ECU while the TJA1101A resides in Sleep mode and remains partly supplied via the battery terminal. In Sleep mode, all internal functions are switched off except for limited SMI operation (all registers can be accessed via an SMI read operation but, with the exception of the POWER_MODE status, the retrieved data is meaningless; the only valid SMI write operation is a Standby mode command; $V_{DD(IO)}$ must be available), the WAKE input and MDI activity detection when enabled.

Releasing the INH output allows the ECU to switch off its main power supply unit. Typically, the entire ECU is powered-down. The TJA1101A is kept partly alive by the permanent battery supply and can still react to activity on the Ethernet lines or WAKE pin. Once Ethernet idle pulses or frames are detected on the lines or there is a HIGH pulse on the WAKE_IN_OUT pin, the TJA1101A wakes up, switching on the main power unit via the INH control signal. As soon as the supply voltages become stable within their operating ranges, the TJA1101A can be switched to Normal mode via an SMI command and the communication link to the partner can be re-established.

Sleep mode can be entered from Normal mode via the intermediate Sleep Request or Silent mode, as well as from Standby mode as shown in Figure 20. Note that the configuration register settings are maintained in Sleep mode.

If CLK_IN_OUT is used to provide the clock for other devices (e.g. other PHYs), the TJA1101A can be configured (CLK_HOLD = 1) to keep the clock and INH on while the PHY core is in Sleep mode. In this situation, the device is not fully in Sleep mode. It can be switched to full Sleep mode by setting FORCE_SLEEP = 1. Note that this command switches the PHY to sleep mode immediately (if it was not already in Sleep mode).

5.4 Sleep Request mode

Sleep Request mode is an intermediate state used to initiate a transition to Sleep mode. In Sleep Request mode, the PHY transmits LPS codes to inform the link partner about the request to enter Sleep mode. The Sleep Request timer starts when the TJA1101A enters Sleep Request mode. If this timer expires before before the link partner has responded, the PHY returns to Normal mode and sets the SLEEP_ABORT bit to indicate that the sleep handshake has failed.

If the transition to Sleep Request mode was trigged by the receipt of an LPS from the link partner, the Sleep acknowledge timer is started to initiate the Sleep ACK phase as per the TC10 standard. It is still possible to return to Normal mode via a host command while this timer is running. The PHY only begins sending LPS codes when the Sleep acknowledge timer has expired.

When the sleep handshake is successful (LPS received and LPS sent), the PHY enters Silent mode.

5.5 Silent mode

Silent mode is an intermediate state between Sleep Request mode and Sleep mode. It is provided to allow time to switch off the transmitter after a sleep request has been accepted before entering Sleep mode. The TJA1101A will switch to Sleep mode once the channel goes silent.

If the channel remains active for longer than $t_{to(req)sleep}$, the PHY returns to Normal mode and a SLEEP_ABORT interrupt is generated.

5.6 Disable mode

When the Ethernet interface is not in use or must be disabled for fail-safe reasons, the PHY can be switched off by pulling pin EN LOW. The PHY, including the internal 1.8 V regulator (if enabled), is switched off completely in Disable mode to minimize power consumption. The configuration register settings are maintained. EN must be forced HIGH to exit Disable mode and activate the PHY. The device will also exit Disable mode if an undervoltage is detected on $V_{DD(IO)}$.

5.7 Reset mode

The device can be completely reset by asserting the active-LOW RST_N pin for at least $t_{det(rst)(max)}$. All registers (including configuration registers) will be reset to their default values. In contrast, a software reset only resets the PHY part of the device.

5.8 Mode transitions

The sleep, wake-up and wake-up forwarding concepts of the TJA1101A are compliant with the OPEN Alliance Wake-Up and Sleep Specification [6]. The OPEN Alliance specification supports a controlled link shutdown to deactivate selective parts of the network, and a global wake-up for an entire Ethernet network. The TJA1101A allows for further customer-specific configuration beyond the OPEN Alliance Wake-Up and Sleep concept. To achieve full OPEN Alliance compliant behavior, the settings in Table 6 are recommended. These settings are assumed for the more detailed discussions on mode transitions in Section 5.8.1 "Link transition to Sleep" to Section 5.8.3 "Wake-up forwarding".

Table 6. OPEN Alliance Sleep/Wake-up configuration

Symbol	Bit	Value
SLEEP_CONFIRM	18.6	1
LPS_WUR_DIS	18.5	0
SLEEP_ACK	18.4	1
LPS_ACTIVE	18.0	1
SLEEP_REQUEST_TO	19[1:0]	11

Note that the TC10 SLEEP_ACK state is realised in the TJA1101A by the sleep acknowledge timer. The TJA1101A Sleep Request mode mirrors the TC10 SLEEP_ACK state while the timer is running.

To simulate the TC10 SLEEP_FAIL state, the device returns to Normal mode and generates a SLEEP_ABORT interrupt to indicate that the sleep handshake had failed.

In case the TC10 sleep/wakeup functionality is not used, it is recommended to disable the functionality by setting relevant bits in the Configuration register 1, as shown in Table 7. If a local wakeup should be used, LOCWUPHY can be used individually to activate WAKE_IN_OUT pin without impact to the MDI communication.

Table 7. Recommended setting if TC10 sleep/wakeup functionality is not used

Symbol	Bit	Value
REMWUPHY	18.11	0
LPS_WUR_DIS	18.5	1
FWDPHYREM	18.2	0
LPS_ACTIVE	18.0	0

5.8.1 Link transition to Sleep

The process involved in switching a link to Sleep mode is illustrated in detail in Figure 21. The 'Sleep' state of a link is expected to be negotiated at network management (NM) level. Once the sleep handshake has been initiated, it cannot be aborted and a new wake-up is only possible from Sleep mode. The NM may observe wake sources and set the system to remain awake in case new requests are received during the handshake.

To initiate the transition to Sleep mode, a Sleep Request is sent to PHY1 via an SMI command (POWER_MODE = 0xB) to start the handshake. PHY1 enters Sleep Request mode, starts the sleep request timer and starts sending LPS codes. The link partner (PHY2) detects these LPS codes and responds by also entering Sleep Request mode

and simultaneously starting the sleep acknowledge and sleep request timers. When the sleep acknowledge timer expires, PHY2 starts sending LPS codes back to PHY1. When PHY1 detects that it has sent and received LPS codes, both PHYs switch to Sleep mode (via an intermediate step through Silent mode).

When the link partner switches to Silent mode, symbol errors may be reported. They should be ignored during the sleep handshake.

If no confirmation LPS codes are received from the link partner before the sleep request timer expires, PHY1 returns to Normal mode and generates a SLEEP_ABORT interrupt. PHY2 returns to Normal mode on receipt of a Normal mode command (POWER_MODE = 0x3), if a wake-up request is received before the sleep acknowledge timer expires, or no LPS codes can be sent before the Sleep Request timer expires. An example of a sleep request being aborted because confirmation LPS codes were not received is shown in Figure 22.

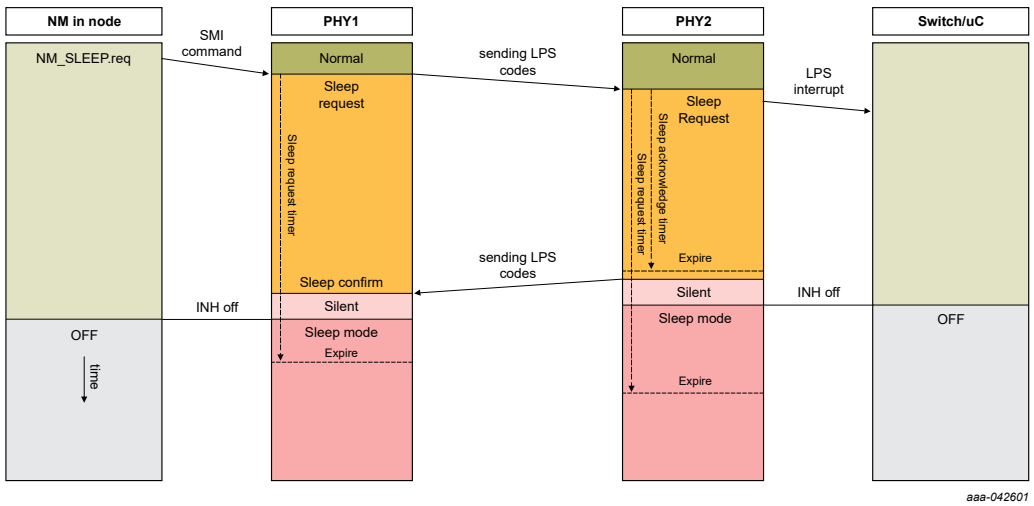


Figure 21. Link transition to Sleep

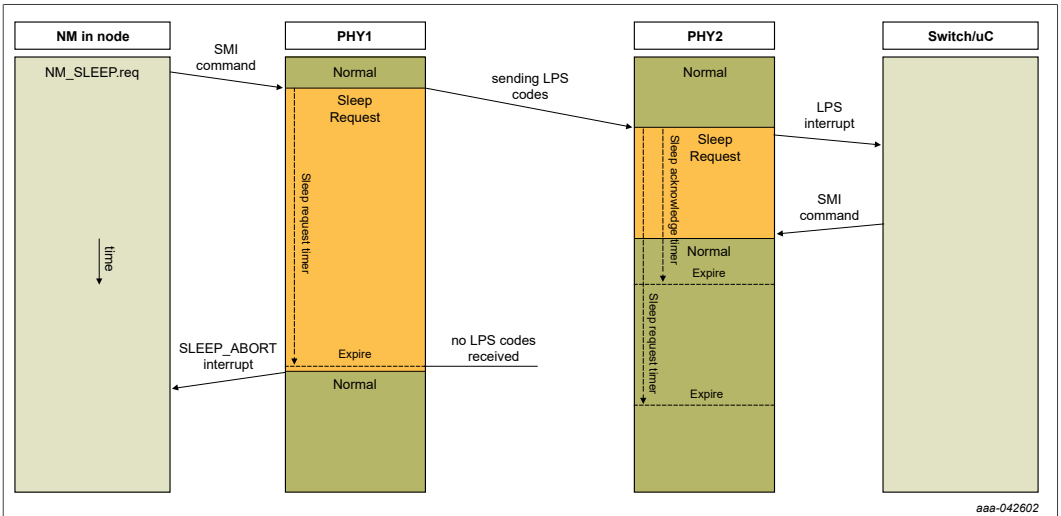


Figure 22. Sleep abort because no LPS confirmation received

5.8.2 Link wake-up from Sleep

The procedure for waking up and reactivating a link from Sleep mode is illustrated in Figure 23. Assume as a starting point that both link partners are in Sleep mode. An end node (here on the left side) may have received a wake-up request from the CAN or LIN interface or a local wake-up, and now requests Ethernet communication. The management software initiates the wake-up process by switching PHY1 to Normal mode and reactivates the link by issuing a wake-up request (WAKE_REQUEST = 1) to the PHY. See Section 4.3.5 "WAKE_REQUEST (bit 17.0)" for further details on using WAKE_REQUEST.

As a result, the PHY starts transmitting a WUP pulse. Note that a training sequence (idle pulses transmitted by a PHY configured as Master when link control is enabled) is also recognized as a WUP pulse. The activity on the twisted-pair lines will be detected by the partner PHY as a remote wake-up, which in turn switches via Standby to Normal mode and activates its ECU via the INH signal. After a software-determined interval, the microcontroller can trigger the training phase by enabling link control (LINK_CONTROL = 1).

A WU interrupt signals a remote wake-up event to the management and the wake-up source can be read from the PHY registers. As soon as the link is ready, signaled by a LINK_UP interrupt, the network management can start with sending NM messages.

Since a dedicated wake-up phase has been introduced, the procedure described is the same whether a Master PHY or Slave PHY initiates the link wake-up.

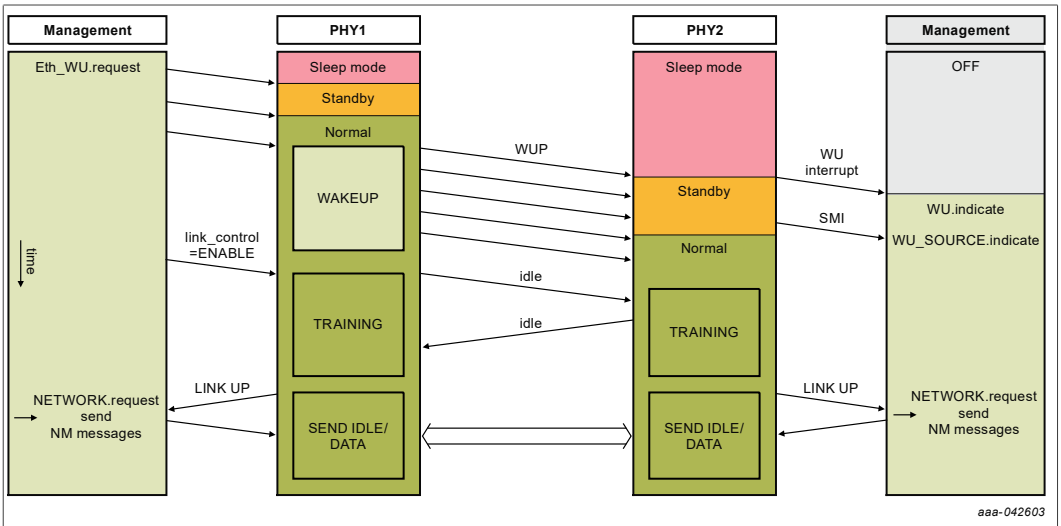


Figure 23. Wake-up from Sleep

5.8.3 Wake-up forwarding

A controlled link shutdown to deactivate selective parts of the network to conserve energy is supported by the OPEN Alliance Wake-Up and Sleep Specification [6]. To avoid impacting the normal operation of ECUs in network, a fast global wake-up is defined in the specification. A wake-up forwarding function without the need for switch, MAC or µC action is also defined to support fast global wake-up.

The wake-up and forwarding behavior of the TJA1101A can be configured. These features are active in Normal, Standby (forwarding only) and Sleep modes. The following

configuration options are available and are selected via Configuration register 1. Note that MDI wake-up is also known as remote wake-up.

- Wake-up in response to a remote wake pattern at the MDI (REMWUPHY)
- Forward an MDI wake-up locally, via the WAKE_IN_OUT pin (FWDPHYLOC)
- Local wake-up via the WAKE_IN_OUT pin (LOCWUPHY)
- Forward a local wake-up via to the MDI via the WAKE_IN_OUT pin (FWDPHYREM)

An example wake-up forwarding procedure is illustrated in Figure 24 and Figure 25. The status of the PHYs, and the connections between them, is shown in Figure 24. The WAKE_IN_OUT pin of PHY2 is configured as a forwarding wake-up output connected to wake_up input pins on PHY3 and PHY5.

It is assumed that all PHYs are configured to react to MDI and local wake-up (REMWUPHY = 1 and LOCWUPHY = 1), and can forward an MDI wake-up locally and a local wake-up to the MDI (FWDPHYLOC = 1 and FWDPHYREM = 1).

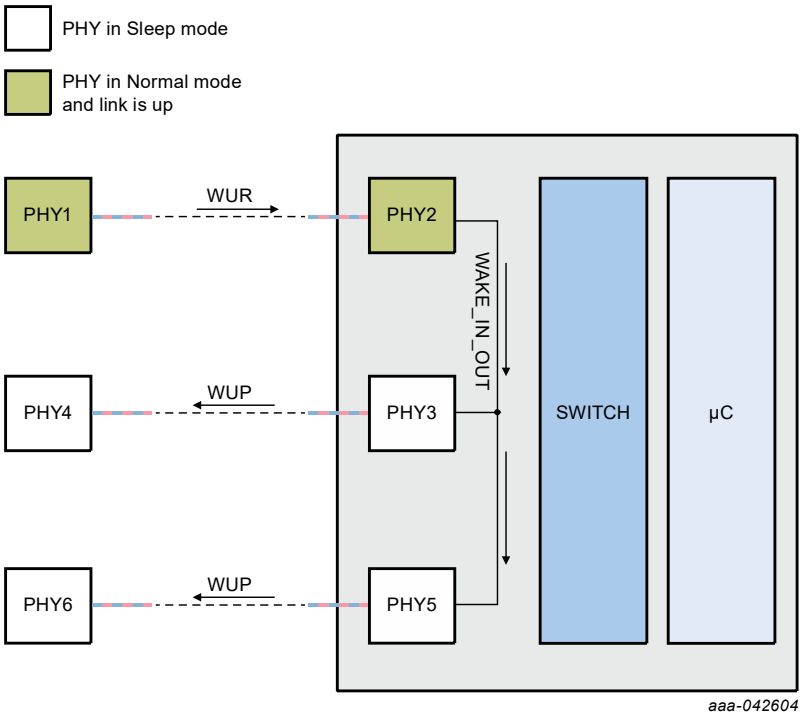


Figure 24. Wake-up forwarding; PHY status and connections

Figure 25 illustrates the following wake-up forwarding procedure:

- Assume that the active node (here PHY1) has received a critical message, and was asked to deliver the message to all Ethernet nodes in the network. The management software initiates the wake-up process by issuing a WUR (wake-up request, WAKE_REQUEST = 1) to PHY1. As a result, PHY1 starts transmitting WUR scrambler code groups over the active link to PHY 2 during idle periods.
  Note that the WUR is encoded in the scrambler stream as defined in the OPEN Alliance Sleep wake-up specification [6].
- PHY2 detects the WUR code stream and interprets it as a remote wake-up request. It responds by forwarding the wake-up request to PHY3 and PHY5 via the WAKE_IN_OUT pin (battery-related open-drain output).

- PHY 3 detects the local wake-up request from PHY2, responds by entering Normal mode via Standby mode, then forwards the wake-up request by transmitting a WUP pulse to PHY4 over the passive link. PHY4 interprets the WUP pulse as a remote wake-up request and responds by waking up.
- In the meantime, PHY5 reacts on the local wake-up request from PHY2 by forwarding it to PHY6 via a WUP pulse over the passive link. PHY6 then wakes up in response to the WUP pulse, interpreted as a remote wake-up request.
- At this stage, all PHYs have been woken up without any intervention from the switch, MAC or µC and a fast global wake-up has been achieved.

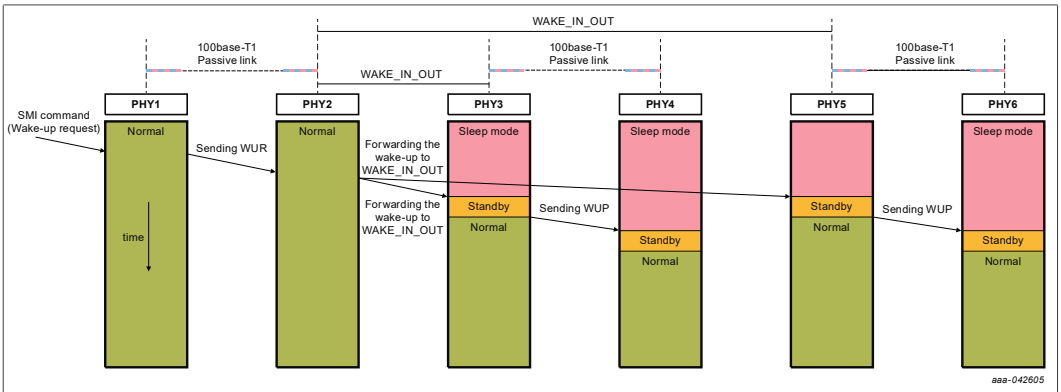


Figure 25. Wake-up forwarding 1

6 Software aspects

6.1 Default register settings for compliance testing

The register settings, which were applied for compliance testing, are documented in the respective compliance test report. The same register settings are also hard coded into the PHY as default configuration.

6.2 Configuration for EMC testing

The register settings, which were applied for EMC testing, are documented in the respective EMC test report. EMC tests are done with MII mode standard driver strength and using a XTAL as clock reference. See Table 8. Using RMII or an external clock requires verification on ECU level.

Using reduced driver strength on short distance MII is expected to improve EMC behavior, but timing behavior should be checked.

Table 8. Configuration for EMC testing

Symbol	Bit	Value
MII_MODE	18.9 to 8	00
MII_DRIVER	18.7	0
CLK_MODE	27.13 to 12	00

6.3 Latching function

In the TJA1101A, some register bits have been implemented with a latching function - indicated by LL (latched LOW) or LH (latched HIGH) in the Access column of the register. When events or fault condition cause these bits to be latched, they will remain set or cleared as appropriate until read or reset, even if the fault/condition has been cleared/ removed. So latched bits need to be read a second time to get an accurate reading of the current status.

Note that latched bits in the Basic and Communication status registers are not latched if link control is disabled (bit LINK_CONTROL = 0).

6.4 Interrupt source register

The Interrupt source register (register 21) is cleared after being read. The interrupt handler must make sure to capture the content of the register after each readout to ensure that, when multiple interrupts are generated, all interrupts get processed.

6.5 Autonomous operation

As described in the datasheet [3], the TJA1101A can be configured to start up and operate independently of the host. If the host controller later takes control, bit AUTO_OP in the Common configuration register must be reset to 0. Otherwise there may be a conflict between autonomous and manual control.

The only exception is for autonomous link startup after wakeup; in this case, AUTO_OP should be set before initiating the sleep request.

6.6 Test modes

According to the OPEN Alliance ECU test specification [5], the ECU must perform several physical layer tests. To enable such tests, the TJA1101A needs to follow defined procedures.

6.6.1 MDI return loss test

Follow these steps to set up the test:

1. Enable configuration register access by setting CONFIG_EN = 1
2. Set the PHY to Normal mode and disable link control (LINK_CONTROL = 0)
3. Configure the PHY as Slave
4. Enable link control (LINK_CONTROL = 1)

MDI return loss test can now be run.

6.6.2 MDI mode conversion loss test

Follow these steps to set up the test:

1. Enable configuration register access by setting CONFIG_EN = 1
2. Set the PHY to Normal mode and disable link control (LINK_CONTROL = 0)
3. Configure the PHY as Slave
4. Enable link control (LINK_CONTROL = 1)

MDI mode conversion loss test can now be run.

6.6.3 Loopback modes

Follow these steps to set up test:

1. Set the PHY to Normal mode and disable link control (LINK_CONTROL = 0)
2. Select loopback mode via bits LOOPBACK_MODE in the Extended control register
3. Enable loopback operation via bit LOOPBACK in the Basic control register (LOOPBACK = 1)
4. Enable link control (LINK_CONTROL = 1)

Loopback operation is now active and can be monitored.

6.6.4 Test modes

Follow these steps to run the test:

1. Set the PHY to Normal mode and disable link control (LINK_CONTROL = 0)
   - For Text mode 4, the PHY should be configured in Master mode
2. Select the required test mode via the Extended control register

The test can now be run.

Signal measurements taken on the MDI interface in test modes 1, 2, 4 and 5 are shown Figure 26 to Figure 29. Channel 1 is TRX_P, channel 2 is TRX_M and the differential signal (TRX_P - TRX_M) is shown in purple. Please note that signals measured using different boards may not be exactly the same, but the pattern will be similar.

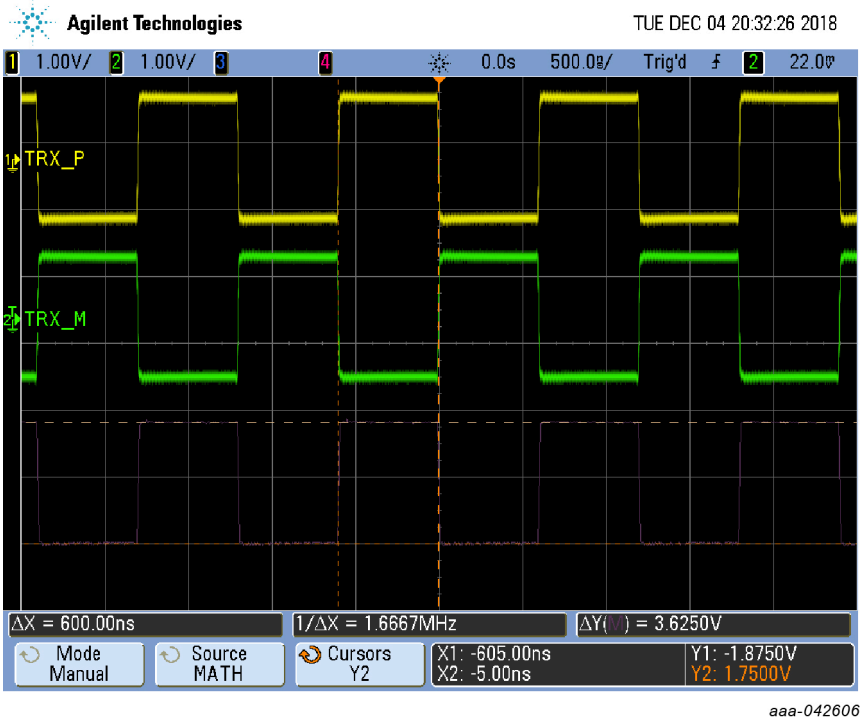


Figure 26. Fig 25. MDI signal measurements: test mode 1

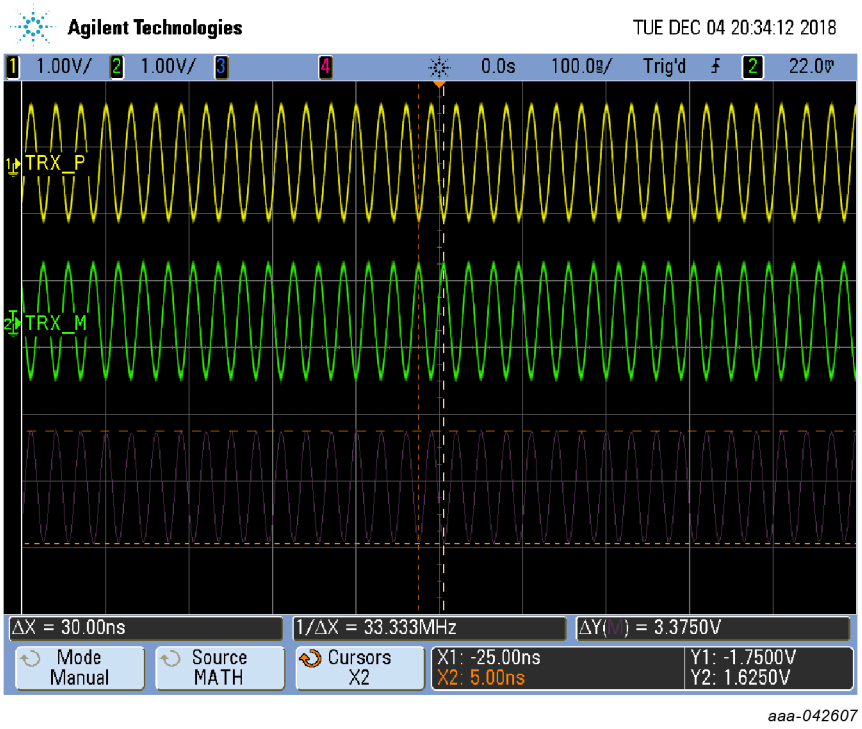


Figure 27. MDI signal measurements: test mode 2

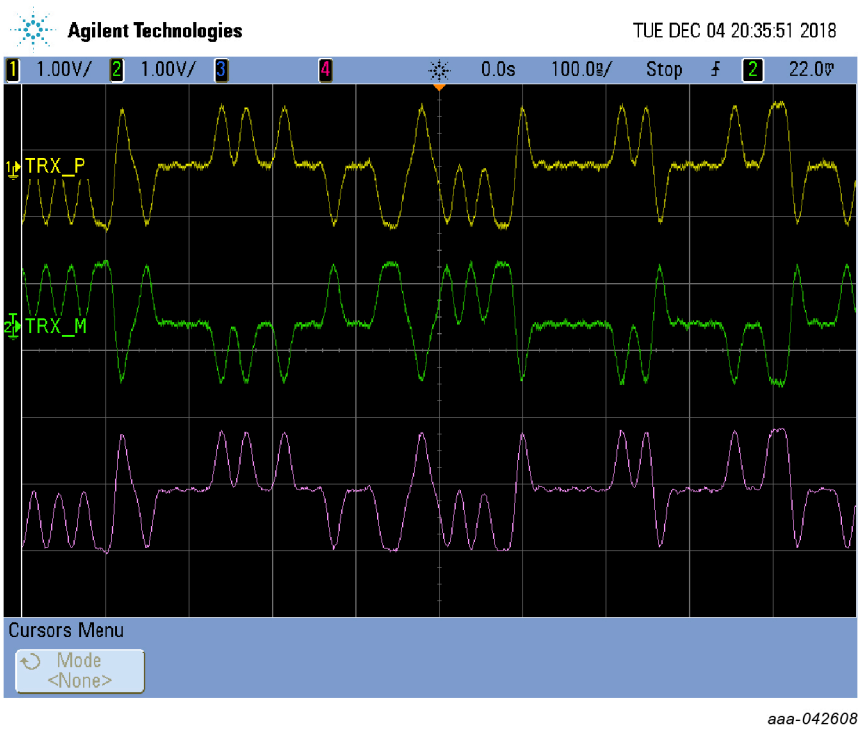


Figure 28. MDI signal measurements: test mode 4

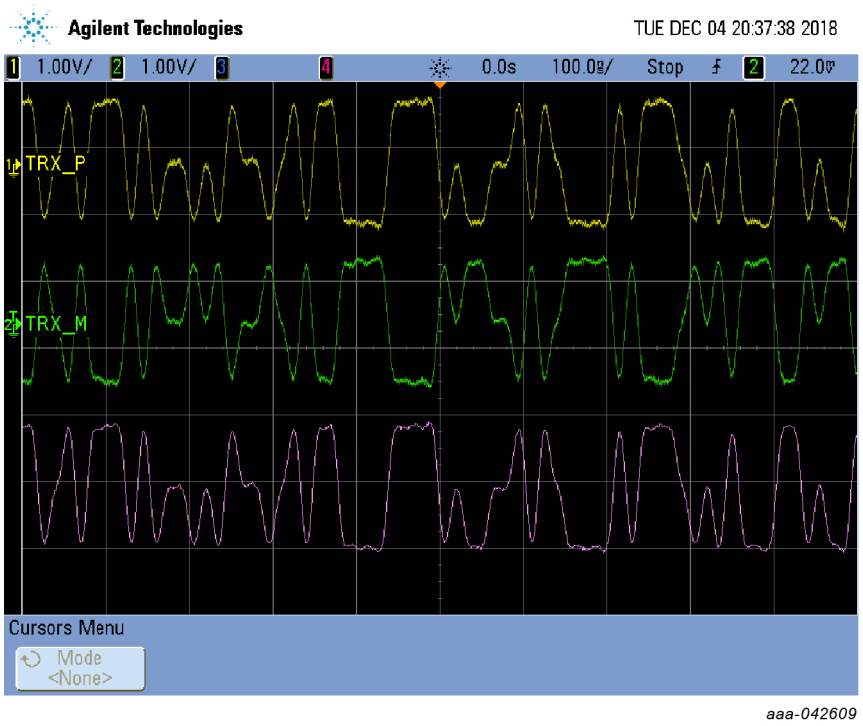


Figure 29. MDI signal measurements: test mode 5

6.6.5 Slave jitter test

Follow these steps to set up the test:

1. Enable configuration register access by setting CONFIG_EN = 1
2. Configure the PHY as Slave
3. Set the PHY to Normal mode and disable link control (LINK_CONTROL = 0)
4. Enable Slave jitter test (SLAVE_JITTER_TEST = 1)
5. Enable link control (LINK_CONTROL = 1)

The slave jitter test can now be run.

6.6.6 Cable test

Follow these steps to run the test:

1. Set the PHY to Normal mode and disable link control (LINK_CONTROL = 0)
2. Start the cable text via the Extended control register (CABLE_TEST = 1)

7 Printed circuit board checklist

Table 9. PCB checklist

Refer also to the PCB design guide [7] for further details.

No.	Pin name	Pin no.	TJA1101A requirement
1	-	-	check pinning
2	P0_RXD3/CONFIG5 P0_RXD2/CONFIG6 P1_RXD3/CONFIG3 P1_RXD2/PHYAD1	1, 2, 34, 35	MII mode: connect to the corresponding RXD3/RXD2 pin on the MAC; a 20 Ω series resistor can be added to improve EMC performance. RMII mode: can be left open
3			The trace length between PHY and MAC should be kept short to ensure a capacitive load of less than 15 pF. If reduced MII output driver strength is used, the capacitive load should be below 7.5 pF. The PCB trace impedance should be at least 50 Ω with a line delay of less than 1 ns.
4	P0_RXD1/CONFIG7 P0_RXD0 P1_RXD1/PHYAD2 P1_RXD0/PHYAD3	3, 4, 36, 37	MII mode: connect to the corresponding RXD1/RXD0 pin on the MAC; a 20 Ω series resistor can be added to improve EMC performance.
5			The trace length between PHY and MAC should be kept short to ensure a capacitive load of less than 15 pF. If reduced MII output driver strength is used, the capacitive load should be below 7.5 pF. The PCB trace impedance should be at least 50 Ω with a line delay of less than 1 ns.
6	P0_RXC/P0_REF_CLK P1_RXC/P1_REF_CLK	5, 38	MII mode: connect to the corresponding RXC pin on the MAC RMII mode: connect to the corresponding REF_CLK pin on the MAC A series resistor can be added to improve EMC performance in MII and RMII modes without an external clock. The impedance of the series resistor plus the output impedance of the clock driver should match the impedance of the PCB trace. A 50 MHz external oscillator (+-50ppm) can be connected to this pin if configured in RMII mode with external clock.
7	$V_{DD(IO)}$	6, 31, 39, 53	The four $V_{DDA(IO)}$ pins should be connected together on the PCB.
8			It is recommended to connect a 100 nF ceramic capacitor between each of the $V_{DD(IO)}$ pins and GND; the capacitors should be located close to the pins.
9			A series ferrite bead (600 Ω ±25 % @100 MHz, e.g. BLM18AG601 SN1) is recommended, and the assembly depends on the EMC results. At least the footprint of the ferrite bead should be reserved. Only one ferrite bead is needed for these pins.
10			The power supplies to the $V_{DDA(3V3)}$ and $V_{DD(IO)}$ pins should be connected to make sure these pins are powered at the same time
11	P0_TXC, P1_TXC	7, 40	MII mode: connect to the corresponding TXC pin on the MAC; a series resistor can be added to improve EMC performance. The impedance of the series resistor plus the output impedance of the clock driver should match the impedance of the PCB trace.
12	P0_TXEN, P1_TXEN	8, 41	connect to the corresponding TXEN pin on the MAC; a 20 Ω series resistor can be added to improve EMC performance.

Table 9. PCB checklist*...continued*

Refer also to the PCB design guide [7] for further details.

No.	Pin name	Pin no.	TJA1101A requirement
13	P0_TXD3, P0_TXD2, P1_TXD3, P1_TXD2	9, 10, 42, 43	MII mode: connect to the corresponding TXD3/TXD2 pin on the MAC; a 20 Ω series resistor can be added to improve EMC performance. RMII mode: can be left open
14			The trace length between PHY and MAC should be kept short to ensure a capacitive load of less than 15 pF. If reduced MII output driver strength is used, the capacitive load should be below 7.5 pF. The PCB trace impedance should be at least 50 Ω with a line delay of less than 1 ns.
15	P0_TXD1, P0_TXD0, P1_TXD1, P1_TXD0	11, 12, 44, 45	MII/RMII mode: connect to the corresponding TXD1/TXD0 pin on the MAC; a 20 Ω series resistor can be added to improve EMC performance.
16			The trace length between PHY and MAC should be kept short to ensure a capacitive load of less than 15 pF. If reduced MII output driver strength is used, the capacitive load should be below 7.5 pF. The PCB trace impedance should be at least 50 Ω with a line delay of less than 1 ns.
17	P0_TXER, P1_TXER	13, 46	MII mode: connect to the corresponding TXER pin on the MAC; should be connected to GND when not used
18	RST_N	14	RST_N should be connected to a GPIO or port pin on the µC. A pull-up resistor of about 10 kΩ to $V_{DD(IO)}$ can be added (but is not essential)
19	SEL_1V8	15	Connect to 3.3 V or GND with a pull-up/down resistor of between 5 kΩ and 20 kΩ. Make sure the input voltage <0.8 V (LOW) or >2.0 V (HIGH).
20	P0_$V_{DDA(TX)}$, P1_$V_{DDA(TX)}$, $V_{DDD(3V3)}$, $V_{DDA(3V3)}$	16, 19, 23, 26, 48, 52	The two P0_$V_{DDA(TX)}$ pins should be connected together on the PCB.
21			The two P1_$V_{DDA(TX)}$ pins should be connected together on the PCB.
22			It is recommended to connect a 220 nF ceramic capacitor between the P0_$V_{DDA(TX)}$ pins and GND - one low-impedance capacitor for two pins or two symmetrical capacitors, one for each pin.
23			It is recommended to connect a 220 nF ceramic capacitor between the P1_$V_{DDA(TX)}$ pins and GND - one low-impedance capacitor for two pins or two symmetrical capacitors, one for each pin.
24			It is recommended to connect a 100 nF ceramic capacitor between the $V_{DDD(3V3)}$ pin and GND.
25			It is recommended to connect a 100 nF ceramic capacitor between the $V_{DDA(3V3)}$ pin and GND.
26			A series ferrite bead (600 Ω ±25 % @100 MHz, e.g. BLM18 AG601SN1) is recommended for the $V_{DDD(3V3)}$, $V_{DDA(3V3)}$ and two P0_$V_{DDA(TX)}$ pins, and the assembly depends on the EMC results. At least the footprint of the ferrite bead should be reserved.

Table 9. PCB checklist...*continued*

Refer also to the PCB design guide [7] for further details.

No.	Pin name	Pin no.	TJA1101A requirement
27			A series ferrite bead (600 Ω ±25 % @100 MHz, e.g. BLM18AG601 SN1) is recommended for the two P1_$V_{DDA(TX)}$ pins, and the assembly depends on the EMC results. At least the footprint of the ferrite bead should be reserved.
28			The capacitors should be located close to the pins.
29			It is recommended to implement a short loop between these pins and GND.
30			It is recommended to connect a 22 µF capacitor at the 3.3 V voltage regulator output. This value only considers the buffering needs of the TJA1101A. A higher value may be needed if the buffering requirements of other 3.3 V loads need to be taken into account.
31	P0_TRX_P P0_TRX_M P1_TRX_P P1_TRX_M	17, 18, 25, 24	See Figure 13 and Figure 14 for recommended circuits.
32			The tolerance of the 100 nF series capacitors should be within 10 % with max rating ≥50 V
33			For reasons of symmetry, the resistors should be ±1 % rated. In order to survive EMI disturbances, an anti-surge rating of at least 0.4 W is needed. Please check details of the implementation with the end customer (OEM). No specific power rating is specified for the 100 kΩ resistor and 4.7 nF capacitor, but components should be 50 V rated.
34			It is recommended to place the ESD diode between the PHY and CMC for greater robustness when needed by the customer.
35			The PCB tracks should be routed close together in a symmetrical arrangement.
36			The recommended impedance of the PCB trace is 100 Ω.
37	WAKE_IN_OUT	20	If this pin is used as a wake-up input, only a rising edge will trigger a local wake-up.
38			If used as a wake-up output, this pin is switched to V_{BAT} level for a time when activated; otherwise it will be floating.
39			If not needed, this pin should be left open or shorted to GND via a series resistor. Local wake-up (LOCWUPHY = 0) and wake forwarding should be disabled (FWDPHYLOC = 0).
40	V_{BAT}	21	This pin can be connected to the battery supply via a reverse polarity protection diode if the wake-up or wake-up function source is needed.
41			This pin can be connected to a 3.3 V power supply instead of a battery supply if the wake-up function is not needed
42			If this pin is connected to a battery supply, it is recommended to connect 100 nF ceramic capacitor and a 1 kΩ series resistor between the pin and GND as a noise filter. The capacitor should have a voltage robustness of 50 V. An optional 1 nF ceramic capacitor can be connected in parallel to improve EMC performance.
43	INH	22	The maximum voltage drop on this pin is 1 V when the output current is 1 mA; double-check the load on the INH pin.

Table 9. PCB checklist...*continued*

Refer also to the PCB design guide [7] for further details.

No.	Pin name	Pin no.	TJA1101A requirement
44			pin can be left open if not used
45	EN	27	This pin is typically connected to a GPIO pin on a µC or permanently connected to $V_{DD(IO)}$.
46	INT_N	28	If connected to the µC, it needs a pull-up resistor of about 10 kΩ to $V_{DD(IO)}$; the pull-up can also be in the µC. The value of the pull-up resistor should be chosen to guarantee a proper HIGH/LOW level.
47			pin can be left open if not used
48	MDIO	29	Connect to MDIO pin on the µC with a pull-up resistor of about 10 kΩ to $V_{DD(IO)}$; the pull-up can be also in the µC. Make sure only one 10 kΩ pull-up resistor is connected to the same MDIO bus.
49	MDC	30	Connect to MDC pin of the µC; a series resistor can be added to improve EMC performance. Note that the impedance of the series resistor plus the output impedance of the MDC driver should match the impedance of the PCB trace.
50			If more than one PHY on the board uses the same MDC clock, PCB branches and stubs used to distribute the MDC clock to multiple PHYs should be as short as possible.
51	P1_RXER/CONFIG1/P0_TXCLK P0_RXER/CONFIG0/P1_TXCLK	32, 55	MII/RMII mode: connect to the corresponding RXER pin on the MAC; a 20 Ω series resistor can be connected to improve EMC performance; pin should be left open if not used.
52			In some test modes, pin P1_RXER reconfigured to output the TX_TCLK clock signal (66.67 MHz) of PHY P0, and pin P0_RXER reconfigured to output the TX_TCLK clock signal (66.67 MHz) of PHY P1. If planning to use the TX_CLK in those test modes, it should be possible to disconnect the pin from the circuit to allow a probe to be connected.
53	P1_RXDV/P1_CRSDV/CONFIG2 P0_RXDV/P0_CRSDV/CONFIG4	33, 56	MII mode: connect to the corresponding RXDV pin on the MAC RMII mode: connect to the corresponding CRSDV pin on the MAC A 20 Ω series resistor can be connected to improve EMC performance.
54	$V_{DDD(1V8)}$	47	It is recommended to connect a 470 nF ceramic capacitor between this pin and GND. The capacitor should be located close to this pin.
55	GND	49	The GND pin should be soldered to board GND with low impedance.
56	XO XI	50, 51	If a 25 MHz external crystal (+-100ppm) is used, it is recommended to connect a ceramic capacitor to XO according to the crystal supplier's recommendations (e.g. 15 pF); this pin can be left open if not used.
57			The 25 MHz crystal should meet the following requirements: tolerance <100 ppm (including all influencing effects), max. ESR: 100 Ω, load capacitance: around 10 pF, drive level: <100 µW.
58			The equivalent load capacitance of the two series capacitors at the XI/XO pins should be ≤8 pF. The max. ESR of the capacitor should be <60 Ω.
59	CLK_IN_OUT	54	When configured as a clock output, a 25 MHz clock signal is available on this pin.

Table 9. PCB checklist...*continued*

Refer also to the PCB design guide [7] for further details.

No.	Pin name	Pin no.	TJA1101A requirement
60			When configured as a clock input, the external 25 MHz clock should be <±100 ppm.
61	CONFIG0 to CONFIG7 PHYAD1 to PHYAD3	55, 32, 33, 34, 56, 1, 2, 3, 35, 36, 37	If pin strapping is used, the pull-up/down resistors should be between 5 kΩ and 20 kΩ. Make sure the input voltage <0.8 V (LOW) or >2.0 V (HIGH).
62	exposed die pad		The exposed die pad should be soldered to GND with low impedance.

8 Abbreviations

Table 10. Abbreviations

Acronym	Description
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
HBM	Human Body Model
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
INH	Inhibit
LPS	Low Power Sleep
MAC	Medium Access Controller
MDI	Medium Dependent Interface
MII	Medium Independent Interface
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PMA	Physical Medium Attachment
RMII	Reduced Medium Independent Interface
SMI	Serial Management Interface
SPI	Serial Peripheral Interface
SQI	Signal Quality Indicator
WU	Wake-up
WUP	Wake-up Pulse
WUR	Wake-up Request

9 References

[1] 802.3bw-2015 - IEEE Standard for Ethernet Amendment 1: Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1), 26th October 2015, IEEE-SA Standards Board

[2] IEEE 100BASE-T1 EMC Test Specification for Common Mode Chokes, Version 1.0, Oct. 2017, OPEN Alliance

[3] TJA1102A - 100BASE-T1 dual/single PHY for automotive Ethernet data sheet

[4] IEEE 100BASE-T1 EMC Test Specification for ESD suppression devices, Version 1.0, Oct. 2017, OPEN Alliance

[5] OPEN Alliance Automotive Ethernet ECU Test Specification, Version 2.0, July 2017, OPEN Alliance

[6] OPEN Alliance Wake-Up and Sleep Specification, Version 2.0, Feb. 2017, OPEN Alliance

[7] AN13335 – PCB design guide for automotive Ethernet

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Tables

Figures

Contents

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