AN13230

Kinetis KW45 and K32W Bluetooth LE Power Consumption Analysis

Rev. 1 — 18 September 2023 Application note

Document Information

Information	Content
Keywords	KW45, K32W1, Low Power, Bluetooth LE
Abstract	This document provides information about the power consumption of Kinetis KW45B41Z and K32W148 wireless MCUs

1 Introduction

This document provides information about the power consumption of Kinetis KW45B41Z and K32W148 wireless MCUs, how the hardware is designed and optimized for low-power operation, and how the software is configured to achieve the best low-power profile. The role of this document is to offer an overview and guidance on achieving the best low-power profile while maintaining the system's high performance. The setup and the procedures to measure the current consumption of the KW45 and K32W1 chips are also described in this document.

The power consumption of wireless devices is a critical requirement for the fast-coming Internet of Things (IoT) world. As a result, the hardware has been gradually improved and optimized from a power consumption perspective, and new communication standards have been developed. Bluetooth Smart (also known as Bluetooth Low Energy or Bluetooth LE) is part of these new standards developed for long-term battery operation, typically for years.

Kinetis KW45 and K32W1 are radio-based MCUs that support the Bluetooth LE v5.2 protocol. The prerequisites for understanding this document are that the reader has good knowledge of the Bluetooth Smart protocol and basic knowledge about Arm MCU architecture and radio communication basics.

2 Acronyms and abbreviations

Table 1 defines the acronyms and abbreviations used in this document.

Table 1. Acronyms and abbreviations

Acronym	Description
ADC	Analog-to-digital converter
ADV	Advertising
Arm	Advanced RISC Machine (RISC – Reduced Instruction Set Computer)
Bluetooth LE	Bluetooth Low-Energy aka Bluetooth Smart
BPSK	Binary Phase-Shift Keying
BTLL	Bluetooth Link-Layer
CMP	Comparator module
DAC	Digital-to-Analog Converter
DC	Direct Current
DSM	Deep Sleep Mode
DUT	Device Under Test
ESR	Equivalent Series Resistance
FRDM	Freedom board
GAP	Generic Access Profile
GFSK	Gaussian Frequency Shift Keying
GPIO	General Purpose Input / Output
IEEE	Institute of Electrical and Electronics Engineers
IoT	Internet of Things
ISM	Industrial Scientific and Medical bands
LE	Low Energy

Table 1. Acronyms and abbreviations...*continued*

Acronym	Description
LL	Link-Layer
LLS	Low-Leakage Stop
LLWU	Low-Leakage Wake-up Unit
LPTMR	Low-power Timer
LPUART	Low-power UART
MBAN	Medical Body Area Network
MCU	Microcontroller Unit
NBU	Narrow Band Unit
O-QPSK	Offset Quadrature Phase Shift Keying
PC	Personal Computer
PDU	Protocol Data Unit
PMC	Power Management Controller
POR	Power-On Reset
RTOS	Real-time Operating Systems
RX	Reception
SAR	Successive Approximation Register ADC
SCGC	System Clock Gating Control register
SIM	System Integration Module
SMPS	Switched Mode Power Supply
SRAM	Static Random Access Memory
TMR	Timer
TSM	Transceiver Sequence Manager
TX	Transmission
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VLLS	Very Low Leakage Stop
XCVR	Transceiver

3 Bluetooth Smart power metrics

The following bullet lists the Bluetooth Smart power metrics.

- KW45-EVK or K32W1-EVK board is used to perform the several current measurements
- Low-power (central and peripheral) reference design application software is used (similar to the temperature sensor in Low-power mode) to set the device in different modes for the current measurements. The revision software used is the SDK PRC2 Release Candidate 2 (RC2) (1st August 2022).
- CM33 (core main power domain) and NBU (core radio power domain) could be active in of the state as follows:
  - Sleep mode

  - Deep sleep mode
  - Power-down mode
  - Deep-power down mode
- CM33 is woken up (core wake-up power domain) and performs system initialization and some pre-processing
- Transceiver Narrow Band Unit (NBU) is woke-up and ready to operate. The CM33 may enter in Inactive mode if the software allows it.
- Transceiver is performing one or more RX / TX sequences
- CM33 is processing the received or transmitted packets
- Transceiver is put back in Sleep mode
- CM33 enters low-power (Deep sleep mode)

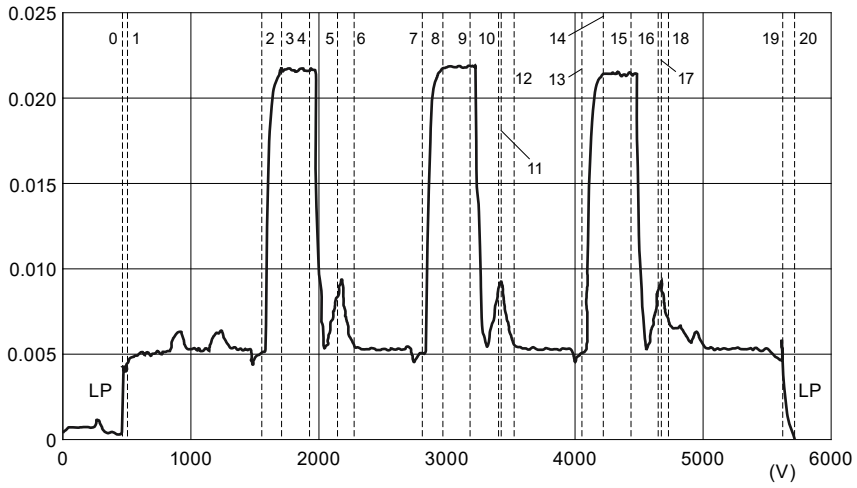

Figure 1. Typical operation cycle of a wireless low-power end device

Figure 1 shows how current consumption, varies over time for each operation cycle of the device.

At power-up, the system performs the so-called power-on reset, and after that it performs the system initialization. On the completion of initialization, the system enters in Low-power mode. There are several Low-power modes available for both MCUs and the radio, but usually the software defines only the most suitable combinations of CM33 and XCVR Low-power modes, for example, Deep-sleep mode for CM33 and NBU.

The timings shown in Figure 1 are explained in Table 2.

Table 2. Timings of a typical low-power device

Event - Peripheral	Event - Peripheral
LP. SoC in Deep Sleep mode	10. TX to RX transition
0. SoC awakes from Deep Sleep mode	11. XCVR Active RX
1. CM33 run: Pre-processing	12. XCVR RX warm down
2. XCVR TX warmup	13. CM33 STOP: RX to TX
3. XCVR Active TX	14. XCVR TX warmup
4. TX to RX transition	15. XCVR Active TX
5. XCVR Active RX	16. TX to RX transition
6. XCVR RX warm down	17. XCVR Active RX
7. CM33 STOP: RX to TX	18. XCVR RX warm down
8. XCVR TX warmup	19. CM33 RUN: Post-processing

Table 2. Timings of a typical low-power device*...continued*

Event - Peripheral	Event - Peripheral
9. XCVR Active TX	20. SoC going to Deep Sleep mode
-	LP. SoC in Deep Sleep mode

The time the transceiver switches from RX to TX is called RX to TX turnaround time, an essential parameter of the transceiver.

When the radio is operational, the CM33 performs various tasks, like serving interrupts or controlling various peripherals. Therefore, the best metric to be applied is current consumption over time, considering the average current of all implied entities.

3.1 Bluetooth Smart (LE)

Bluetooth Smart (Bluetooth Low Energy or Bluetooth LE) is a promising candidate for low-power communication and a good candidate for automotive applications (key fob and anchor) and IoT deployments. Bluetooth LE operates at a 2.4 GHz Industrial Scientific and Medical (ISM) band and uses Gaussian Frequency Shift Keying (GFSK) modulation. The bandwidth bit period product is 0.5, and the modulation index is 0.5 (between 0.45 and 0.55).

Bluetooth LE uses 1 MHz wide, 40 channels, each separated by 2 MHz, or 2 MHz wide channels or long range (S=2 / S=8), three channels for advertising packets, and 37 channels for data exchange. The channels are numbered from 0 to 39.

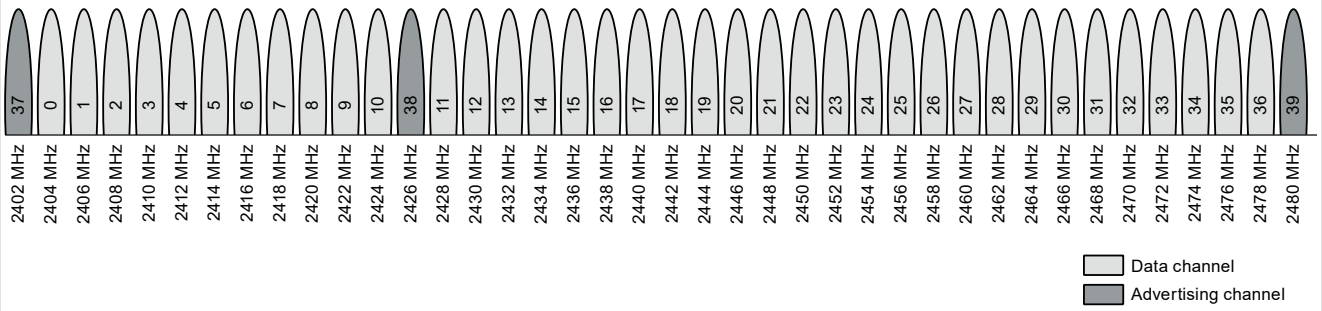

Figure 2. Bluetooth LE radio channels

The low-energy is achieved by having a low-duty cycle of transmission and / or reception of data and by using short advertising and data packets. An asynchronous and connection-less Link-Layer ensures low latency and fast transactions.

At the Generic Access Profile (GAP) layer level, the roles that Bluetooth LE devices may have are GAP central and GAP peripheral. For more details, see Figure 3.

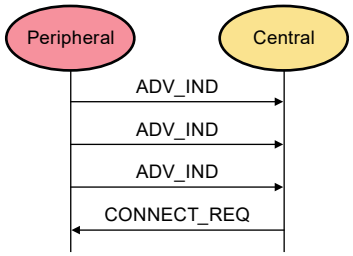

Figure 3. GAP central and GAP peripheral

The peripheral starts sending advertising data to the central. If central is willing to establish a connection with the peripheral, it sends a connection request to the advertiser. Data exchange starts after the connection is established. For more details, see Figure 4.

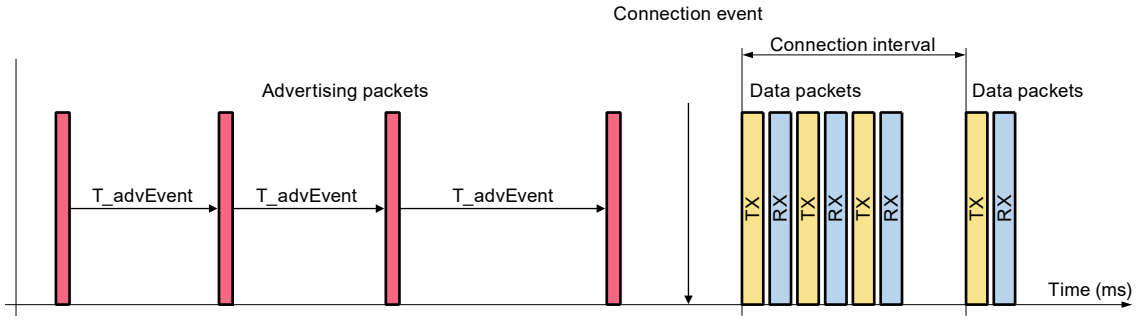

Figure 4. Bluetooth LE advertising and connection events

According to Bluetooth LE specifications, there are four types of advertising packets:

1. `ADV_IND` - Connectable undirected advertising
2. `ADV_DIRECT_IND` - Connectable directed advertising
3. `ADV_NONCONN_IND` - Non-connectable undirected advertising
4. `ADV_SCAN_IND` - Scannable undirected advertising (also known as `ADV_DISCOVER_IND`)

All the above types advertising packets except the non-connectable advertising packets are using a TX followed by an RX sequence, as shown in Figure 5. It is since after sending the advertising packet, the device is waiting for a Scan request or Connect request from a peer device, if any.

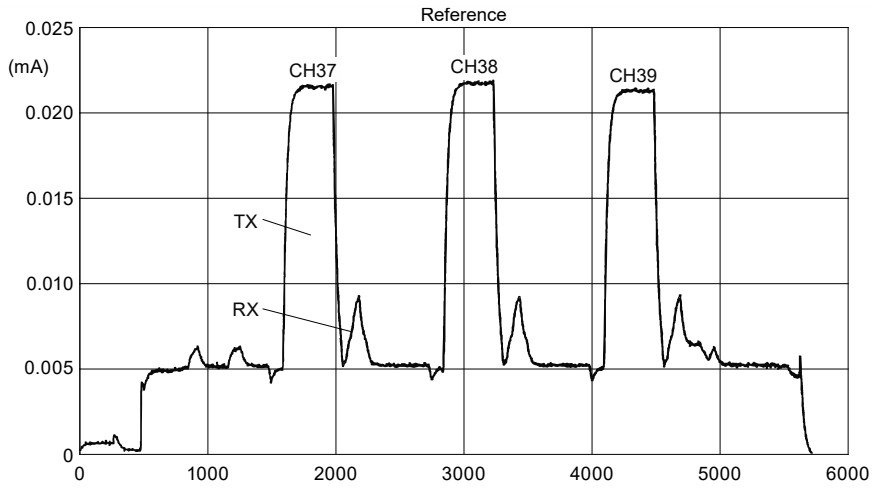

Figure 5. Current consumption vs. time in ADV phase for a Bluetooth LE peripheral device

The current variation with the time when system is in a typical advertising event is shown in Figure 5. All three advertising channels are used. For each channel, a TX operation followed by an RX operation is performed.

Another feature of Bluetooth LE is that the advertising events have a random temporal component, according to Bluetooth LE specifications. For more details, see Figure 6.

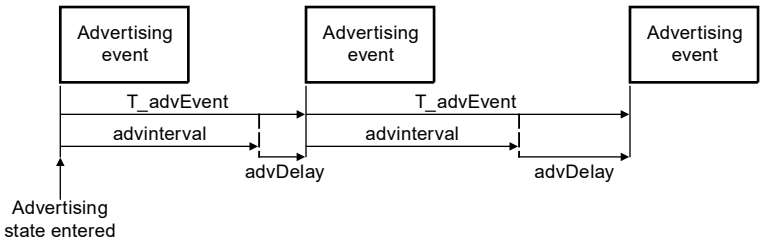

Figure 6. Advertising events occurring at unequal intervals

Equation:

$$T\_advEvent = advInterval + advDelay$$

Where:

- `advInterva`: Integer multiple of 0.625 ms, with a range from 20 ms to 10.24 s
- `advDelay`: Pseudo-random value generated by the Link-Layer, with a range from 0 ms to 10 ms

Therefore, a minimum advertising event interval is 20 ms and a maximum interval is 10.25 s.

Bluetooth LE is designed and implemented for ultra-low power battery operated devices, but the actual power consumption of a real Bluetooth LE device strongly depends on:

- Bluetooth LE application profile
- Application duty cycle
- TX power
- Software management of low-power modes
- Board design and layout

4 Kinetis low-power features

The KW45B41Z and K32W148 (called KW45 throughout this document) are ultra-low power, highly integrated single-chip devices that enable Bluetooth Low Energy (Bluetooth LE - 1 Msps, 2 Msps, 500 ksps (LR S=2), 125 ksps (LR S=8)) version 5.2 and generic FSK (at 250 kbit/s, 500 kbit/s, 1000 kbit/s, and 2000 kbit/s) RF connectivity for portable, extremely low-power embedded systems (Z version) and automotive (A version). KW45 and K32W1 support up to 24 simultaneous Bluetooth LE connections as either a master, a slave, or any combination. The KW45 and K32W1 are designed for applications that center on bridging the embedded world to smartphones to enhance the human interface experience, share-embedded data with the cloud, or enable wireless firmware updates.

Leading the automotive applications is the digital key, where the smartphone can be used as an alternative to the key / smart FOB for unlocking and personalizing the driving experience. But also to provide, select, and authorize access when a key is not needed while sharing your car with others.

The KW45 and K32W1 integrate a Bluetooth LE 5.2 compliant radio transceiver operating in the 2.4 GHz ISM band supporting a range of generic FSK, an Arm Cortex - M3+, Cortex - M33, up to 1 MB Flash and up to 128 kB SRAM, Bluetooth LE Link-Layer hardware and peripherals optimized to meet the requirements of the target applications. The RF section of KW45 is optimized to require very few external components, achieving the smallest RF footprint possible on a printed-circuit board. NXP provides a certified Bluetooth LE stack to support KW45 and K32W1.

Extreme long battery life is achieved through the efficiency of code execution in the Cortex - M3+, Cortex - M33 core and the multiple low-power operating modes of the KW45 and K32W1. Additionally, an integrated DC-DC converter enables a wide operating range from 1.8 V to 3.6 V in Buck mode and 1.8 V to 3.6 V in Bypass mode. The DC-DC in Buck mode allows KW45 and K32W1 to operate from a single coincell battery with a significant

reduction of peak RX and TX current consumption. The DC-DC in Buck mode allows a single alkaline battery to be used throughout its entire useful voltage range of 1.8 V to 3.6 V. The integrated `SYS_LDO` regulator operates from 1.71 V to 3.6 V. Radio analog operates from 1.2 V to 3.6 V. Radio PA operates from 1.1 V to 2.4 V.

4.1 KW45 hardware support for low-power operation

Kinetis KW45 and K32W1 SoC are designed and built with hardware features that allow the chip to operate in various Low-power modes. The features are as follows:

- Multiple CM33 and NBU power modes, including low leakage with memory retention modes
- Bluetooth LE Link-Layer, Deep sleep mode support
- Peripheral modules clock gating
- Several peripheral Doze modes
- DC-to-DC converter
- Transceiver Sequence Manager (TSM) that assures that transceiver analog and digital blocks are not consuming power when no RX / TX sequence is in progress
- Dedicated Power Management Controller (PMC)
- Low-power peripherals (LPTMR, LPUART) that can be configured as wake-up sources to exit a particular low-power state

The software is responsible for configuring all the hardware to achieve the best power scheme required by the applications. As is presented in the following chapters, the chip Low-power modes are combinations of CM33 and LL / Packet processor Deep-sleep modes. The clock gating of peripherals as well as GPIO states before entering Low-power mode, are in charge of the application developer. The connectivity software package provides callbacks that are called before entering Low-power mode and after exiting Low-power mode. The system shall enter Low-power mode when the system is in idle, and all the software layers agree on that. The system shall exit from Low-power mode each time a synchronous or asynchronous event is happening and requires to be processed.

4.1.1 CM33 and NBU Power modes

The PMC module provides various power options to allow the user to optimize and personalize the power consumption regarding the level of functionality that the application requests. Based on Arm architecture power modes, there are four power modes defined as:

1. Sleep mode
2. Deep sleep mode
3. Power-down mode
4. Deep Power-down mode

From the software connectivity perspective, all the following modes could be considered linked to the type of application:

- `DEEP SLEEP 1` mode
- `DEEP SLEEP 2` mode
- `POWER DOWN 1` mode
- `DEEP POWER DOWN 1` mode
- `SMART POWER SWITCH 1` mode

For the details about all the listed power modes, see *KW45B41Z Reference Manual* (document KW45B41ZRM).

4.1.2 Link-Layer Power modes

The Bluetooth Link-Layer (BTLL) has the following power modes available:

- IDLE
- RUN
- DSM

For Bluetooth LE, the connectivity software package implements there are thirteen low-power modes are available for the KW45 and K32W1 SoC, see Table 3:

Table 3. Low-power modes for Bluetooth LE applications

Deep Sleep mode (As defined in Connectivity framework)	Regulators	RAM retention (packet RAM and System RAM CM33)	Core Main Power domain	Core Wake up power domain	Core RF power domain	Peripheral	NBU and Edge Lock	Clock
Deep Sleep 1	all regulators in Low-power mode	All RAM retained in BareMetal	Deep Sleep	Deep Sleep	Deep Sleep	Disabled	Deep Sleep (Disabled)	OSC32K enabled
Deep Sleep 2 (default)	all regulators in Low-power mode	16 kB of RAM retained. All radio RAM retained	Deep Sleep	Deep Sleep	Deep Sleep	Disabled	Disabled	OSC32K enabled
Power Down 1	all regulators in Low-power mode	16KB of RAM retained, All radio RAM retained	Power down	Power down	Power down	Disabled	Disabled	FRO32K enabled
Deep Power Down 1	LDO_ CORE and DC-DC off, LDO_SYS in low power	8 kB of RAM retained, No radio RAM retained	Deep Power Down	Deep Power Down	Deep Power Down	Disabled	Disabled	FRO32K enabled
Smart power switch DPD1	All regulators off	8 kB of RAM retained, No radio RAM retained	Deep Power Down	Deep Power Down	Deep Power Down	Disabled	Disabled	FRO16K enabled

Note: *Bluetooth LE is using a common radio transceiver digital block, the Transceiver Sequence Manager (TSM) that is used to sequence on / off the analog regulators and circuits needed for RX / TX operations so that these circuits only consume power during RX / TX.*

For more details, refer to *KW45K32W1 Connectivity Framework Reference Manual* (document KW45K32W1_CONNFWKRM). To obtain this document, contact your local NXP field applications engineer (FAE) or sales representative.

4.1.3 XCVR Power modes

The KW45 and K32W1 transceiver is coupled with the CM33 and CM3 / NBU. Whenever the CM33 enters Low-power mode, the transceiver analog regulators are powered-off. Depending on the Low-power mode, the digital transceiver logic is power-gated or has its state retained.

4.1.4 DC-to-DC converter

The DC-to-DC module is a Switched Mode Power Supply (SMPS) and has two operational modes:

- Buck: Vin = 1.71 V to 3.6 V
- Bypass: Vin =1.71 V to 3.6 V

The module is configurable through internal registers to operate in Buck mode: `Vdcdc_in` for input and `DCDC_LX` for DC-to-DC output, with CM33 in RUN mode, where peripherals are disabled.

For the detailed information about DC-to-DC converter, see *MKW4xZ/3xZ/3xA/2xZ DC-DC Power Management* (document AN5025).

4.1.5 GPIO, analog pins, and clock gating

A clock gating mechanism was implemented to reduce power dissipation. For example, whenever a peripheral is not used, it can be turned off using the SCGCx registers in the SIM module. Clock gating applies to each peripheral, including the GPIO module. Pruning the clock to a peripheral assures that the internal peripheral circuitry does not have switch states and, therefore, no power consumption, except for the leakage currents.

CAUTION: *After reset, the clock gating bits are cleared, and this implies that before using any peripheral, the corresponding clock gating bit must be set, otherwise, any access to peripheral registers can cause a hardware fault.*

Note: *To turn off a peripheral clock (gate off), the peripheral must be turned off prior to clock.*

The user application must control and set the state of the GPIO ports before the device goes to sleep as well as after the device exits the low-power state. The connectivity software provides callback functions that are called before the device enters a low-power state and after it wakes up.

Related to the analog pins, the device has several analog blocks that have selectable reference voltages. The main blocks are the 16-bit SAR Analog to Digital Converter (ADC) and Comparator Module (CMP). The board design shall consider the chip analog pins and use them appropriately.

The external analog inputs are typically shared with digital I / O. To improve the performance in the presence of noise, or when the source impedance is high, it is recommended to use capacitors on these inputs. The capacitors shall be placed as close as possible to chip analog pins.

For more details, refer to *KW45 Reference Manual* (document KW45RM) and *K32W1480 Reference Manual* (document K32W1480RM).

4.2 Software configuration for low-power operation

This section lists the information about software configuration for low-power operation.

4.2.1 Bluetooth Smart application configuration

The Connectivity Software package offers various Bluetooth LE demo projects. The Low-power (LP) project is used to perform the current profile measurements. This project is available at the following relative path (PRC2 RC2 August 2022):

```
<installation_path><SDK revision>\boards\kw45b41zevk\wireless_examples\reference_
design\bluetooth\lp\bm\iar
```

Or

```
<installation_path><SDK revision>\boards\k32w148evk\wireless_examples\reference_
design\bluetooth\lp\bm\iar
```

To set the device for advertising and connect current measurements, the KW45 or K32W1 SDK includes the Low Power (LP) in the Reference Design application folder (based on a temperature sensor in Low-power mode). It requires some changes to allow the application to enter and leave Low-power mode. BareMetal or FreeRTOS versions of the application are used.

For more information, refer to *KW45/K32W1 Low Power Connectivity Reference Design User's Guide* (document KW45_K32W_LPCDUG) on how to set the different Low-power mode. This document is available in the SDK document package use MCUXpresso SDK Builder to download.

Different built are described in section Section 4.2.1.1 to set the KW45-EVK or K32W1-EVK in different states:

Low-power application:

- Advertising and connection events: (default software setting at +10 dBm)
  - MCU Deep Sleep mode 2, All RAM retained, NBU Deep Sleep mode, RF output power = +10 dBm (default)
- Deep sleep mode 2 (DSM2)

The KW45-EVK or K32W1-EVK board is used to perform the current consumption. It is programmed with the Low-power binary (advertising event and connect events).

Two different ways to flash the board:

- Using embedded MCU link on the EVK by connecting USB cable to a PC
- Using J-Link for Arm as programming/debug tool

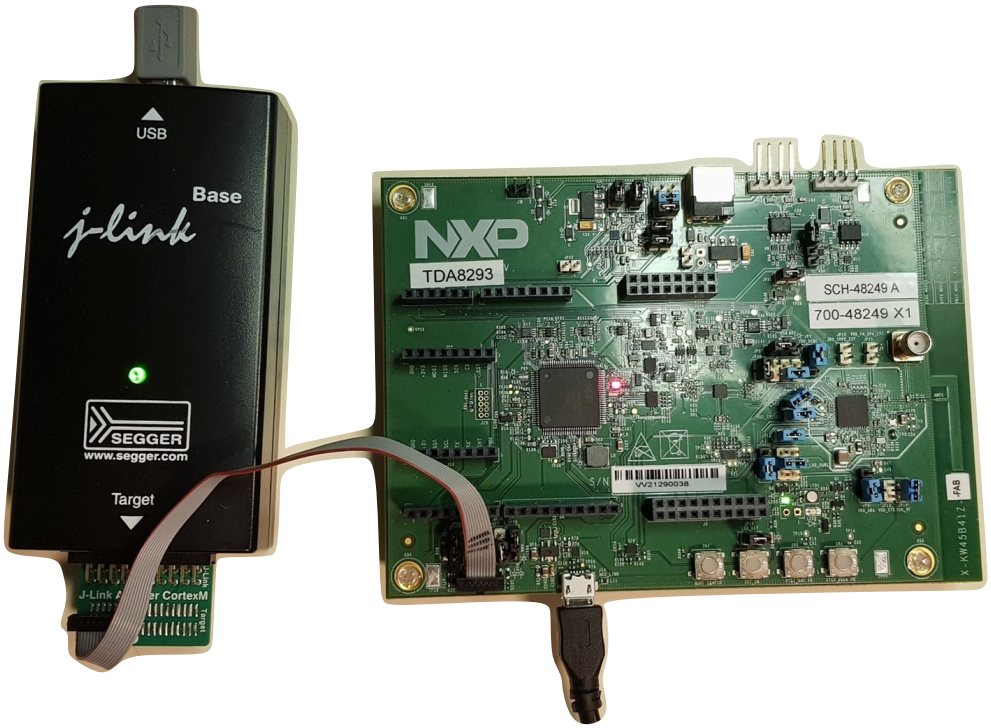

Figure 7. J-Link for Arm programmer / debugger

4.2.1.1 Preparing software

Refer to *KW45/K32W1 Low Power Connectivity Reference Design User's Guide* (document KW45_K32W_LPCDUG) to set all the different modes measured in this report. This document is available in the SDK document package use MCUXpresso SDK Builder to download. For more details, see Table 4.

Table 4. Deep sleep modes available in the SDK software

Deep-sleep mode	Regul.	RAM retention	Core main power domain	Core wake-up power domain	Core RF power domain	Peripherals	NBU and Edge Lock	Clock
Deep Sleep 2	All regulators in Low-power mode	16KB of RAM retained All radio RAM retained	Deep sleep	Deep sleep	Deep sleep	Disabled	Deep sleep (disabled)	OSC32K (enabled)

5 Power measurements and timing analysis

This section lists the details about the following bullet points:

- Setup test environment and DUT
- Measuring the current consumption
- Advertising extension
- Scan extension
- Channel selection algorithm #1 and #2
- High-duty cycle advertising
- Reports

5.1 Setup test environment, Device Under Test (DUT)

This section explains how to set up the testing environment, what hardware tools and boards are needed, and all the steps that must be taken prior to taking measurements.

All the measurements are performed using Keysight:

- Power analyzer: CX3322A
- Current probe: CX1101A

For more details, see Figure 8.

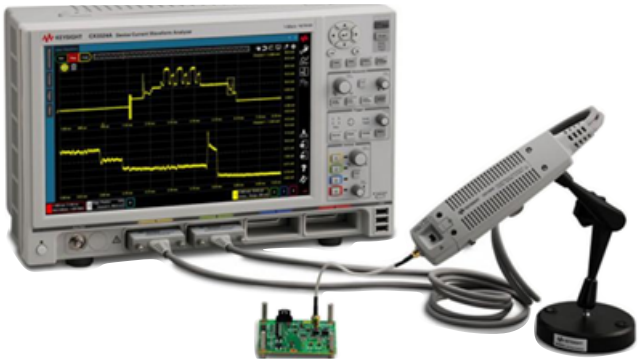

Figure 8. Keysight CX3322A power analyzer and CX1101A current probe

An external source powers the KW45-EVK or K32W1-EVK board, and the power analyzer module 1 is used as an ampere meter. The power source was programmed to deliver 3.6 V DC. One pair of premium cables is needed to supply the board, while the other is needed to measure current. To prevent unintended spikes, power losses, or board resets, the connections between the power analyzer and the EVK board must be flawless. For more details, see Figure 9.

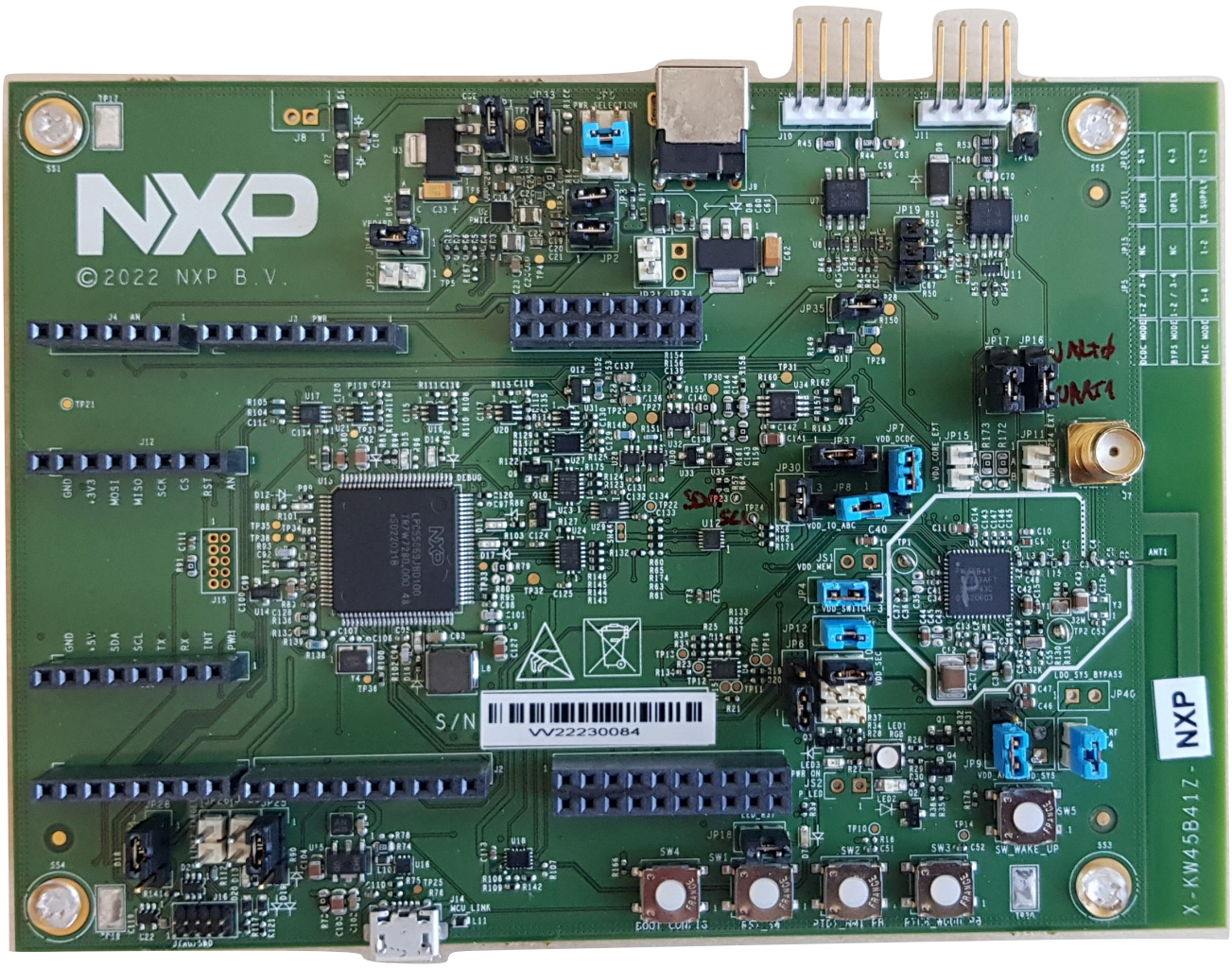

Figure 9. KW45-EVK board

The current measurements are performed in two setup modes using the KW45-EVK or K32W1-EVK board:

- Bypass mode
- Buck modes

For more details, see Table 5, Figure 10, and Figure 11.

Table 5. Header power consumption access points

Current names	Header number
Ireg	JP5:3-4
Idd_LDO_CORE	JP12:1-2
Idd_RF	JP14:1-2
Idd_ANA	JP9:1-2
Idd_dcdc/Idd_IO_D	JP7:1-2
Idd_IO_ABC	JP8:1-2
Idd_Switch	JP4:1-2

Table 5. Header power consumption access points*...continued*

Current names	Header number
Idd_PA_2p4GHz	JP11:1-2

Note: *Ireg = Idd_LDO_Core + Idd_RF + Idd_ANA + Idd_dcdc + Idd_IO_ABC + Idd_Switch + Idd_PA_2p4GHz*

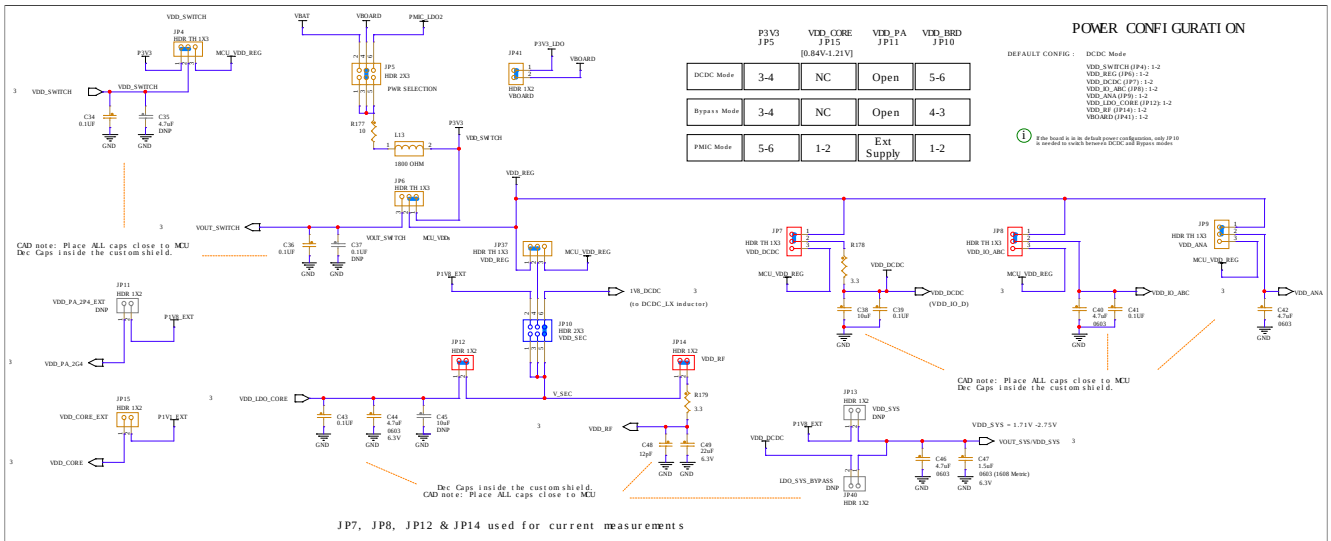

Figure 10. KW45-EVK schematic, current header positions

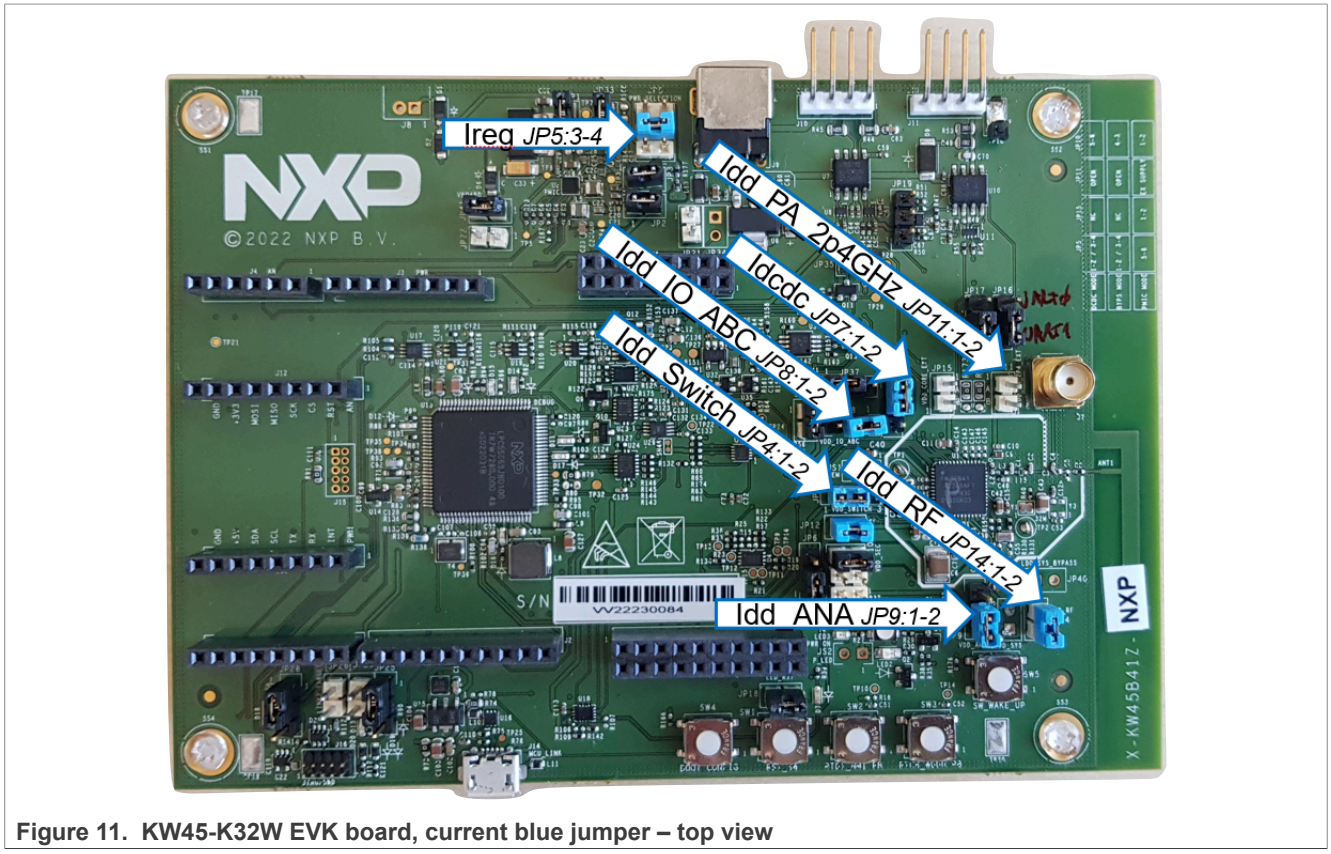

Figure 11. KW45-K32W EVK board, current blue jumper – top view

5.1.1 Preparing hardware

The EVK is set up to prevent the current from peaking below at each Bluetooth Low Energy event stat up. To do this set up, a ferrite bead (BLM15HD182SN1) and a 3.3 ohm serial resistor are attached to the Vbat wire. Both the `Vdd_dcdc` (effective in Buck mode) and the `Vdd_RF` are connected to 3.3 ohm serial resistors, see Figure 12.

These components smooth the current peaks but the general consumption also. That means the shape of the `Ibat` current consumption is not sharp. In case you want to analyze the different steps of the current consumption, you could remove these four components.

In this application note, the measurements and current consumption are done without the serial resistor on advertising, and also in connect events and scan events.

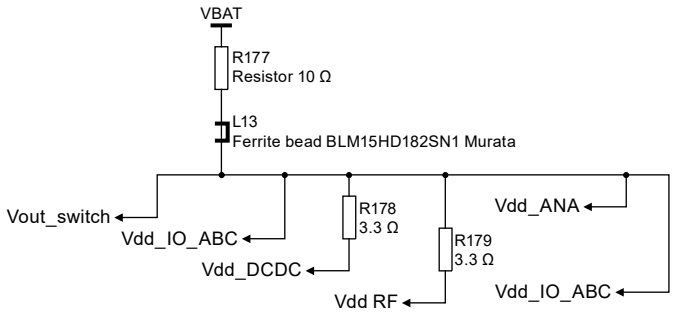

Figure 12. Serial resistors to limit the peak of current

Figure 13 and Figure 14 shows the Ibat waveforms during an advertising event with and without the serial components:

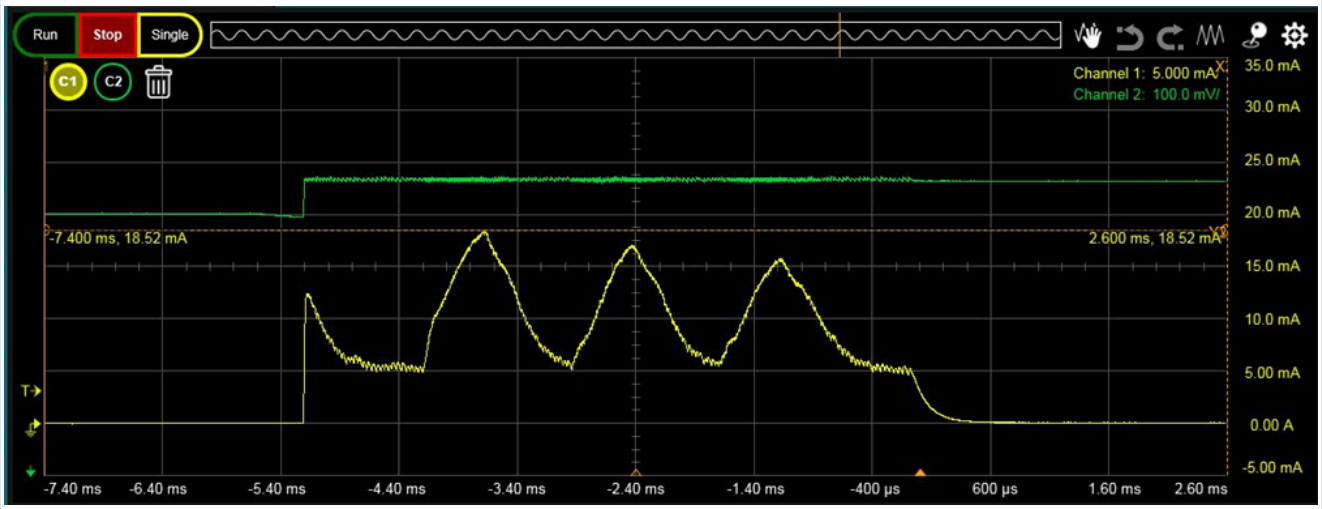

Figure 13. `Ibat` (yellow curve) during advertising event using serial components (default hardware setting)

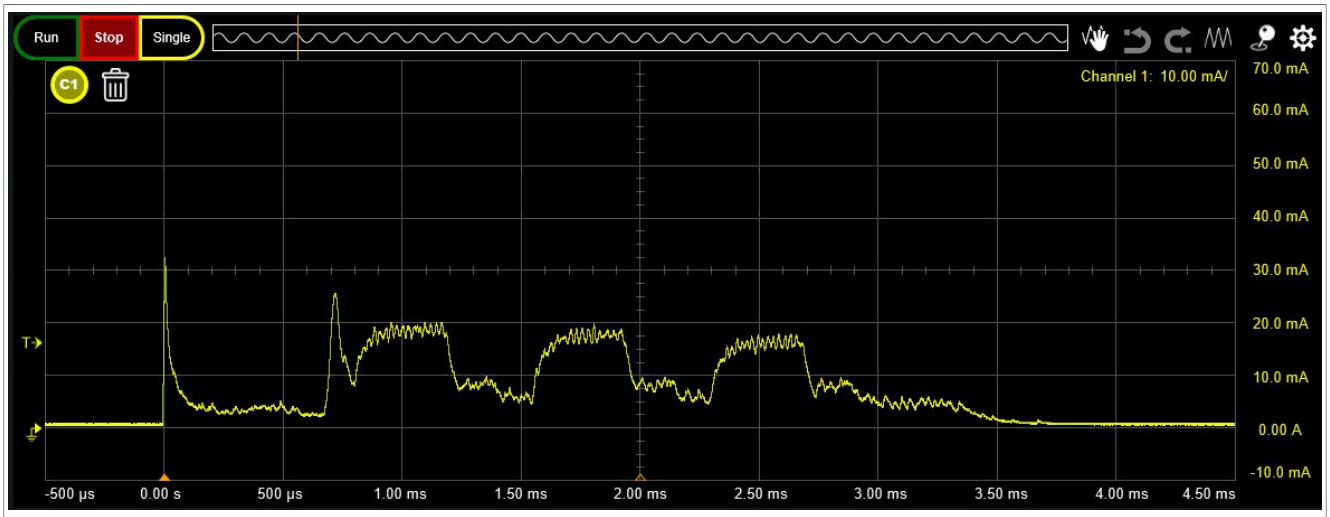

Figure 14. `Ibat` (yellow curve) during advertising event removing serial components (hardware setting used for the current analysis)

5.1.2 Current measurement

The jumpers must be placed as shown in Figure 15 to measure the KW45 or K32W1 current consumption in a selected mode as listed. For the JP10 header supply configuration, see Table 6.

- Jumper `JP10` must be shunt at 1-2 position to allow PMIC mode
- Jumper `JP10` must be shunt at 3-4 position to allow Bypass mode
- Jumper `JP10` must be shunt at 5-6 position to allow Buck mode

Table 6. JP10 header supply configuration (Buck mode, Bypass mode, or PMIC mode)

Supply modes	Header JP10
PMIC	1-2
Bypass	3-4
Buck	5-6

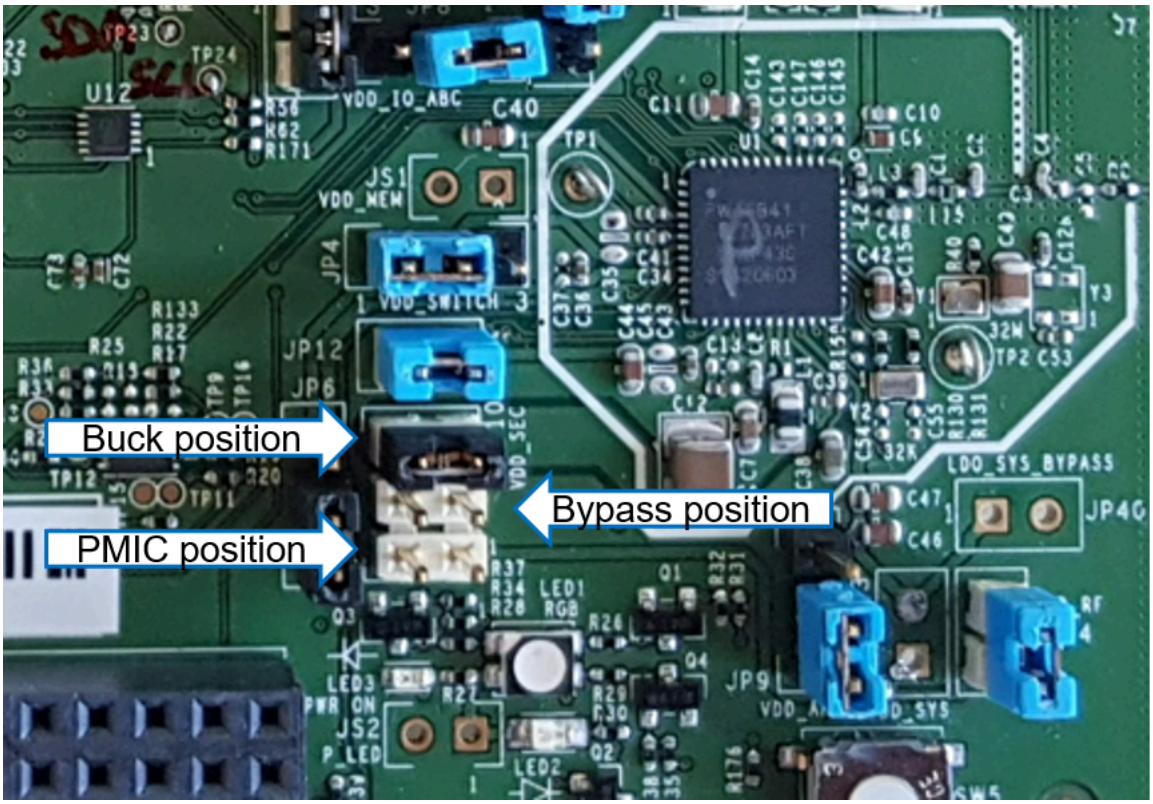

Figure 15. KW45-EVK JP10 header to select Buck mode, Bypass mode, or PMIC mode

5.1.3 `Ireg` current measurement example

Follow the steps as listed to measure the `Ireg` current:

1. Remove the `JP5` jumper
2. Connect the current probe to `JP5-JP3` to measure the global power consumption (`Ireg`) of the KW45 or K32W1
3. Connect current probe in positive polarity to an external power supply
4. Set the external power supply to 3.6 V
5. Supply the KW45-EVK board via the USB connector

For more details, see Figure 16.

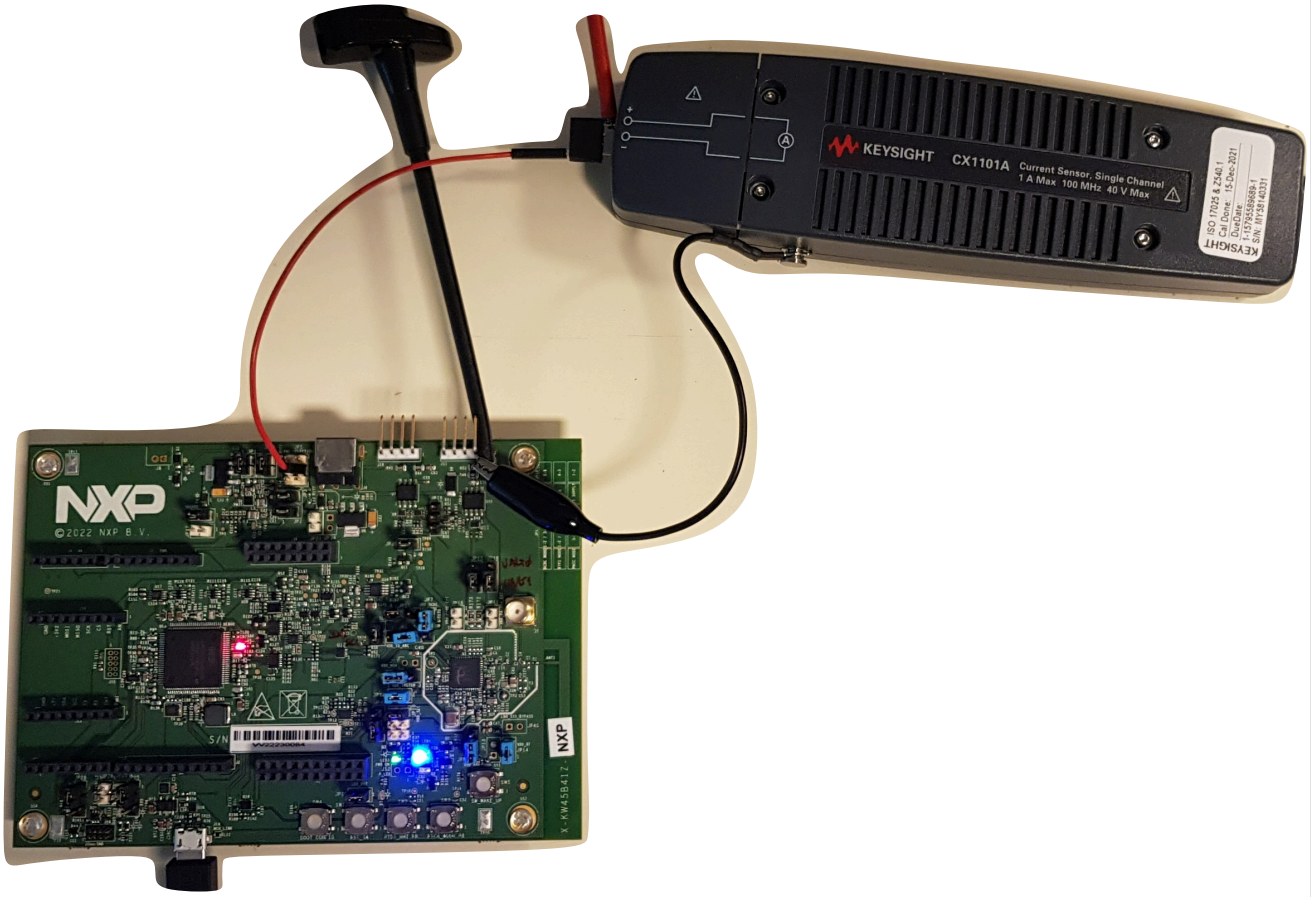

Figure 16. KW45-EVK board, current probe connected to JP5.3 example

If the board has SMA connector, C4 capacitor is populated and C3 not populated, then a SMA antenna is required to be connected to the board, for more details Figure 17.

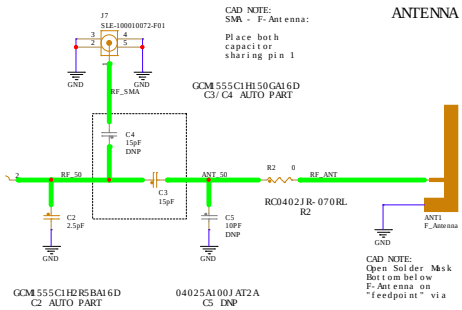

Figure 17. SMA configuration

5.2 Measuring current consumption

This section gives the information to set up the hardware and software to measure current consumption using the KW45-EVK or K32W1-EVK board.

5.2.1 Instruction

Follow the instruction as listed to measure the current consumption:

1. Choose the Buck or Bypass mode, refer Section 5.2.2.3.2 or Section 5.2.2.3.1.
2. Connect the board to a PC and download the `LP_peripheral` (advertising or connect) or `LP_master` (scan) project created as in Section 4.2 to the board.
3. Set the output voltage of the external power source to 3.6 V.
   CAUTION: *Voltage range must be within 1.71 V and 3.6 V.*
4. Connect `TP18` (GND) to the power source, see Figure 18.
   CAUTION: *Ensure that the power source is disabled while connecting the power connector to the board to avoid any damage.*
5. Connect the Keysight CX3322A power analyzer and CX1101A current probe to `JP5-3` and to the power source, Figure 18.
   For more details related to connections, see Figure 19.

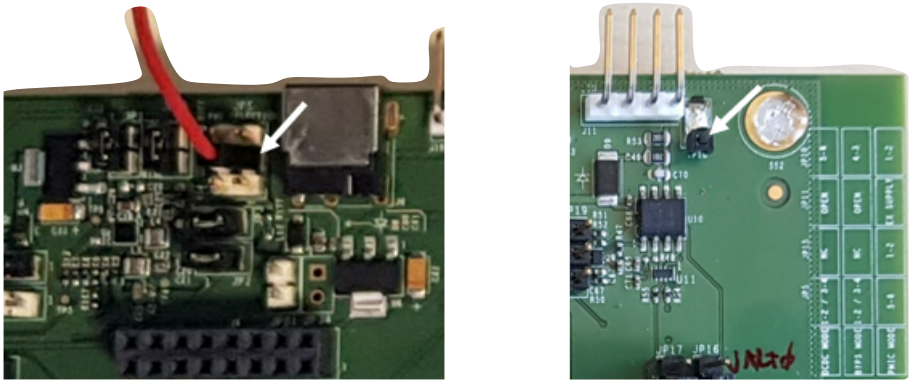

Figure 18. JP5-3, GND TP18

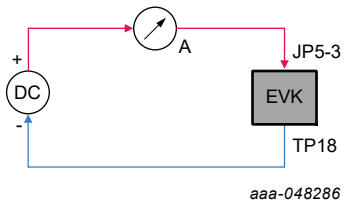

Figure 19. Connection block diagram

6. Apply voltage to the board.

The current measurement is performed by using the power analyzer built-in display and a USB flash memory stick to save the results.

5.2.2 Measurements and results

All the measurements within the following subsection are done with:

- CM33 in Deep Sleep mode
- Flash in Doze mode, RF output at +10 dBm (10 mW), see file `app_preinclude.h`, at `../Connectivitiy_test_bm/source/`).
- Power supplies at 3.6 V
- Room temperature at 25 °C)

KW45 device is coming from a typical process. All the measurement and results are listed in the following subsections. For summary results, see Section 5.7.

Note: *How to use the power analyzer is not explained in this document.*

5.2.2.1 Overview

This section gives an overview of a 20 seconds sequence after a power-up `LP_peripheral` application. For more details, see Figure 20.

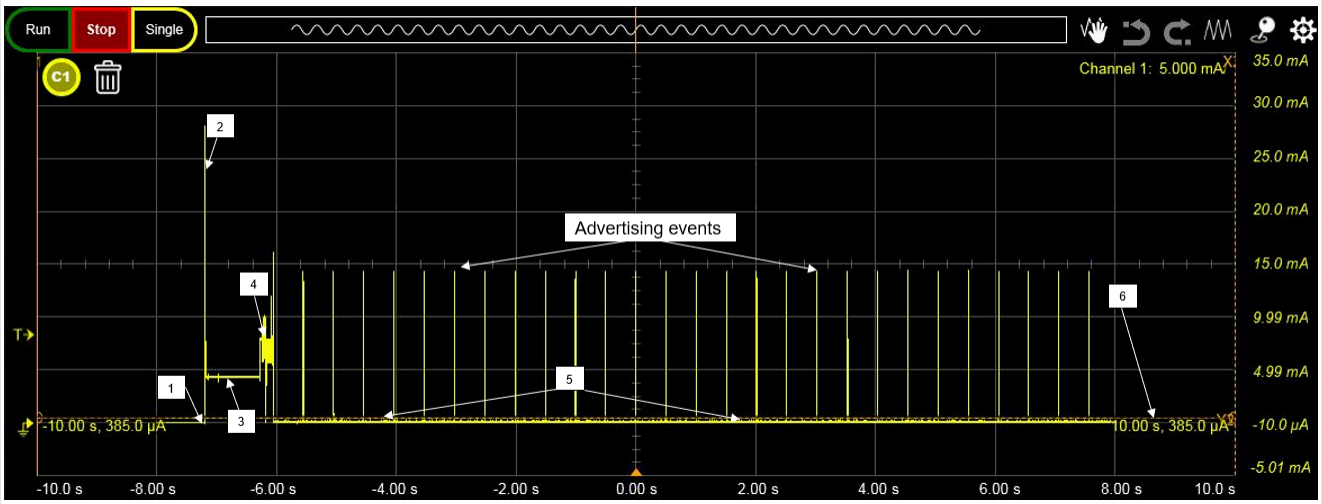

Figure 20. KW45 SoC current consumption sequence

Figure 20 shows the current consumption of the KW45 SoC during different operational phases:

Table 7. Different operational phase current consumption

Phase	Description
1	Power-on reset (POR), just after the SoC is connected to power supply. The spike from the figure is about 26 mA and is because of the coupling capacitors as well as the SoC internal circuitry (regulators, clock oscillators, MCU, radio digital, radio analog, and so on).
2	MCU is initialized among all the software: low-level drivers, framework, RTOS, Bluetooth LE stack, application
3	MCU running
4	The MCU leaves Deep Sleep mode 2 and resumes its execution. The Bluetooth LE Link-Layer goes to RUN state
5	Between advertising events, the system enters in Deep Sleep mode 2
6	After a disconnect, the SoC enters in Deep Sleep mode 2

5.2.2.2 Deep sleep modes

When the SoC is connected to the power supply, a power-up spike occurs due to coupling of the board to power supply. After MCU POR:

- Software execution begins
- Clocks and peripherals are enabled and configured
- Connectivity Framework is initialized
- Real-time operating systems (RTOS) tasks are initialized and started
- Bluetooth LE stack is up and running
- Bluetooth LE application is started

Once all these steps are completed, the system could enters in a different Deep Sleep mode. The default Deep Sleep mode is the `Deep Sleep mode 2` (sorted the list from lowest to highest current consumption). For more details, see Section 4.1.

The initialization phase before the system enters Deep Sleep mode, it takes several milliseconds depending of the Deep Sleep mode chosen.

For the different use cases, the device operates directly in `Deep Sleep mode x`.

5.2.2.3 Power-On reset

The EVK board is set in Buck mode configuration by default.

The binary file setting used is: Buck mode, `Deep Sleep mode 2` for both CM33 and CM3 / NBU with 48 MHz clock mode, automatic start advertising.

The very first POR timing is 900 ms from power-up to first TX advertising. For more details, see Figure 21 and Table 8.

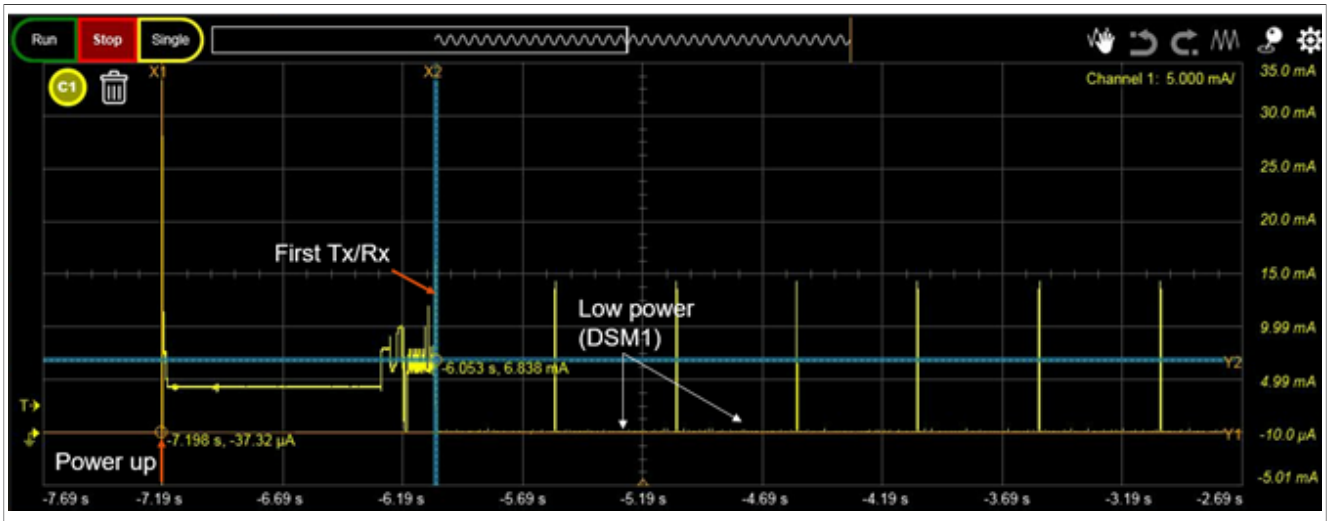

Figure 21. EVK SoC first POR timing

Table 8. POR timing at 900 ms

Type of wake-up	Timing (ms) (HW + SW initialization)
POR	900

The other reset (button pressed / software reset) timings are 108 ms from power-up to first TX advertising, see Figure 22 and Table 9.

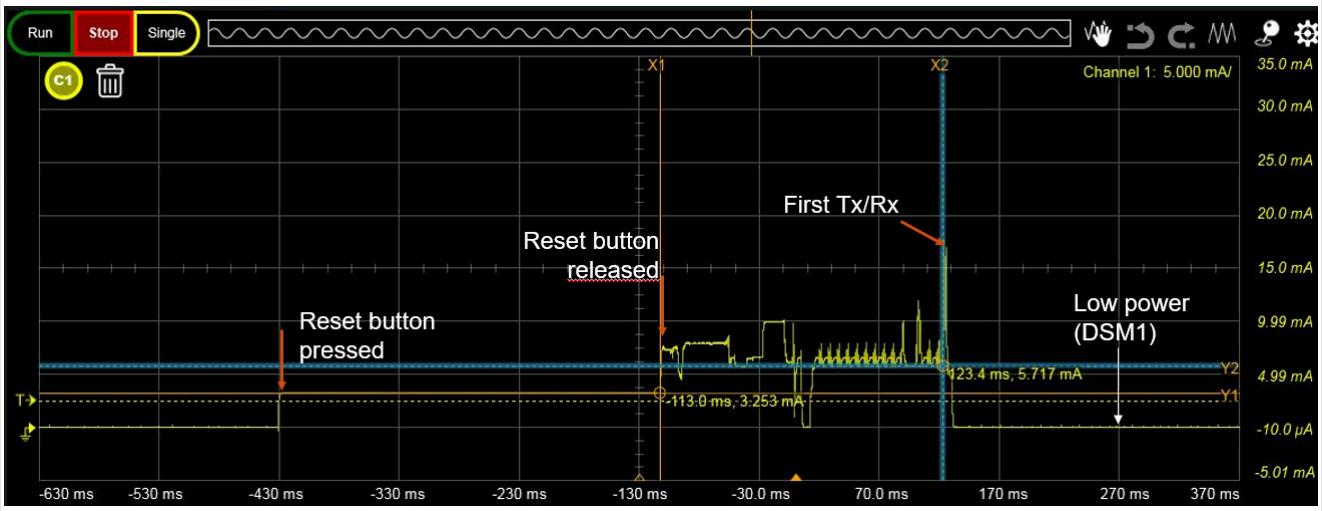

Figure 22. SoC reset timing

Table 9. Reset timings at 108 ms

Type of wake-up	Timing (ms) (HW + SW initialization)	Power consumption (mA) (HW + SW initialization)
First Reset (POR)	900	4.8
Other reset	108	7.65

5.2.2.3.1 Bypass

For the Bypass mode, the `Deep Sleep mode 2` is used where the EVK jumpers are in bypass configuration.

The device enters in `Deep Sleep mode 2` automatically after power-up. The Kinetis device enters in Advertising mode when the `SW1` button is pressed. For more details, see Figure 23 and Table 10.

The binary file setting used as in Bypass mode: `lp_kw45b41zevk_buck.srec`, advertising period 500 ms with payload and connectable.

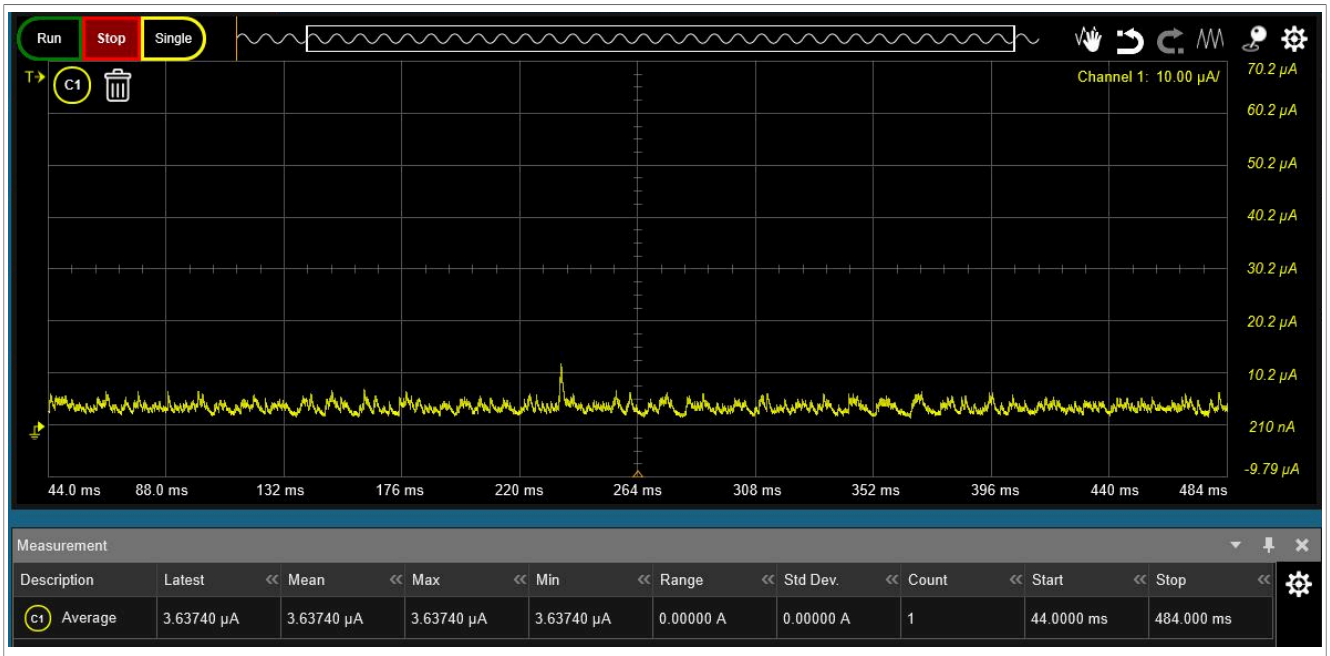

Figure 23. KW45 Deep Sleep mode 2 – Bypass mode

Table 10. Deep Sleep mode 2 current consumption between events in Bypass mode

Measured current			
DCDC_IN=3.0 V	Avg	Max	Min
DCDC_IN=3.0 V	3.6 µA	4.58 µA	2.83 µA

The low-power current consumption is measured 3.6 µA at 3.0 V between advertising events.

5.2.2.3.2 Buck mode

In the Buck mode, the `Deep Sleep mode 2` is used, where the EVK jumpers are in buck configuration.

The device enters in `Deep Sleep mode 2` automatically after power-up. The device enters in Advertising mode when the SW1 button is pressed. For more details, see, Figure 24 and Table 11.

The binary file setting used as in Bypass mode: `lp_kw45b41zevk_bypass.srec`, advertising period 500 ms with payload and connectable.

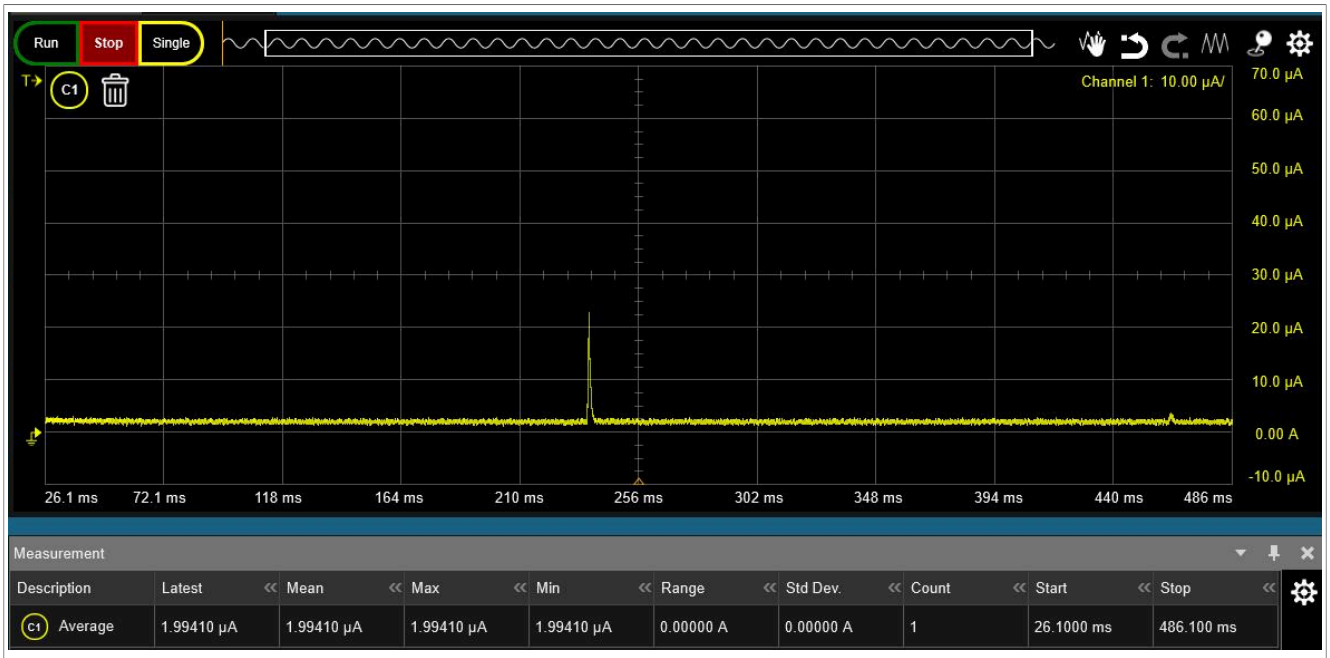

Figure 24. `Deep Sleep mode 2` - Buck mode

Table 11. `Deep Sleep mode 2` current consumption between events in Buck mode

Measured current			
DCDC_IN=3.0 V	**Avg**	**Max**	**Min**
DCDC_IN=3.0 V	1.99 µA	1.72 µA	2.49 µA

The low-power current consumption is measured at 1.99 µA on 3.0 V between advertising events.

For the Low-power summary, see Table 12, Figure 25, and Table 13.

Table 12. `Deep Sleep mode 2` current consumption between events in Buck mode and Bypass modes

Deep sleep mode	Regul.	RAM retention	Core Main Power domain	Core Wake up power domain	Core RF power domain	Peripherals	DC-to-DC	Current consumption at 3 V
Deep sleep 2	all are in Low-power mode	All RAM retained	Deep sleep	Deep sleep	Deep sleep	Disabled	Buck	1.99 µA
Deep sleep 2	all are in Low-power mode	All RAM retained	Deep sleep	Deep sleep	Deep sleep	Disabled	Bypass	3.6 µA

Note: *DC-to-DC peak information in Buck mode, the DC-to-DC peaks occur every 500 ms. The nominal DC-to-DC peak is represented in the below figure. Nominal DC-to-DC peak timing is around 500 us for advertising period of 500 ms.*

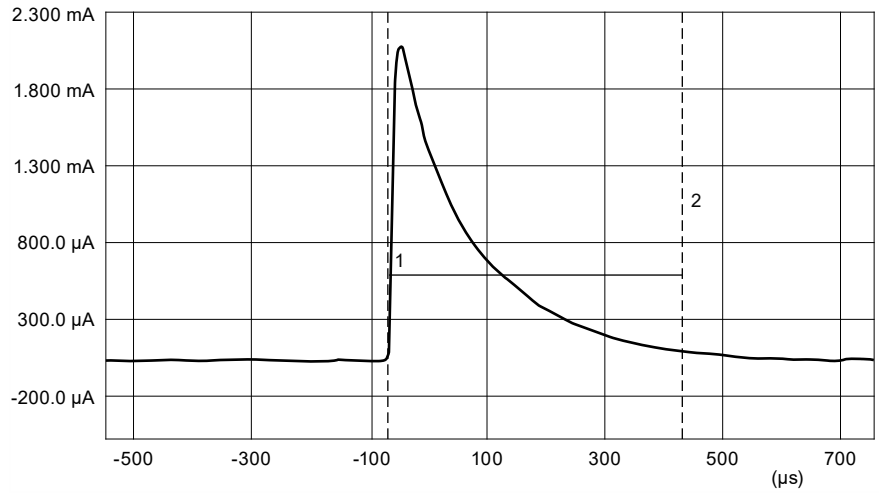

Figure 25. Nominal DC-to-DC peak - Buck mode

Table 13. DC-to-DC peak consumption between advertising events - Buck mode

Buck mode	Idd_REG (total consumption)		
State	Time (ms)	Current (µA)	mA x mS
DC-to-DC peak Consumption	0.500	614	0.307 mA-mS
Charge Integral: 85.27 pAh			

5.2.2.4 Advertising mode

An advertising event is where the Bluetooth LE peripheral device broadcasts some information in order to either share it or become connected to a Bluetooth LE central device, such as a smartphone. The device wakes-up and broadcasts packets on three separate channels and listens on each of these channels for scan requests or connection requests.

Figure 26 and Table 14 shows the current consumption during the advertising event using data rate at 1 Mbit/s and without serial components (setting for coin cells to avoid peak of current).

The binary file settings used are:

- 48 MHz clock
- Advertising with X bytes TX payload, Y bytes RX payload and connectable
- RF output +10 dBm, 1 Mbit/s

Buck mode: Wake-up from Low-power mode `Deep sleep mode 2`

Bypass mode: Wake-up from Low-power mode `Deep sleep mode 2`

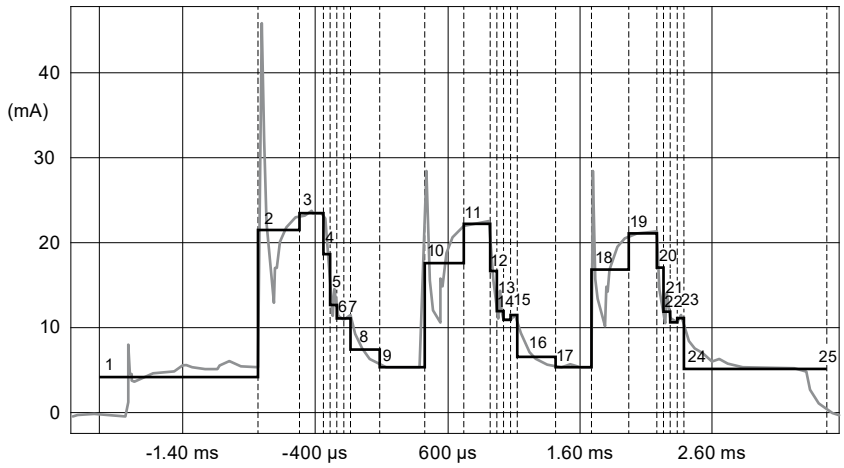

Figure 26. Current consumption - advertising event period

Table 14. Advertising event

No.	ADV event timing
1	Pre-processing
2	TX warm-up
3	Active TX
4	TX warm-down
5	TX to RX transition
6	RX warm-up
7	Active RX
8	RX warm-down
9	MCU stop
10	TX warm-up
11	Active TX
12	TX worm-down
13	TX to RX transition
14	RX warm-up
15	Active RX
16	RX warm-down
17	MCU stop
18	TX warm-up
19	Active TX
20	TX warm-down
21	TX to RX transition
22	RX warm-up
23	Active RX
24	RX warm-down
25	Post-processing

Test environment: Advertising

Table 15. Test environment

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	Vdd_RF = 3 V Vdd_LDO_Core=3 V
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s	
Payload	Tx:31 bytes; Rx:0 Byte	
Connectable	Yes	
Flash	Doze	
CM33	Deep Sleep mode 2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	LP_Peripheral (2.15.2 MR2 release)	

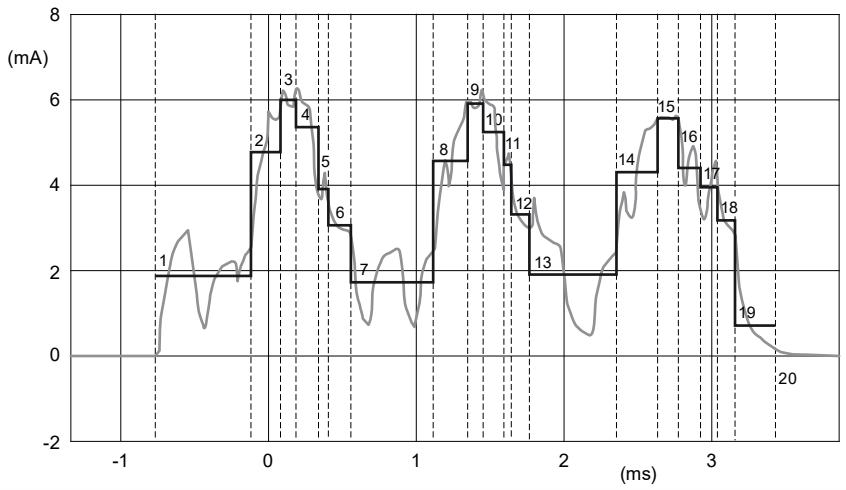

Figure 27. Advertising current profile event after `DSM2` mode, Buck mode

Table 16. Advertising current profile event after `DSM2` mode, Buck mode

Buck mode	`Idd_REG` (total consumption)			Spread: +/- 3sigma
State	**Time (ms)**	**Current (mA)**	**mA x mS**	**-**
Pre-Processing	0.650 ms	2.900 mA	1.885 mA-ms	+/-0.04 mA
TX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
TX1 Level	0.328 ms	6.860 mA	2.250 mA-ms	+/-0.04 mA
TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
TX1 to RX1 Transition	0.050 ms	6.840 mA	0.342 mA-ms	-
RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
RX1 Level	0.080 ms	6.948 mA	0.556 mA-ms	+/-0.08 mA

Table 16. Advertising current profile event after `DSM2` mode, Buck mode*...continued*

Buck mode	`Idd_REG` (total consumption)			Spread: +/- 3sigma
State	**Time (ms)**	**Current (mA)**	**mA x mS**	**-**
RX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
MCU Stop	0.280 ms	1.800 mA	0.503 mA-ms	-
TX2 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
TX2 Level	0.328	6.860 mA	2.250 mA-ms	+/-0.04 mA
TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
TX1 to RX1 Transition	0.050 ms	6.840 mA	0.342 mA-ms	-
RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
RX2 Level	0.080 ms	6.948 mA	0.556 mA-ms	+/-0.08 mA
RX2 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
MCU Stop	0.280 ms	1.800 mA	0.503 mA-ms	-
TX3 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
TX3 Level	0.328 ms	6.860 mA	2.250 mA-ms	+/-0.05 mA
TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
TX1 to RX1 Transition	0.050 ms	6.840 mA	0.342 mA-ms	-
RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
RX3 Level	0.080 ms	6.948 mA	0.556 mA-ms	+/-0.07 mA
RX3 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
Post-Processing	0.275 ms	2.750 mA	0.756 mA-ms	-
Active Consumption	3.458 ms	4.973 mA	**17.195 mA-ms**	+/-0.05 mA
Charge Integral: 4.78 nAh				

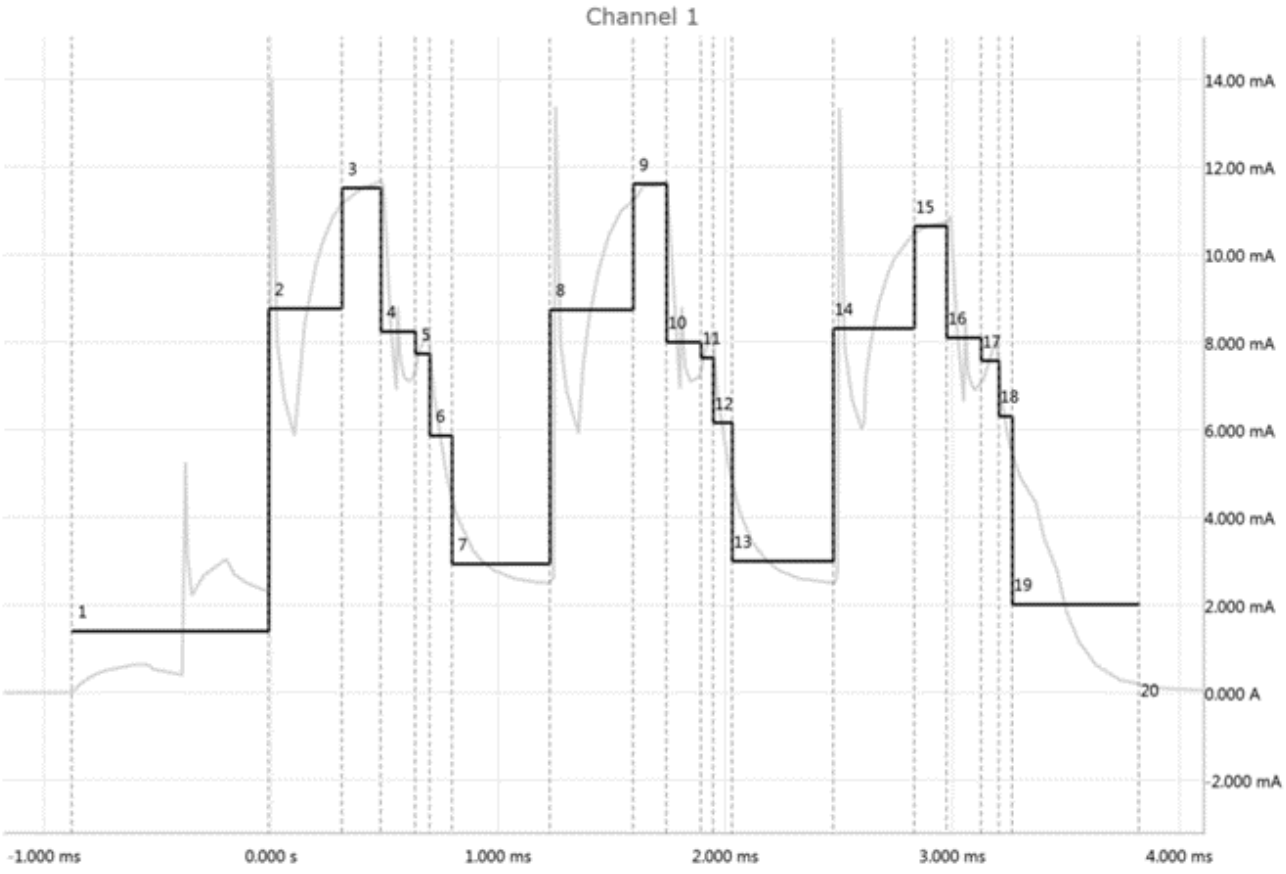

Figure 28. Advertising current profile event after DSM2 mode, bypass mode

Table 17. Advertising current profile event after DSM2 mode, bypass mode

	Bypass mode	Idd_REG (total consumption)			Spread: +/- 3sigma
	State	Time (ms)	Current (mA)	mA x mS	-
ADVERTISING	Pre-Processing	0.900 ms	2.400 mA	2.160 mA-ms	+/-0.29 mA
	TX1 Rise	0.080 ms	3.950 mA	0.316 mA-ms	-
	TX1 Level	0.328 ms	14.401 mA	4.724 mA-ms	+/-0.05 mA
	TX1 Fall	0.020 ms	3.950 mA	0.079 mA-ms	-
	TX1 to RX1 Transition	0.050 ms	3.950 mA	0.198 mA-ms	-
	RX1 Rise	0.080 ms	3.950 mA	0.316 mA-ms	-
	RX1 Level	0.080 ms	14.612 mA	1.169 mA-ms	+/-0.13 mA
	RX1 Fall	0.020 ms	3.950 mA	0.079 mA-ms	-
	MCU Stop	0.280 ms	2.900 mA	0.811 mA-ms	-
	TX2 Rise	0.080 ms	3.950 mA	0.316 mA-ms	-
	TX2 Level	0.328 ms	14.401 mA	4.724 mA-ms	+/-0.07 mA
	TX1 Fall	0.020 ms	3.950 mA	0.079 mA-ms	-
	TX1 to RX1 Transition	0.050 ms	3.950 mA	0.198 mA-ms	-
	RX1 Rise	0.080 ms	3.950 mA	0.316 mA-ms	-

Table 17. Advertising current profile event after DSM2 mode, bypass mode...*continued*

	Bypass mode	Idd_REG (total consumption)			Spread: +/- 3sigma
	RX2 Level	0.080 ms	14.612 mA	1.169 mA-ms	+/-0.17 mA
	RX2 Fall	0.020 ms	3.950 mA	0.079 mA-ms	-
	MCU Stop	0.280 ms	2.900 mA	0.811 mA-ms	-
	TX3 Rise	0.080 ms	3.950 mA	0.316 mA-ms	-
	TX3 Level	0.328 ms	14.401 mA	4.724 mA-ms	+/-0.05 mA
	TX1 Fall	0.020 ms	3.950 mA	0.079 mA-ms	-
	TX1 to RX1 Transition	0.050 ms	3.950 mA	0.198 mA-ms	-
	RX1 Rise	0.080 ms	3.950 mA	0.316 mA-ms	-
	RX3 Level	0.080 ms	14.612 mA	1.169 mA-ms	+/-0.26 mA
	RX3 Fall	0.020 ms	3.950 mA	0.079 mA-ms	-
	Post-Processing	0.560 ms	4.000 mA	2.240 mA-ms	-
	Active Consumption	3.993 ms	6.677 mA	26.661 mA-ms	+/-0.21 mA
	Charge Integral: 7.41 nAh				

Advertising connectable vs non-connectable comparison:

Table 18. Test environment

DC-to DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	Vdd_RF = 3 V Vdd_LDO_Core=3 V
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s	
Payload	Tx:31 bytes; Rx:0 Byte	
Connectable	Yes	
Flash:	Doze	
CM33:	Deep Sleep mode 2	
Setting:	Advertise from low-power DSM2 Slave to Master	
Software:	LP_Peripheral (2.15.2 MR2 release)	

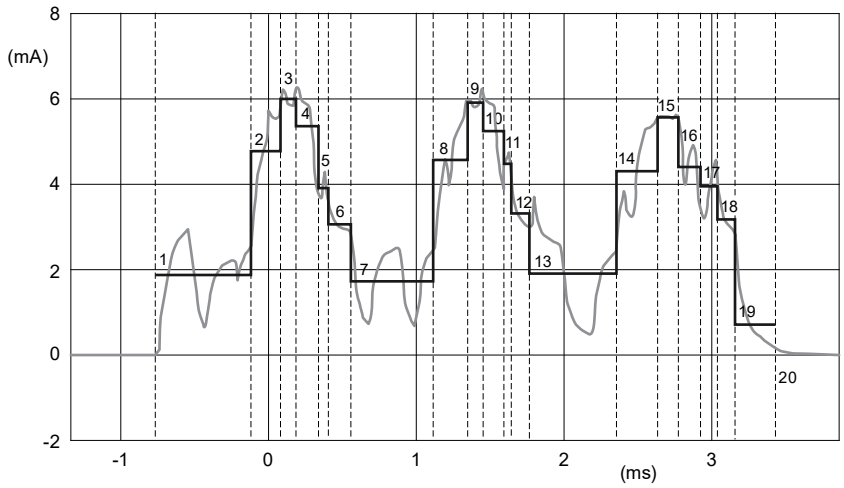

Figure 29. Advertising current profile event after DSM2 mode, buck mode, non connectable

Table 19. Advertising current profile event after DSM2 mode, buck mode, non connectable

	Buck mode	Idd_REG (total consumption)		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADVERTISING non-connectable	Pre-Processing	0.650 ms	2.900 mA	1.885 mA-ms
	TX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	TX1 Level	0.328 ms	6.860 mA	2.250 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	MCU Stop	0.510 ms	1.800 mA	0.917 mA-ms
	TX2 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	TX2 Level	0.328 ms	6.860 mA	2.250 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	MCU Stop	0.510 ms	1.800 mA	0.917 mA-ms
	TX3 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	TX3 Level	0.328 ms	6.860 mA	2.250 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	Post-Processing	0.275 ms	2.750 mA	0.756 mA-ms
	Active Consumption	3.228 ms	5.452 mA	13.278 mA-ms
	Charge Integral:3.69 nAh			

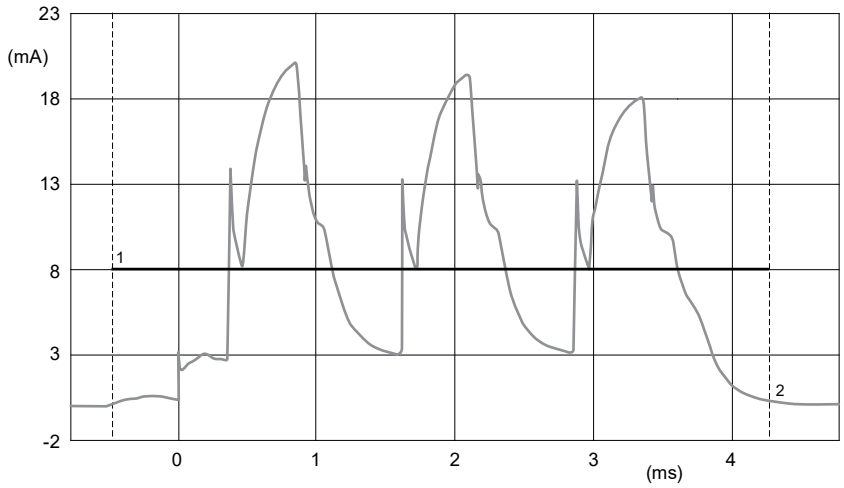

Figure 30. Advertising current profile event after DSM2 mode, bypass mode, non connectable

Table 20. Advertising current profile event after DSM2 mode, bypass mode, non connectable

	Bypass mode	**Idd_REG (total consumption)**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADVERTISING non-connectable	Pre-Processing	0.900 ms	2.400 mA	2.160 mA-ms
	TX1 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX1 Level	0.328 ms	14.401 mA	4.724 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.510 ms	2.900 mA	1.478 mA-ms
	TX2 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX2 Level	0.328 ms	14.401 mA	4.724 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.510 ms	2.900 mA	1.478 mA-ms
	TX3 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX3 Level	0.328 ms	14.401 mA	4.724 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	Post-Processing	0.560 ms	4.000 mA	2.240 mA-ms
	Active Consumption	3.763 ms	10.446 mA	25.546 mA-ms
	Charge Integral: 7.10 nAh			

Advertising connectable power consumption is equal to 4.97mA during 3.46ms (4.78nAh) in buck mode and 6.68mA during 3.99ms (7.41nAh) in bypass mode.

Advertising non connectable power consumption is equal to 5.45mA during 3.23ms (3.69nAh) in buck mode and 10.45mA during 3.76ms (7.10nAh) in bypass mode.

Table 21. Connectable vs non connectable advertising comparison, buck and bypass mode

DC-to-DC mode	connectable	Duration event (ms)	Power consumption (mA)	Total power (nAh)
Buck	No	3.228 ms	5.452 mA	3.69 nAh
Buck	Yes	3.458 ms	4.973 mA	4.78 nAh
Bypass	No	3.763 ms	10.45 mA	7.10 nAh
Bypass	Yes	3.993 ms	6.677 mA	7.41 nAh

Summary:

Table 22. Detailed current profile during advertising event

48 MHz clock using 32KHx Crystal	Buck mode Vdd_dcdc=3 V, Vdd_RF=Vdd_LDO_Core=1.25 V	Bypass mode Vdd_dcdc=Vdd_RF=Vdd_LDO_Core=3 V
	DSM2	DSM2
	T= 25 °C	
Advertising consumption on 1 event at +0 dBm	3.458 ms	3.993 ms
	4.973 mA	6.677 mA
	4.78 nAh	7.41 nAh
Advertising consumption details at +0 dBm		
TX Active (+0 dBm) – MCU STOP	5.060 mA	11.501 mA
RX Active - MCU STOP	5.148 mA	11.712 mA
TX Warm-up - MCU STOP	5.040 mA	10.500 mA
TX Warm-down - MCU STOP	5.040 mA	10.500 mA
RX warm-up - MCU STOP	5.040 mA	10.500 mA
RX warm-down - MCU STOP	5.040 mA	10.500 mA
TX to RX transition - MCU STOP (Advertising event)	5.040 mA	10.500 mA

Table 23. Pre and post-processing timing during advertising

48 MHz clock using 32KHx Crystal	Buck mode Vdd_dcdc=3 V, Vdd_RF=Vdd_LDO_Core=1.25 V	Bypass mode Vdd_dcdc=Vdd_RF=Vdd_LDO_Core=3 V
	DSM2	
	T= 25 °C	
ADV Pre-processing Time	0.650 ms	0.900 ms
ADV Postprocessing Time	0.275 ms	0.560 ms

Table 24. Pre and post-processing and MCU consumption during advertising

48 MHz clock using 32KHx Crystal	Buck mode Vdd_dcdc=3 V, Vdd_RF=Vdd_LDO_Core=1.25 V	Bypass mode Vdd_dcdc=Vdd_RF=Vdd_LDO_Core=3 V
	DSM2	
	T= 25 °C	
ADV pre-processing	2.900 mA	2.400 mA
Radio Post-processing	2.750 mA	4.000 mA
MCU STOP	1.800 mA	2.900 mA

Table 25. Advertising current consumption event

Advertising	Duration (ms)	power consumption (mA)	Energy (nAh)
Buck mode Vdd_dcdc=3 V, Vdd_RF=Vdd_LDO_Core=1.25 V	3.458 ms	4.973 mA	4.78 nAh
Bypass mode Vdd_dcdc=Vdd_RF=Vdd_LDO_Core=3 V	3.993 ms	6.677 mA	7.41 nAh

5.2.2.5 LDO_CORE consumption

LDO_CORE consumption measurement is performed by placing the current probe on jumper JP12. The power supply is always applied via the USB connected to a PC, see Figure 31 and Table 26.

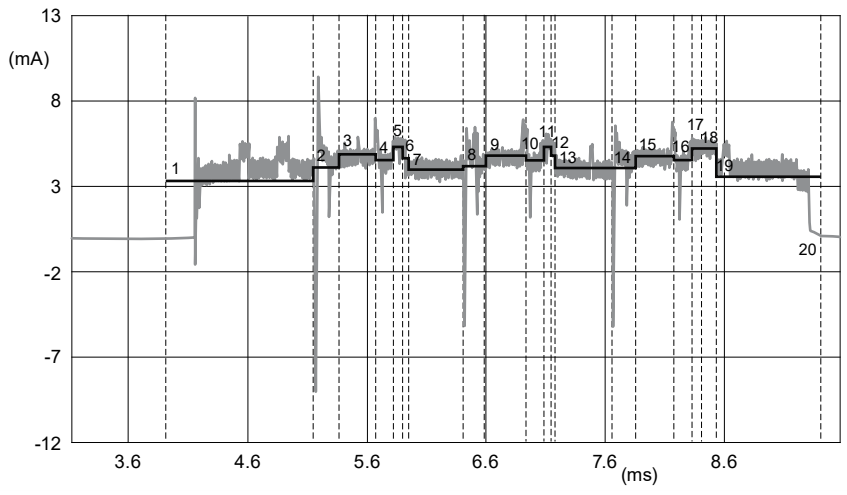

Figure 31. LDO_Core current consumption

Table 26. Event

No.	Adv event timing
1	Pre-processing
2	TX warm-up
3	Active TX
4	TX to RX transition
5	Active RX

Table 26. Event*...continued*

No.	Adv event timing
6	RX warm-down
7	MCU stop
8	TX warm-up
9	Active TX
10	TX to RX transition
11	Active RX
12	RX warm-down
13	MCU stop
14	TX warm-up
15	Active TX
16	TX to RX transition
17	Active RX
18	RX warm-down
19	Post-processing

Figure 31 shows the `LDO_Core` current consumption during the advertising event.

The binary file settings used are:

- 48 MHz clock
- Advertising with X bytes TX payload, Y bytes RX payload and connectable
- RF output +10 dBm

Buck mode: Wake-up from low-power mode `Deep Sleep mode 2`

Bypass mode: Wake-up from low-power mode `Deep Sleep mode 2`

Test environment: `Idd_dcdc/Idd_IO_D`

Table 27. Test environment

DC-to-DC mode	Buck	Bypass
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s	
Payload	Tx:31 bytes; Rx:0 Bytes	
Connectable	Yes	
Flash	Doze	
MCU	Deep Sleep Mode 2 (DSM2)	
Setting	Advertise from low power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

Buck mode:

DC-to-DC output supply the LDO core and the radio blocks.

`Idd_DCDC=Idd_LDO_Core+Idd_RF`

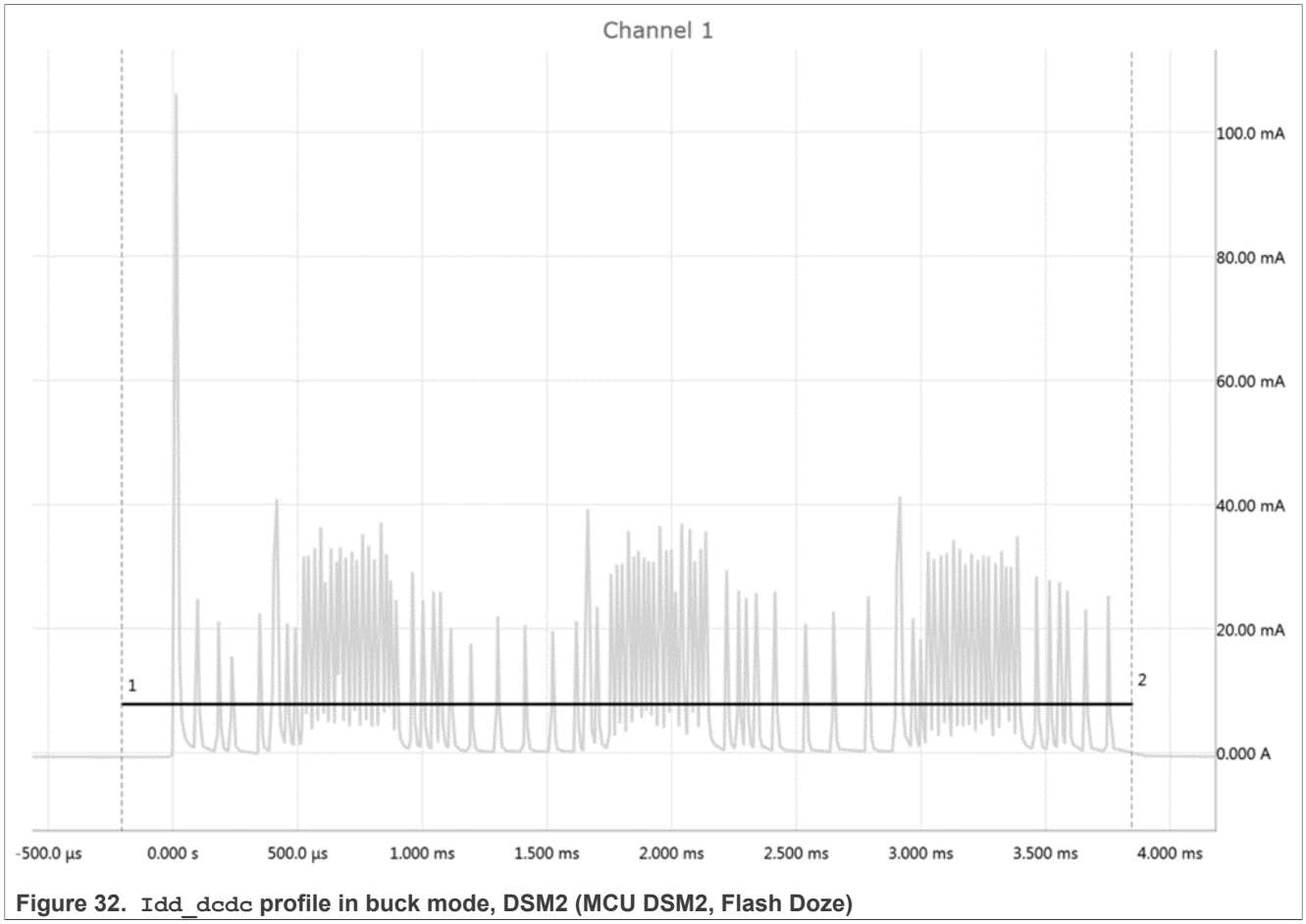

Figure 32. `Idd_dcdc` profile in buck mode, DSM2 (MCU DSM2, Flash Doze)

Table 28. `Idd_DCDC` current consumption in buck mode, `DSM2` (MCU `DSM2`, flash doze)

Idd_DCDC			
State	**Time (ms)**	**Current (mA)**	**mA x mS**
Pre-Processing	1.500 ms	1.282 mA	1.923 mA-ms
TX1 Rise	0.084 ms	3.540 mA	0.296 mA-ms
TX1 Level	0.216 ms	6.880 mA	1.487 mA-ms
TX1 Fall	0.020 ms	2.330 mA	0.047 mA-ms
TX1 to RX1 Transition	0.150 ms	2.945 mA	0.442 mA-ms
RX1 Rise	0.080 ms	1.552 mA	0.124 mA-ms
RX1 Level	0.080 ms	8.545 mA	0.684 mA-ms
RX1 Fall	0.022 ms	1.552 mA	0.034 mA-ms
MCU Stop	0.604 ms	2.243 mA	1.355 mA-ms
TX2 Rise	0.080 ms	3.420 mA	0.272 mA-ms
TX2 Level	0.216 ms	6.910 mA	1.495 mA-ms
TX1 Fall	0.021 ms	2.382 mA	0.050 mA-ms
TX1 to RX1 Transition	0.150 ms	2.853 mA	0.428 mA-ms

Table 28. `Idd_DCDC` current consumption in buck mode, `DSM2` (MCU `DSM2`, flash doze) *...continued*

Idd_DCDC			
State	**Time (ms)**	**Current (mA)**	**mA x mS**
RX1 Rise	0.079 ms	1.839 mA	0.145 mA-ms
RX2 Level	0.080 ms	8.530 mA	0.682 mA-ms
RX2 Fall	0.019 ms	1.840 mA	0.036 mA-ms
MCU Stop	0.604 ms	2.240 mA	1.353 mA-ms
TX3 Rise	0.072 ms	3.350 mA	0.241 mA-ms
TX3 Level	0.216 ms	6.640 mA	1.437 mA-ms
TX1 Fall	0.019 ms	2.360 mA	0.045 mA-ms
TX1 to RX1 Transition	0.150 ms	2.360 mA	0.354 mA-ms
RX1 Rise	0.081 ms	2.360 mA	0.191 mA-ms
RX3 Level	0.080 ms	8.490 mA	0.679 mA-ms
RX3 Fall	0.020 ms	1.580 mA	0.032 mA-ms
Post-Processing	0.980 ms	1.897 mA	1.859 mA-ms
Active Consumption	5.624 ms	2.112 mA	11.869 mA-ms
Charge Integral: 3.297 nAh			

Bypass mode: (DC-to-DC off), `Idd_dcdc=100nA`

Summary:

Table 29. Idd_DCDC current consumption event

Event	V_main=3 V	DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
Idd_DCDC	buck	5.62	2.112	3.297
	bypass	5.62	0.000100	0.000156

Test environment: `Idd_LDO_Core`

Bypass mode:

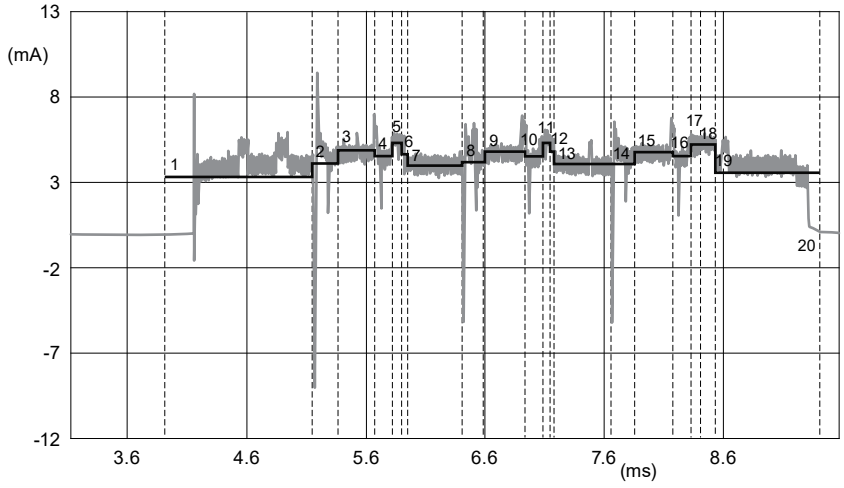

Figure 33. LDO_Core profile in bypass mode, DSM2 (MCU DSM2, Flash Doze)

Table 30. LDO_Core current consumption in bypass mode, DSM2 (MCU DSM2, flash doze)

Idd_LDO_CORE			
State	**Time (ms)**	**Current (mA)**	**mA x mS**
Pre-Processing	1.500 ms	2.628 mA	3.942 mA-ms
TX1 Rise	0.084 ms	2.022 mA	0.160 mA-ms
TX1 Level	0.216 ms	2.718 mA	0.586 mA-ms
TX1 Fall	0.020 ms	2.022 mA	0.040 mA-ms
TX1 to RX1 Transition	0.150 ms	2.038 mA	0.306 mA-ms
RX1 Rise	0.080 ms	2.058 mA	0.163 mA-ms
RX1 Level	0.080 ms	3.165 mA	0.253 mA-ms
RX1 Fall	0.022 ms	2.035 mA	0.037 mA-ms
MCU Stop	0.604 ms	1.797 mA	1.085 mA-ms
TX2 Rise	0.080 ms	2.022 mA	0.161 mA-ms
TX2 Level	0.216 ms	2.720 mA	0.587 mA-ms
TX1 Fall	0.021 ms	2.042 mA	0.043 mA-ms
TX1 to RX1 Transition	0.150 ms	2.042 mA	0.306 mA-ms
RX1 Rise	0.079 ms	2.059 mA	0.167 mA-ms
RX2 Level	0.080 ms	3.165 mA	0.253 mA-ms
RX2 Fall	0.019 ms	2.035 mA	0.040 mA-ms
MCU Stop	0.604 ms	1.900 mA	1.147 mA-ms
TX3 Rise	0.072 ms	2.023 mA	0.160 mA-ms
TX3 Level	0.216 ms	2.714 mA	0.574 mA-ms
TX1 Fall	0.019 ms	2.042 mA	0.043 mA-ms
TX1 to RX1 Transition	0.150 ms	2.061 mA	0.309 mA-ms
RX1 Rise	0.081 ms	2.066 mA	0.169 mA-ms
RX3 Level	0.080 ms	3.299 mA	0.264 mA-ms
RX3 Fall	0.020 ms	2.161 mA	0.042 mA-ms
Post-Processing	0.980 ms	1.879 mA	1.842 mA-ms
Active Consumption	5.624 ms	2.050 mA	11.521 mA-ms
Charge Integral: 3.2 nAh			

Summary:

Table 31. LDO_Core current consumption event

Event	V_main=3 V	DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
LDO_Core	bypass	5.62	2.050	3.2

5.2.2.6 `Vdd_RF` consumption

`Vdd_RF` consumption measurement is performed by placing the current probe on jumper `JP12`. The power supply is always applied via the USB connected to a PC.

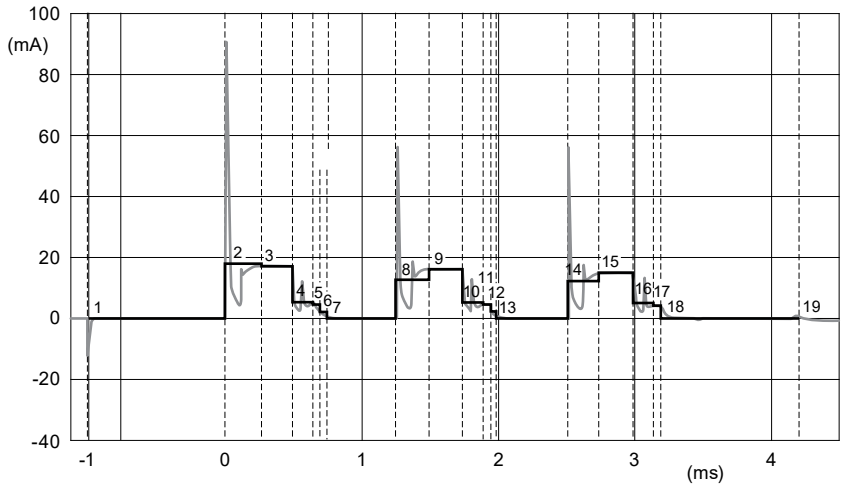

Figure 34. `Vdd_RF` current consumption

Table 32. Event

No.	Adv event timing
1	Pre-processing
2	TX warm-up
3	Active TX
4	TX to RX transition
5	Active RX
6	RX warm-down
7	MCU stop
8	TX warm-up
9	Active TX
10	TX to RX transition
11	Active RX
12	RX warm-down
13	MCU stop
14	TX warm-up
15	Active TX
16	TX to RX transition
17	Active RX
18	RX warm-down
19	Post-processing

Figure 34 and Table 32 shows the `Vdd_RF` current consumption during the advertising event.

The binary file settings used are:

- 48 MHz clock
- Advertising with X bytes TX payload, Y bytes RX payload and connectable
- RF output +10 dBm

Buck mode: Wake-up from low-power mode `Deep Sleep mode 2`

Bypass mode: Wake-up from low-power mode `Deep Sleep mode 2`

Test environment: `Vdd_RF`

Table 33. Test environment

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core = 1.25 V	Vdd_RF = 3 V, Vdd_LDO_Core = 3 V
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s	
Payload	Tx:31 bytes; Rx:0 Bytes	
Connectable	Yes	
Flash	Doze	
MCU	Deep Sleep Mode 2 (DSM2)	
Setting	Advertise from low power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

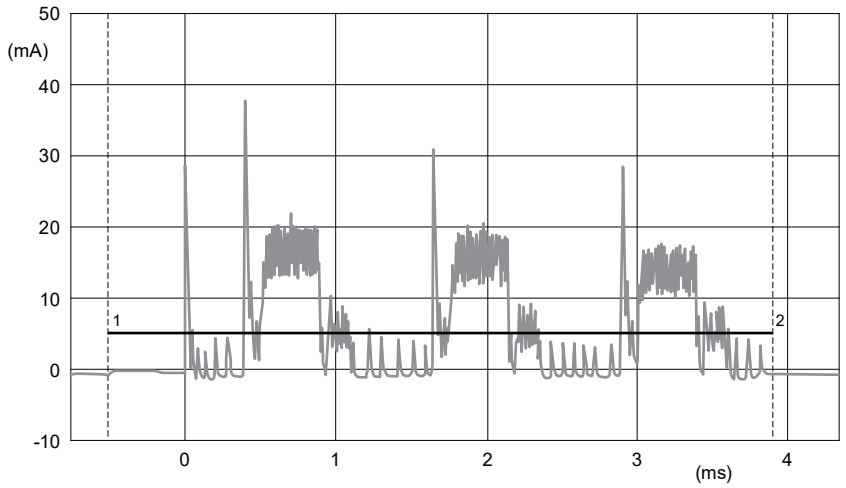

Figure 35. `Vdd_RF` profile in Buck mode, `DSM2` (MCU `DSM2`, flash doze)

Table 34. `Vdd_RF` current consumption in buck mode, `DSM2` (MCU `DSM2`, flash doze)

State	Time (ms)	Current (mA)	mA x mS
Pre-Processing	1.500 ms	0.380 mA	0.570 mA-ms
TX1 Rise	0.084 ms	1.709 mA	0.143 mA-ms
TX1 Level	0.216 ms	2.441 mA	0.527 mA-ms
TX1 Fall	0.020 ms	1.709 mA	0.034 mA-ms
TX1 to RX1 Transition	0.150 ms	2.224 mA	0.334 mA-ms
RX1 Rise	0.080 ms	2.984 mA	0.239 mA-ms
RX1 Level	0.080 ms	4.641 mA	0.371 mA-ms

Table 34. `Vdd_RF` current consumption in buck mode, `DSM2` (MCU `DSM2`, flash doze)*...continued*

State	Time (ms)	Current (mA)	mA x mS
RX1 Fall	0.022 ms	2.099 mA	0.046 mA-ms
MCU Stop	0.604 ms	0.306 mA	0.185 mA-ms
TX2 Rise	0.080 ms	1.733 mA	0.138 mA-ms
TX2 Level	0.216 ms	2.445 mA	0.529 mA-ms
TX1 Fall	0.021 ms	2.006 mA	0.042 mA-ms
TX1 to RX1 Transition	0.150 ms	2.006 mA	0.301 mA-ms
RX1 Rise	0.079 ms	3.059 mA	0.242 mA-ms
RX2 Level	0.080 ms	4.641 mA	0.371 mA-ms
RX2 Fall	0.019 ms	2.137 mA	0.041 mA-ms
MCU Stop	0.604 ms	0.307 mA	0.186 mA-ms
TX3 Rise	0.072 ms	1.731 mA	0.125 mA-ms
TX3 Level	0.216 ms	2.444 mA	0.529 mA-ms
TX1 Fall	0.019 ms	2.027 mA	0.039 mA-ms
TX1 to RX1 Transition	0.150 ms	2.444 mA	0.367 mA-ms
RX1 Rise	0.081 ms	3.031 mA	0.246 mA-ms
RX3 Level	0.080 ms	4.662 mA	0.373 mA-ms
RX3 Fall	0.020 ms	2.162 mA	0.044 mA-ms
Post-Processing	0.980 ms	0.295 mA	0.289 mA-ms
Active Consumption	5.624 ms	1.122 mA	6.309 mA-ms
Charge Integral: 1.75 nAh			

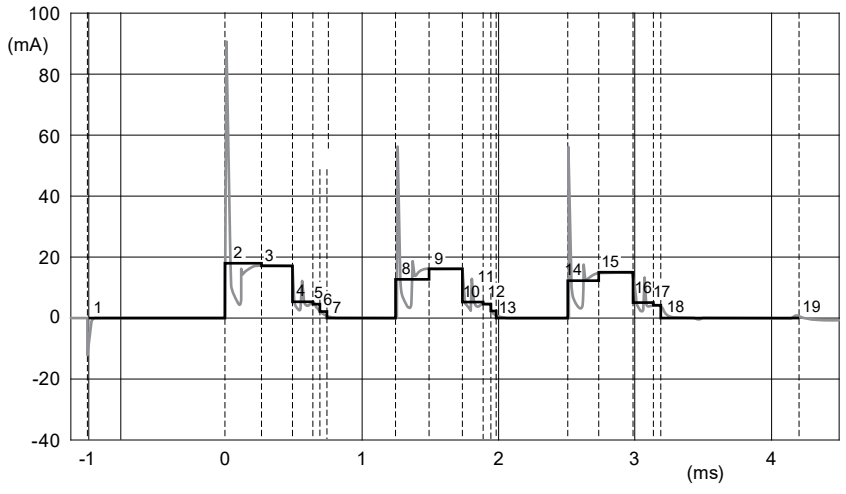

Figure 36. `Vdd_RF` profile in bypass mode, `DSM2` (MCU `DSM2`, flash doze)

Table 35. `Vdd_RF` current consumption in bypass mode, `DSM2` (MCU `DSM2`, flash doze)

State	Time (ms)	Current (mA)	mA x mS
Pre-Processing	1.500 ms	0.160 mA	0.240 mA-ms
TX1 Rise	0.079 ms	2.284 mA	0.181 mA-ms
TX1 Level	0.216 ms	7.188 mA	1.551 mA-ms

Table 35. Vdd_RF current consumption in bypass mode, DSM2 (MCU DSM2, flash doze)*...continued*

State	Time (ms)	Current (mA)	mA x mS
TX1 Fall	0.020 ms	2.284 mA	0.046 mA-ms
TX1 to RX1 Transition	0.150 ms	2.073 mA	0.311 mA-ms
RX1 Rise	0.079 ms	2.049 mA	0.162 mA-ms
RX1 Level	0.080 ms	5.051 mA	0.404 mA-ms
RX1 Fall	0.018 ms	2.019 mA	0.037 mA-ms
MCU Stop	0.604 ms	0.225 mA	0.136 mA-ms
TX2 Rise	0.080 ms	2.561 mA	0.204 mA-ms
TX2 Level	0.216 ms	7.154 mA	1.545 mA-ms
TX1 Fall	0.021 ms	1.868 mA	0.039 mA-ms
TX1 to RX1 Transition	0.150 ms	1.868 mA	0.280 mA-ms
RX1 Rise	0.081 ms	1.871 mA	0.152 mA-ms
RX2 Level	0.080 ms	5.097 mA	0.408 mA-ms
RX2 Fall	0.020 ms	2.036 mA	0.040 mA-ms
MCU Stop	0.604 ms	0.207 mA	0.125 mA-ms
TX3 Rise	0.079 ms	2.582 mA	0.204 mA-ms
TX3 Level	0.212 ms	7.038 mA	1.489 mA-ms
TX1 Fall	0.021 ms	1.828 mA	0.038 mA-ms
TX1 to RX1 Transition	0.150 ms	2.282 mA	0.342 mA-ms
RX1 Rise	0.082 ms	2.017 mA	0.165 mA-ms
RX3 Level	0.080 ms	5.059 mA	0.405 mA-ms
RX3 Fall	0.019 ms	2.019 mA	0.039 mA-ms
Post-Processing	0.980 ms	0.206 mA	0.202 mA-ms
Active Consumption	5.621 ms	1.340 mA	7.531 mA-ms
Charge Integral: 2.092 nAh			

Summary:

Table 36. Vdd_RF current consumption event

Event	V_main=3 V	DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
Vdd_RF	buck	5.62	1.122	1.75
	bypass	5.62	1.340	2.092

Test environment: Vdd_PA_2p4GHz

Table 37. Test environment

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core= 1.25 V	Vdd_RF = 3 V, Vdd_LDO_Core=3 V
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s	

Table 37. Test environment*...continued*

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core= 1.25 V	Vdd_RF = 3 V, Vdd_LDO_Core=3 V
Payload	Tx:31 bytes; Rx:0 Bytes	
Connectable	Yes	
Flash	Doze	
MCU	Deep Sleep Mode 2 (DSM2)	
Setting	Advertise from low power DSM2 Slave to Master	
Software	Low-power (2.12.5 MR2 release)	

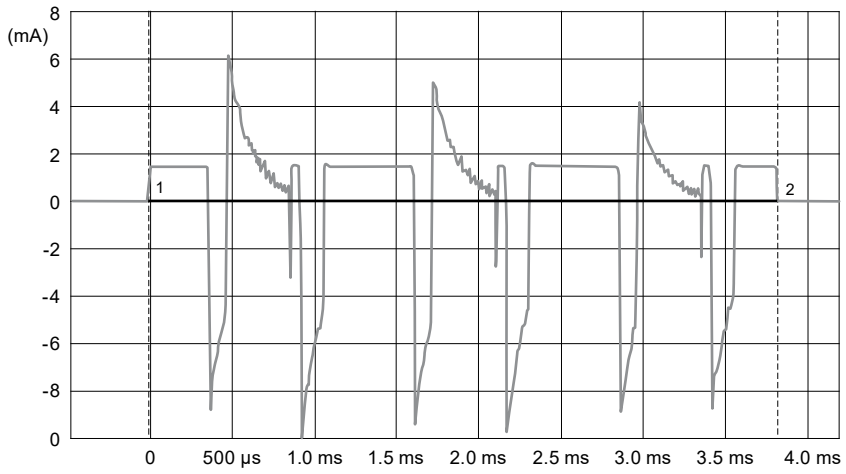

Figure 37. `Vdd_PA_2p4GHz` profile in buck mode, `DSM2` (MCU `DSM2`, flash doze)

Table 38. `Vdd_PA_2p4GHz` current consumption in buck mode, `DSM2` (MCU `DSM2`, flash doze)

`Idd_PA_2p4GHz`			
State	**Time (ms)**	**Current (mA)**	**mA x mS**
Pre-Processing	1.500 ms	0.929 mA	1.394 mA-ms
TX1 Rise	0.084 ms	0.012 mA	0.001 mA-ms
TX1 Level	0.216 ms	14.180 mA	3.064 mA-ms
TX1 Fall	0.020 ms	0.846 mA	0.017 mA-ms
TX1 to RX1 Transition	0.150 ms	0.846 mA	0.127 mA-ms
RX1 Rise	0.080 ms	0.846 mA	0.068 mA-ms
RX1 Level	0.080 ms	0.037 mA	0.003 mA-ms
RX1 Fall	0.022 ms	0.110 mA	0.002 mA-ms
MCU Stop	0.604 ms	0.576 mA	0.348 mA-ms
TX2 Rise	0.080 ms	10.650 mA	0.848 mA-ms
TX2 Level	0.216 ms	14.050 mA	3.040 mA-ms
TX1 Fall	0.021 ms	3.450 mA	0.072 mA-ms
TX1 to RX1 Transition	0.150 ms	3.450 mA	0.518 mA-ms

Table 38. `Vdd_PA_2p4GHz` current consumption in buck mode, `DSM2` (MCU `DSM2`, flash doze)*...continued*

`Idd_PA_2p4GHz`			
State	**Time (ms)**	**Current (mA)**	**mA x mS**
RX1 Rise	0.079 ms	3.450 mA	0.273 mA-ms
RX2 Level	0.080 ms	0.046 mA	0.004 mA-ms
RX2 Fall	0.019 ms	0.200 mA	0.004 mA-ms
MCU Stop	0.604 ms	0.571 mA	0.345 mA-ms
TX3 Rise	0.072 ms	11.190 mA	0.806 mA-ms
TX3 Level	0.216 ms	12.700 mA	2.748 mA-ms
TX1 Fall	0.019 ms	2.596 mA	0.049 mA-ms
TX1 to RX1 Transition	0.150 ms	2.596 mA	0.389 mA-ms
RX1 Rise	0.081 ms	2.596 mA	0.210 mA-ms
RX3 Level	0.080 ms	0.044 mA	0.004 mA-ms
RX3 Fall	0.020 ms	0.350 mA	0.007 mA-ms
Post-Processing	0.980 ms	0.667 mA	0.654 mA-ms
Active Consumption	5.624 ms	2.666 mA	14.994 mA-ms
Charge Integral: 4.165 nAh			

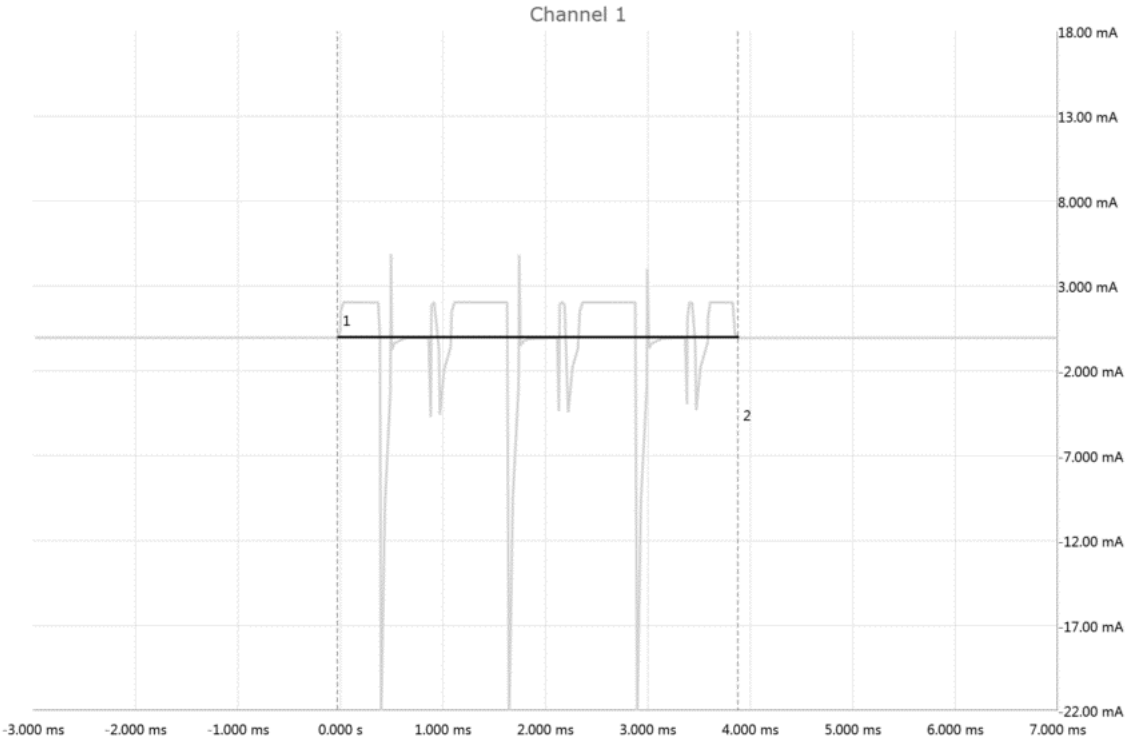

Figure 38. `Vdd_PA_2p4GHz` profile in bypass mode, `DSM2` (MCU `DSM2`, flash doze)

Table 39. `Vdd_PA_2p4GHz` current consumption in bypass mode, `DSM2` (MCU `DSM2`, flash doze)

State	Time (ms)	Current (mA)	mA x mS
Pre-Processing	1.500 ms	0.273 mA	0.410 mA-ms
TX1 Rise	0.079 ms	1.660 mA	0.132 mA-ms

Table 39. `Vdd_PA_2p4GHz` current consumption in bypass mode, `DSM2` (MCU `DSM2`, flash doze) *...continued*

State	Time (ms)	Current (mA)	mA x mS
TX1 Level	0.216 ms	15.500 mA	3.344 mA-ms
TX1 Fall	0.020 ms	2.266 mA	0.045 mA-ms
TX1 to RX1 Transition	0.150 ms	2.254 mA	0.338 mA-ms
RX1 Rise	0.079 ms	2.254 mA	0.178 mA-ms
RX1 Level	0.080 ms	6.092 mA	0.487 mA-ms
RX1 Fall	0.018 ms	1.359 mA	0.025 mA-ms
MCU Stop	0.604 ms	2.091 mA	1.263 mA-ms
TX2 Rise	0.080 ms	1.914 mA	0.152 mA-ms
TX2 Level	0.216 ms	15.380 mA	3.321 mA-ms
TX1 Fall	0.021 ms	2.273 mA	0.048 mA-ms
TX1 to RX1 Transition	0.150 ms	2.273 mA	0.341 mA-ms
RX1 Rise	0.081 ms	2.273 mA	0.184 mA-ms
RX2 Level	0.080 ms	6.092 mA	0.487 mA-ms
RX2 Fall	0.020 ms	1.960 mA	0.039 mA-ms
MCU Stop	0.604 ms	2.103 mA	1.270 mA-ms
TX3 Rise	0.079 ms	2.150 mA	0.170 mA-ms
TX3 Level	0.212 ms	14.730 mA	3.116 mA-ms
TX1 Fall	0.021 ms	2.019 mA	0.042 mA-ms
TX1 to RX1 Transition	0.150 ms	2.273 mA	0.341 mA-ms
RX1 Rise	0.082 ms	2.019 mA	0.166 mA-ms
RX3 Level	0.080 ms	6.095 mA	0.488 mA-ms
RX3 Fall	0.019 ms	1.067 mA	0.021 mA-ms
Post-Processing	0.980 ms	1.109 mA	1.087 mA-ms
Active Consumption	5.621 ms	3.112 mA	17.494 mA-ms
Charge Integral: 4.859 nAh			

Summary:

Table 40. Vdd_PA_2p4GHz current consumption event

-	V_main = 3 V	DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
Vdd_PA_2p4GHz	buck	5.62	2.666	4.165
	bypass	5.62	3.112	4.859

Table 41. Global summary current consumption event

Pin names	V_main=3 V	DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
LDO_Core	buck	5.62	1.140	1.780 nAh
	bypass	5.62	2.050	3.200 nAh
RF	buck	5.62	1.122	1.752 nAh
	bypass	5.62	1.340	2.092 nAh
Ana	buck	5.62	0.064	0.100 nAh
	bypass	5.62	0.064	0.100 nAh
DCDC/IO_D	buck	5.62	2.112	3.297 nAh

Table 41. Global summary current consumption event*...continued*

Pin names	V_main=3 V	DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
	bypass	5.62	0.0001	0.000156 nAh
IO_ABC	buck	5.62	0.451	0.704 nAh
	bypass	5.62	0.897	1.400 nAh
Switch	buck	5.62	0.064	0.100 nAh
	bypass	5.62	0.064	0.100 nAh
PA_2p4GHz	buck	5.62	2.666	4.162 nAh
	bypass	5.62	3.112	4.858 nAh
Total	buck	5.62	2.697	4.201 nAh
	bypass	5.62	4.414	6.892 nAh

Global summary:

In Buck mode: `Idd_reg= Idd_dcdc (power consumption of Idd_LDO_Core and Idd_RF) +Idd_PA+Idd_Ana+Idd_IO_ABC+Idd_switch`

In Bypass mode: `Idd_reg= Idd_LDO_Core + Idd_RF + Idd_dcdc/Idd_IO_D + Idd_PA + Idd_Ana + Idd_IO_ABC + Idd_switch`

Table 42. Global summary current consumption event versus main voltage

Advertising	1.71 V	1.8 V	2.1 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V	Unit
Buck mode	4.10	4.24	4.53	4.82	4.60	4.21	3.91	3.56	nAh
Bypass mode	5.92	6.01	6.37	6.76	6.85	6.89	6.88	6.81	nAh

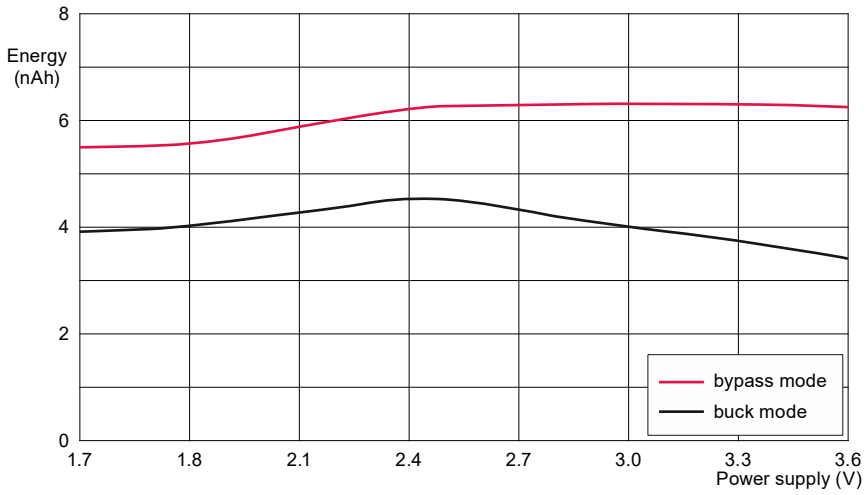

Figure 39. Global Advertising event power consumption profile in buck and bypass mode, DSM2 vs main power supply

Table 43. Buck mode, summary current consumption event versus main voltage and temperature

Advertising, buck	1.7 V	1.8 V	2.1 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	Unit
-40 °C	3.97	4.15	4.48	4.67	4.50	4.13	3.84	3.48	nAh
-20 °C	4.03	4.21	4.52	4.73	4.56	4.17	3.88	3.52	nAh
25 °C	4.10	4.24	4.53	4.82	4.60	4.21	3.91	3.56	nAh

Table 43. Buck mode, summary current consumption event versus main voltage and temperature...*continued*

Advertising, buck	1.7 V	1.8 V	2.1 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	Unit
65 °C	4.30	4.75	5.00	5.28	5.02	4.66	4.26	3.96	nAh
85 °C	4.94	5.40	5.62	6.04	5.60	5.16	4.74	4.16	nAh
105 °C	5.84	6.19	6.54	7.02	6.62	6.07	5.58	5.05	nAh
120 °C	6.25	6.76	7.46	7.99	7.65	6.98	6.42	5.94	nAh

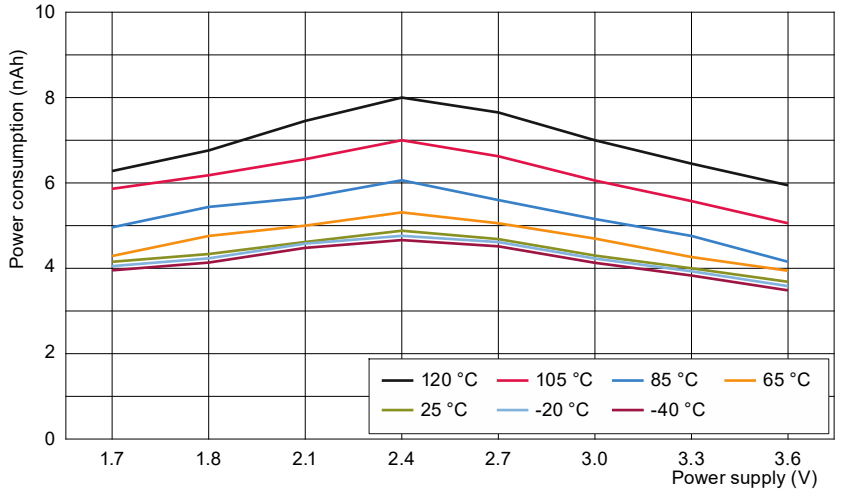

Figure 40. Global Advertising event power consumption profile in buck mode vs voltage and temperature, DSM2 vs main power supply

Table 44. Bypass mode, summary current consumption event versus main voltage and temperature

Advertising, bypass	1.71 V	1.8 V	2.1 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	-Unit
-40 °C	5.73	5.87	6.31	6.55	6.71	6.76	6.74	6.66	nAh
-20 °C	5.82	5.96	6.36	6.65	6.80	6.83	6.81	6.73	nAh
25 °C	5.92	6.01	6.37	6.76	6.85	6.89	6.88	6.81	nAh
65 °C	5.93	6.07	6.42	6.87	6.90	6.93	6.91	6.86	nAh
85 °C	6.02	6.15	6.49	6.95	6.98	7.00	6.98	6.88	nAh
105 °C	6.16	6.31	6.55	7.04	7.02	7.07	7.01	6.96	nAh
120 °C	6.47	6.50	6.60	7.13	7.08	7.14	7.05	7.00	nAh

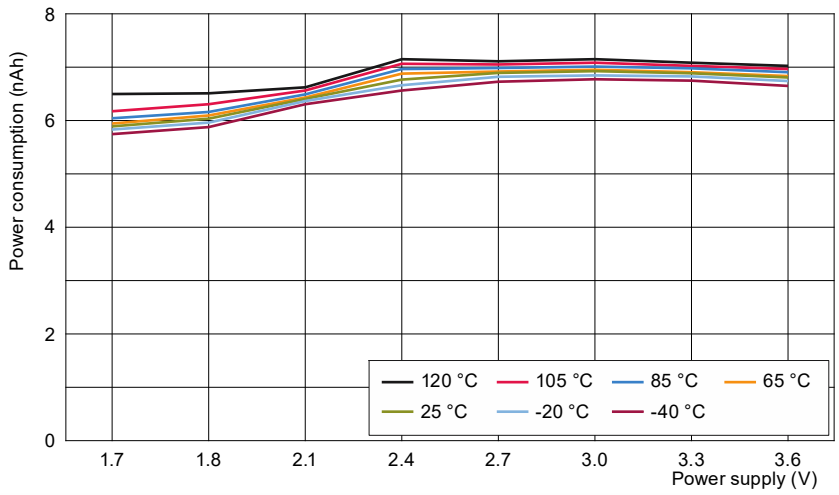

Figure 41. Global Advertising event power consumption profile in bypass mode vs voltage and temperature, DSM2 vs main power supply

5.2.2.7 Connection mode

NXP android app is used to perform connection, see Figure 42.

Figure 42. IoT Toolbox

On the central side (in this case, a smartphone or a tablet with Bluetooth LE 5.x available), the following application must be installed: IoT Toolbox, available on the Google play store and Apple iTunes (IoT toolbox version 5.0.9 minimum).

The Thermometer application must be used. For measuring advertising events, there is no need for a connecting device, but for measuring connection events, it is mandatory. To connect to the KW45-EVK board, the procedure is simple and straightforward:

- Open IoT Toolbox
- Power-up KW45-EVK board and press `SW1` to start advertising
- On Android application the `FSL_Thermo` must be reported at scan phase
- Connect to `FSL_Thermo` peripheral
- Wait for measurements

Templates:

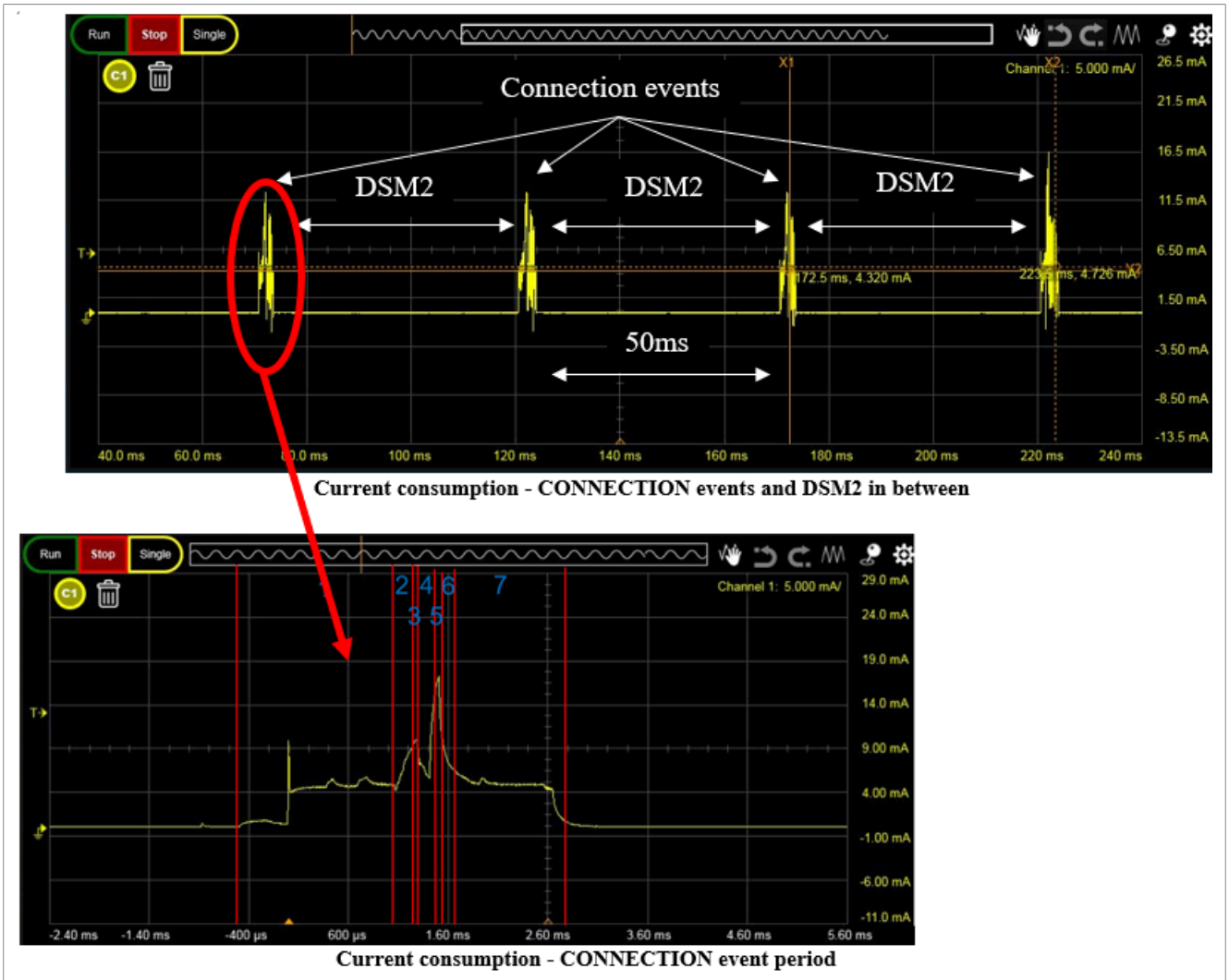

Figure 43. Current consumption during the connect event period

Table 45. Event

No.	Adv event timing
1	Pre-processing
2	TX warm-up
3	Active RX
4	RX to TX transition
5	Active TX
6	TX warm-down

Table 45. Event*...continued*

No.	Adv event timing
7	Post-processing

Note: *In the Figure 43, both use cases are used: Low power Deep Sleep mode 2 (DSM2) is activated between the Connection events.*

Figure 43 shows the current consumption during the connect event.

The binary file settings used (slave) are:

- 48 MHz clock
- Advertising with RX Y bytes payload, X TX payload and connectable
- RF output +0 dBm

Buck mode: Wake-up from low-power mode `Deep Sleep mode 2`

Bypass mode: Wake-up from low-power mode `Deep Sleep mode 2`

The smartphones are the master, which defines the data rate during the connection. Four data rates are considered:

- 1 Mbit/s
- 2 Mbit/s
- 500 kbit/s (LR S=2)
- 125 kbit/s (LR S=8)

In the `app_preinclude.h`, the `gAppExtAdvEnable` must be enabled to get the LR connection.

If enabled, the OPT Host lib is required (must set `lib_ble_5-2_OPT_host_cm33_iar.a` as lib in linker setting) `*/ #define gAppExtAdvEnable_d 1`

Test environment: Connect 1 Mbit/s

Table 46. Test environment

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	Vdd_RF = 3 V Vdd_LDO_Core=3 V
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s	
Payload	Tx:0 bytes; Rx:2 Bytes	
Connectable	Yes	
Flash	Doze	
MCU	Deep Sleep Mode 2 (DSM2)	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low-power (2.12.5 MR2 release)	

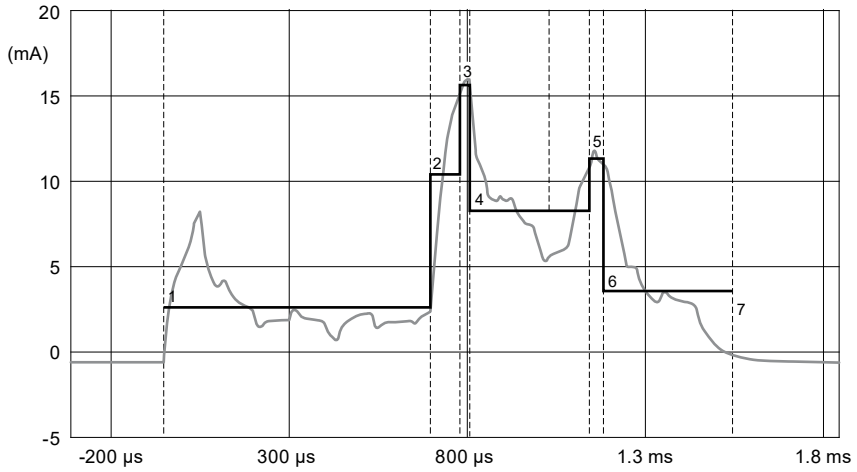

Figure 44. Connect profile in buck mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s

Table 47. Connect current consumption in buck mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s

CONNECTION (1 packet exchange)				
1 Msps	**Buck mode**	**Idd_REG (total consumption)**		
	State	**Time(ms)**	**Current(mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	2.717 mA	2.038 mA-ms
	RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	RX1 Level	0.080 ms	6.948 mA	0.556 mA-ms
	RX1 to TX1 Transition	0.150 ms	6.840 mA	1.026 mA-ms
	TX1 Level	0.096 ms	6.860 mA	0.659 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	Post-Processing	0.360 ms	4.825 mA	1.737 mA-ms
	Active Consumption	1.536 ms	4.361 mA	6.699 mA-ms
Charge Integral: 1.86 nAh				

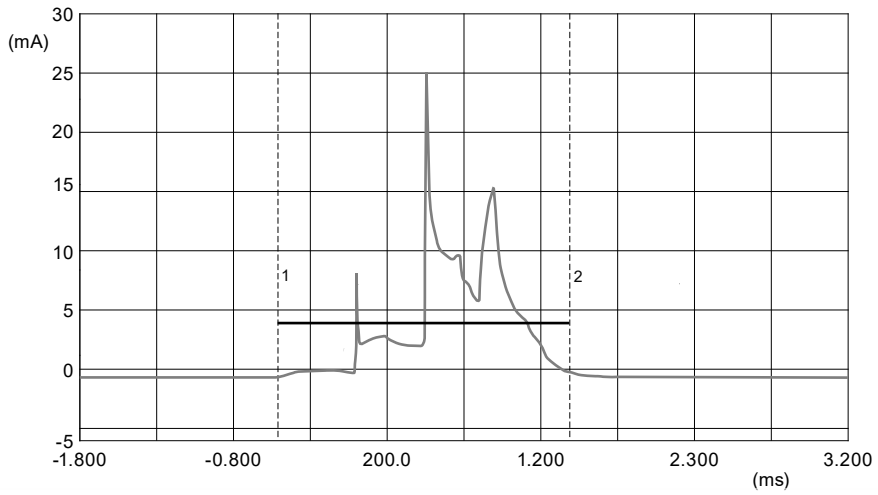

Figure 45. Connect profile in bypass mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s

Table 48. Connect current consumption in bypass mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s

	Bypass mode	Idd_REG (total consumption)		
	State	**Time(ms)**	**Current(mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	3.378 mA	2.534 mA-ms
	RX1 Rise	0.080 ms	3.950 mA	0.316 mA-ms
	RX1 Level	0.080 ms	14.612 mA	1.169 mA-ms
	RX1 to TX1 Transition	0.150 ms	3.950 mA	0.593 mA-ms
	TX1 Level	0.096 ms	14.401 mA	1.383 mA-ms
	TX1 Fall	0.020 ms	3.950 mA	0.079 mA-ms
	Post-Processing	0.360 ms	7.018 mA	2.526 mA-ms
	Active Consumption	1.536 ms	5.598 mA	8.599 mA-ms
	Charge Integral: 2.39 nAh			

Test environment: Connect 2 Mbit/s

Table 49. Test environment

DC-to-DC mode	**Buck**	**Bypass**
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	2 Mbit/s	
Payload	Tx:0 bytes; Rx:2 Bytes	
Connectable	Yes	
Flash	Doze	
MCU	Deep Sleep Mode 2 (DSM2)	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low-power (2.12.5 MR2 release)	

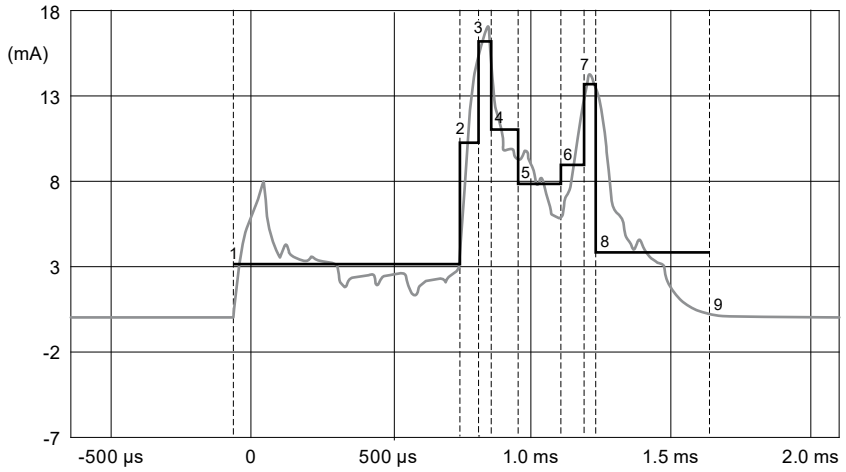

Figure 46. Connect profile in buck mode, DSM2 (MCU DSM2, flash doze), 2 Mbit/s

Table 50. Connect current consumption in buck mode, DSM2 (MCU DSM2, flash doze), 2 Mbit/s

CONNECTION (1 packet exchange)				
2 Msps	**Buck mode**	**Idd_REG (total consumption)**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	1.089 mA	0.816 mA-ms
	RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	RX1 Level	0.044 ms	6.948 mA	0.306 mA-ms
	RX1 to TX1 Transition	0.150 ms	6.840 mA	1.026 mA-ms
	TX1 Level	0.052 ms	6.860 mA	0.357 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	Post-Processing	0.360 ms	4.825 mA	1.737 mA-ms
	Active Consumption	1.456 ms	3.383 mA	4.926 mA-ms
	Charge Integral: 1.37 nAh			

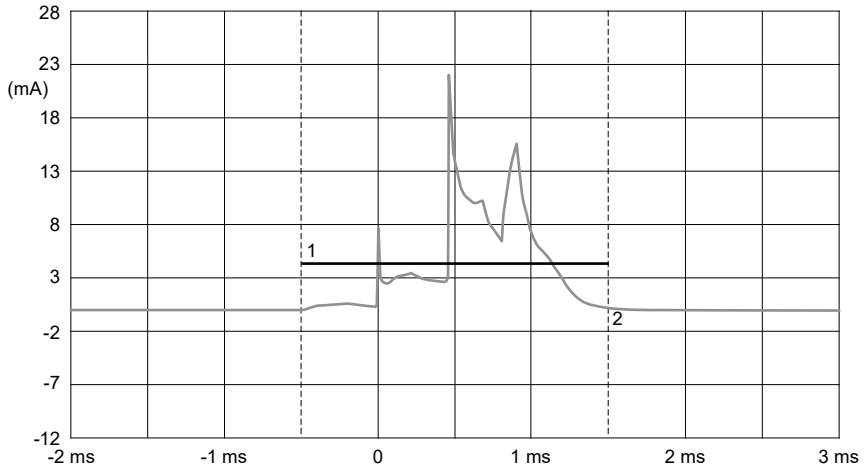

Figure 47. Connect profile in bypass mode, DSM2 (MCU DSM2, flash doze), 2 Mbit/s

Table 51. Connect current consumption in bypass mode, DSM2 (MCU DSM2, flash doze), 2 Mbit/s

CONNECTION (1 packet exchange)				
2 Msps	**Bypass mode**	**Idd_REG (total consumption)**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	1.362 mA	1.021 mA-ms
	RX1 Rise	0.080 ms	3.950 mA	0.316 mA-ms
	RX1 Level	0.044 ms	14.612 mA	0.643 mA-ms
	RX1 to TX1 Transition	0.150 ms	3.950 mA	0.593 mA-ms
	TX1 Level	0.052 ms	14.401 mA	0.749 mA-ms
	TX1 Fall	0.020 ms	3.950 mA	0.079 mA-ms
	Post-Processing	0.360 ms	7.018 mA	2.526 mA-ms
	Active Consumption	1.456 ms	4.071 mA	5.927 mA-ms
	Charge Integral: 1.65 nAh			

Test environment: Connect 500 kbit/s (coded LR S2)

Table 52. Test environment

DC-to-DC mode	**Buck**	**Bypass**
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	500 kbit/s	
Payload	Tx:0 bytes; Rx:2 Bytes	
Connectable	Yes	
Flash	Doze	
MCU	Deep Sleep Mode 2 (DSM2)	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low-power (2.12.5 MR2 release)	

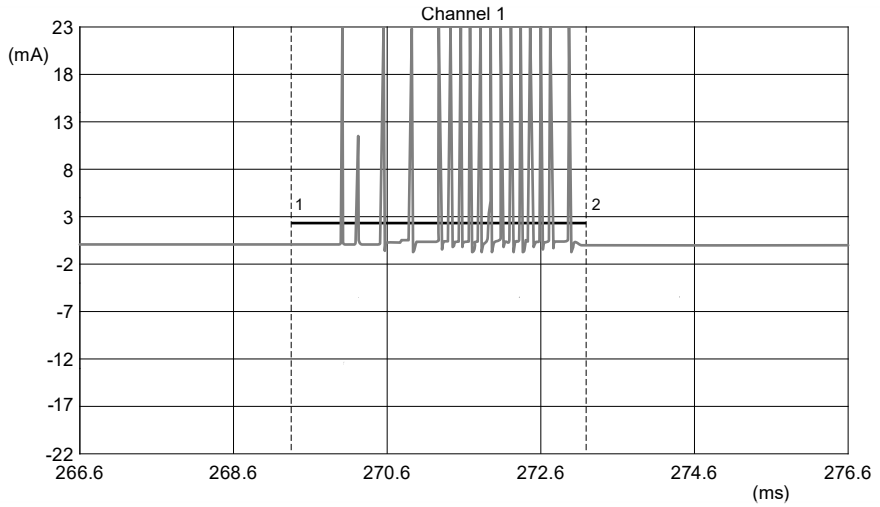

Figure 48. Connect profile in buck mode, DSM2 (MCU DSM2, flash doze), 500 kbit/s LR S2

Table 53. Connect current consumption in buck mode, DSM2 (MCU DSM2, flash doze), 500 kbit/s LR S2

CONNECTION (1 packet exchange)				
500 ksps	**Buck mode**	**Idd_REG (total consumption)**		
	State	**Time(ms)**	**Current(mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	2.726 mA	2.175 mA-ms
	RX1 Rise	0.080 ms	6.840 mA	0.313 mA-ms
	RX1 Level	0.160 ms	6.948 mA	0.960 mA-ms
	RX1 to TX1 Transition	0.150 ms	6.840 mA	0.629 mA-ms
	TX1 Level	0.192 ms	6.860 mA	0.816 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.095 mA-ms
	Post-Processing	0.360 ms	4.825 mA	0.641 mA-ms
	Active Consumption	1.712 ms	4.626 mA	7.920 mA-ms
	Charge Integral: 2.20 nAh			

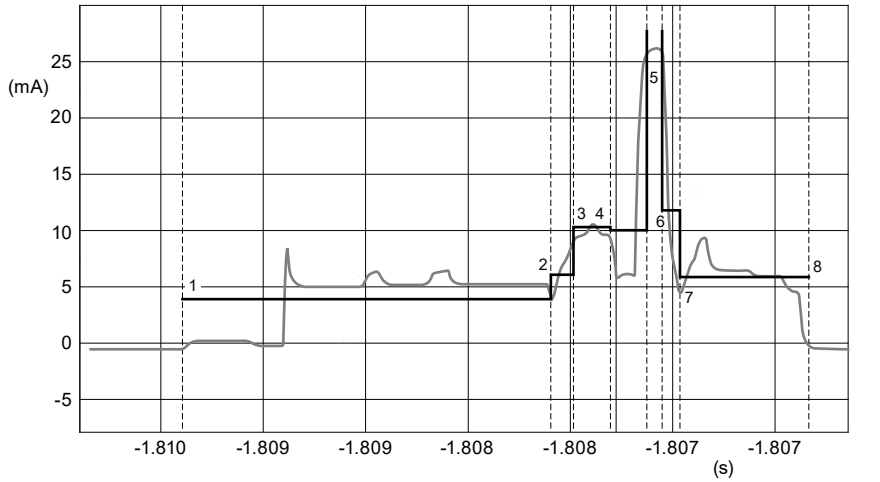

Figure 49. Connect profile in bypass mode, DSM2 (MCU DSM2, flash doze), 500 kbit/s LR S2

Table 54. Connect current consumption in bypass mode, DSM2 (MCU DSM2, flash doze), 500 kbit/s LR S2

CONNECTION (1 packet exchange)				
500 ksps	**Bypass mode**	**Idd_REG (total consumption)**		
LR S2	**State**	**Time (ms)**	**Current (mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	3.430 mA	2.573 mA-ms
	RX1 Rise	0.080 ms	3.950 mA	0.316 mA-ms
	RX1 Level	0.160 ms	14.612 mA	2.338 mA-ms
	RX1 to TX1 Transition	0.150 ms	3.950 mA	0.593 mA-ms
	TX1 Level	0.192 ms	14.401 mA	2.765 mA-ms
	TX1 Fall	0.020 ms	3.950 mA	0.079 mA-ms
	Post-Processing	0.360 ms	12.632 mA	4.547 mA-ms
	Active Consumption	1.712 ms	7.716 mA	13.211 mA-ms
	Charge Integral: 3.67 nAh			

Test environment: Connect 125 kbit/s (coded LR S8)

Table 55. Test environment

DC-to-DC mode	Buck	Bypass
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	125 kbit/s	
Payload	Tx:0 bytes; Rx:2 Bytes	
Connectable	Yes	
Flash	Doze	
MCU	Deep Sleep Mode 2 (DSM2)	
Setting:	Advertise from low-power DSM2 Slave to Master	
Software	Low-power (2.12.5 MR2 release)	

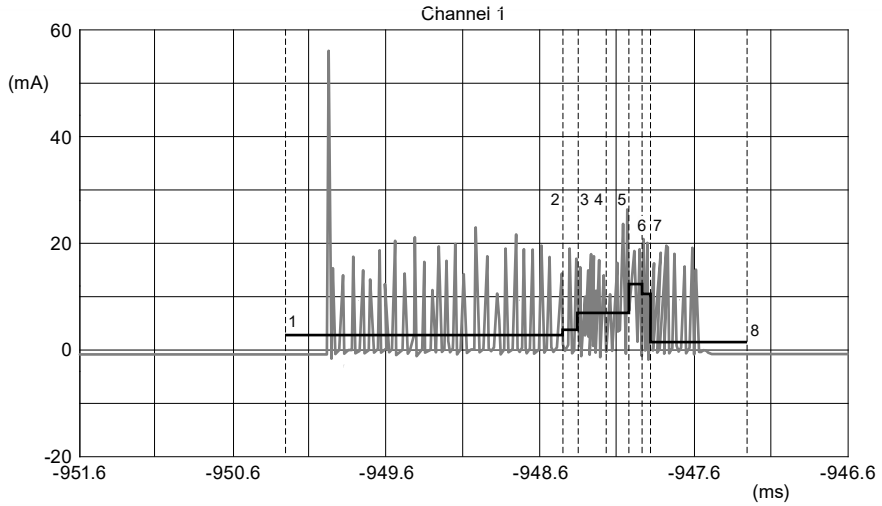

Figure 50. Connect profile in buck mode, DSM2 (MCU DSM2, flash doze), 125 kbit/s LR S8

Table 56. Connect current consumption in buck mode, DSM2 (MCU DSM2, flash doze), 125 kbit/s LR S8

CONNECTION (1 packet exchange)				
125 ksps	**Buck mode**	**Idd_REG (total consumption)**		
	State	**Time(ms)**	**Current (mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	2.731 mA	2.048 mA-ms
	RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	RX1 Level	0.640 ms	6.948 mA	4.447 mA-ms
	RX1 to TX1 Transition	0.150 ms	6.840 mA	1.026 mA-ms
	TX1 Level	0.768 ms	6.860 mA	5.268 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	Post-Processing	0.360 ms	4.825 mA	1.737 mA-ms
	Active Consumption	2.768 ms	5.495 mA	15.210 mA-ms
	Charge Integral: 4.23 nAh			

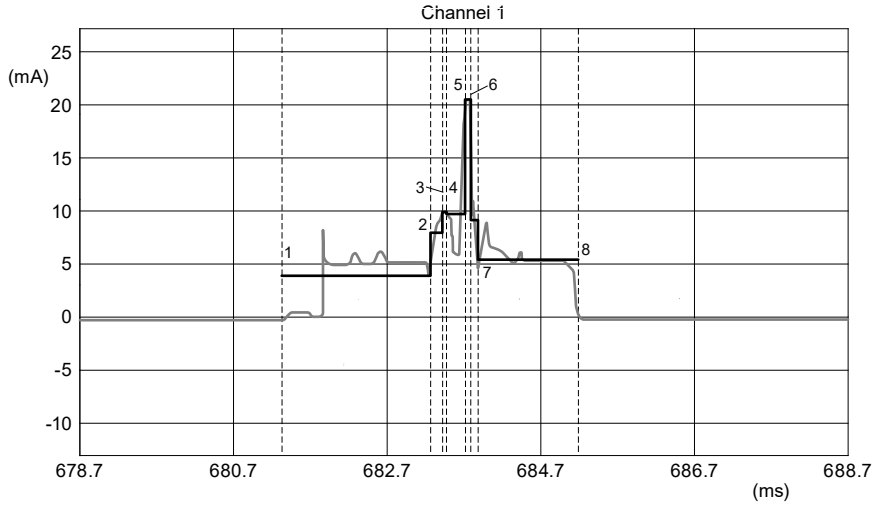

Figure 51. Connect profile in bypass mode, DSM2 (MCU DSM2, flash doze), 125 kbit/s LR S8

Table 57. Connect current consumption in bypass mode, DSM2 (MCU DSM2, flash doze), 125 kbit/s LR S8

CONNECTION (1 packet exchange)				
125 ksps	**Bypass mode**	**Idd_REG (total consumption)**		
LR S8	**State**	**Time(ms)**	**Current(mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	3.457 mA	2.593 mA-ms
	RX1 Rise	0.080 ms	3.950 mA	0.316 mA-ms
	RX1 Level	0.640 ms	14.612 mA	9.351 mA-ms
	RX1 to TX1 Transition	0.150 ms	3.950 mA	0.593 mA-ms
	TX1 Level	0.768 ms	14.401 mA	11.060 mA-ms
	TX1 Fall	0.020 ms	3.950 mA	0.079 mA-ms
	Post-Processing	0.360 ms	12.632 mA	4.547 mA-ms
	Active Consumption	2.768 ms	10.310 mA	28.539 mA-ms
	Charge Integral: 7.93 nAh			

Summary:

Table 58. Connect current consumption (MCU DSM2, flash doze)

48 MHz clock using 32KHx Crystal	Buck mode Consumption (3 V)	Bypass mode consumption (3 V)
	DSM2	DSM2
	T= 25 °C	
CONN pre-processing 1 Mbit/s	4.361 mA	5.598 mA
CONN pre-processing 2 Mbit/s	3.383 mA	4.071 mA
CONN pre-processing 500 kbit/s	4.626 mA	7.716 mA
CONN pre-processing 125 kbit/s	5.495 mA	10.310 mA

Table 59. Connect timing (MCU DSM2, flash doze)

Radio/Profile Timing Parameters (ms)	Buck mode Consumption (3 V)	Bypass mode consumption (3 V)
48 MHz clock using 32 kHz crystal	DSM2	DSM2
	T= 25 °C	
Conn Pre-processing Time – 1 Mbit/s	0.750 ms	0.750 ms
Conn Post-processing Time - 1 Mbit/s	0.360 ms	0.360 ms
Conn Pre-processing Time – 2 Mbit/s	0.750 ms	0.750 ms
Conn Post-processing Time - 2 Mbit/s	0.360 ms	0.360 ms
Conn Pre-processing Time – 500 kbit/s	0.750 ms	0.750 ms
Conn Post-processing Time - 500 kbit/s	0.360 ms	0.360 ms
Conn Pre-processing Time – 125 kbit/s	0.750 ms	0.750 ms
Conn Post-processing Time - 125 kbit/s	0.360 ms	0.360 ms

Table 60. Connect current consumption event

CONNECT	Vdcdc_in=3 V	DSM2		
1 Mbit/s	buck	1.536 ms	4.361 mA	1.861 nAh
	bypass	1.536 ms	5.598 mA	2.389 nAh

Table 60. Connect current consumption event*...continued*

CONNECT	Vdcdc_in=3 V	DSM2		
2 Mbit/s	buck	1.456 ms	3.383 mA	1.368 nAh
	bypass	1.456 ms	4.071 mA	1.646 nAh
LR S2, 500 kbit/s	buck	1.712 ms	4.626 mA	2.200 nAh
	bypass	1.712 ms	7.716 mA	3.670 nAh
LR S8, 125 kbit/s	buck	2.768 ms	5.495 mA	4.225 nAh
	bypass	2.768 ms	10.310 mA	7.928 nAh

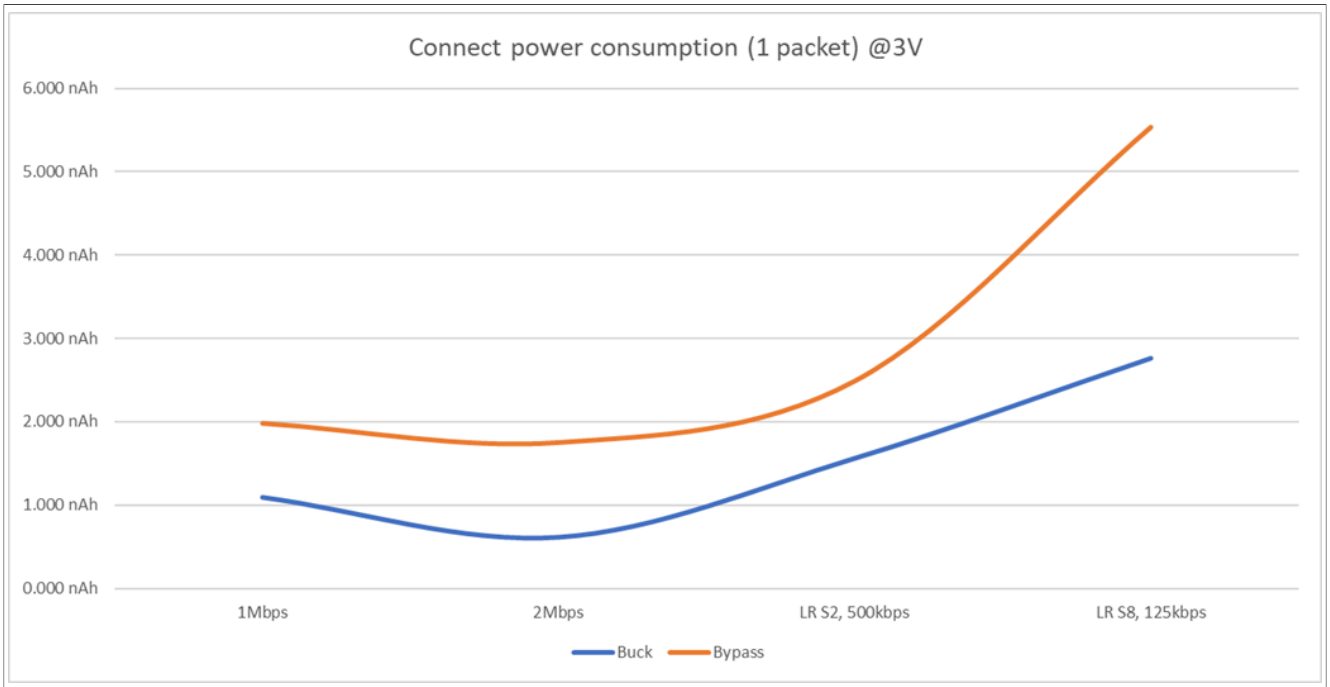

Figure 52. Connect profile vs data rate and DC-to-DC modes, DSM2 (MCU DSM2, Flash Doze)

5.2.2.8 Scan mode

Using the steps listed in Section 4.2, partial Bluetooth LE scenario (Temperature Collector Application) is shown in Figure 53. The main events and phases are listed in Table 61 including all the plots that follow depicts current.

Buck mode and Bypass DC-DC modes are used:

- DSM2 Mode is activated between the scan events.

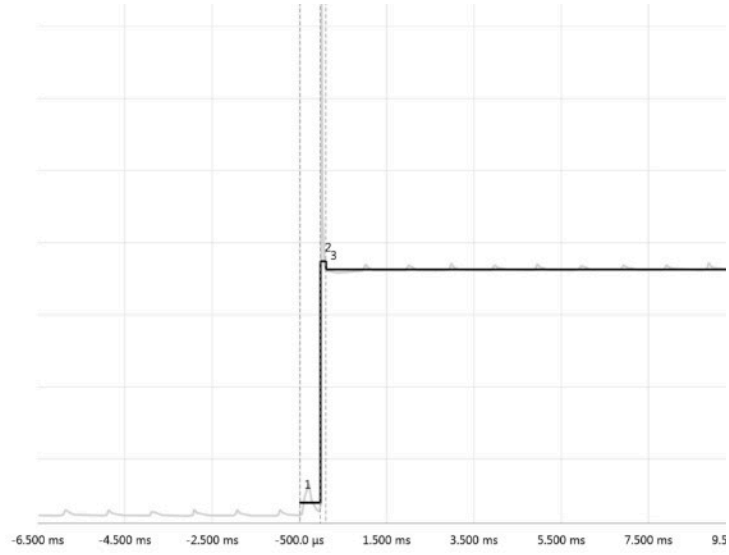

Figure 53. Current consumption - Scan event period

Table 61. Scan events

No.	Event
1	Pre-processing
2	RX warmup
3	Active RX
4	RX warm down
5	Post-processing

Figure 54 shows the current consumption during the scan event.

The binary file settings used are:

- 48 MHz clock
- Scanning

Buck mode: Wake-up from low-power mode `Deep Sleep mode 2`

Bypass mode: Wake-up from low-power mode `Deep Sleep mode 2`

Test environment: Scan mode

Table 62. Test environment

DC-to-DC mode	Buck	Bypass
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**	**Vdd_RF = 3 V** **Vdd_LDO_Core=3 V**
RF output power	na	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s	
Payload	na	
Connectable	Yes	

Table 62. Test environment*...continued*

DC-to-DC mode	Buck	Bypass
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**	**Vdd_RF = 3 V** **Vdd_LDO_Core=3 V**
Flash	Doze	
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

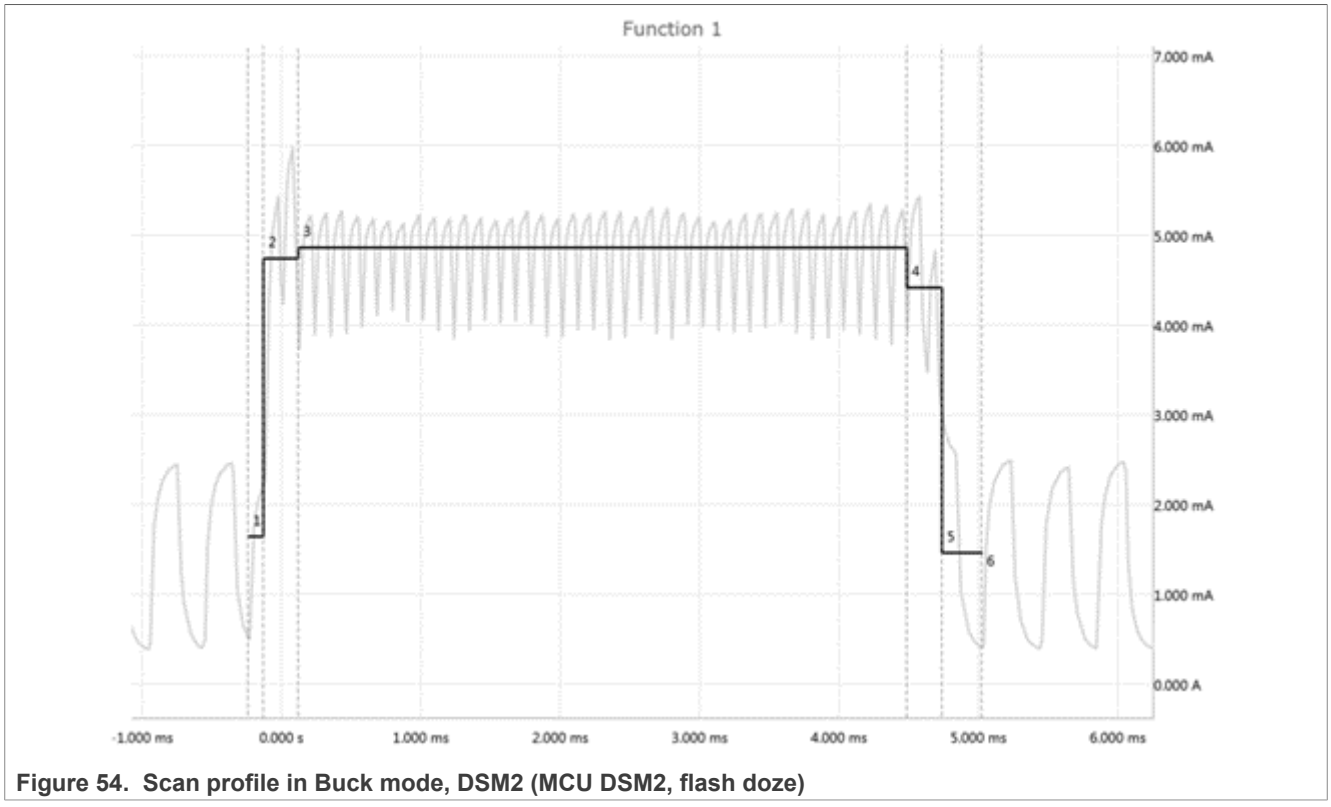

Figure 54. Scan profile in Buck mode, DSM2 (MCU DSM2, flash doze)

Table 63. Scan current consumption in Buck mode, DSM2 (MCU DSM2, flash doze)

Scanning				
Buck	**Scanning windows**	**4.0 ms**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Scan	Scan pre-processing	1.900 ms	2.668 mA	5.069 mA-ms
	RX warm-up	0.080 ms	6.840 mA	0.547 mA-ms
	RX Scan	4.000 ms	7.463 mA	29.851 mA-ms
	RX warm-down	0.020 ms	6.840 mA	0.137 mA-ms
	Scan Post-process	0.150 ms	4.550 mA	0.683 mA-ms
	Active Consumption	6.150 ms	Avg= 5.672 mA	36.287 mA-ms
	Charge Integral: 10.08 nAh			

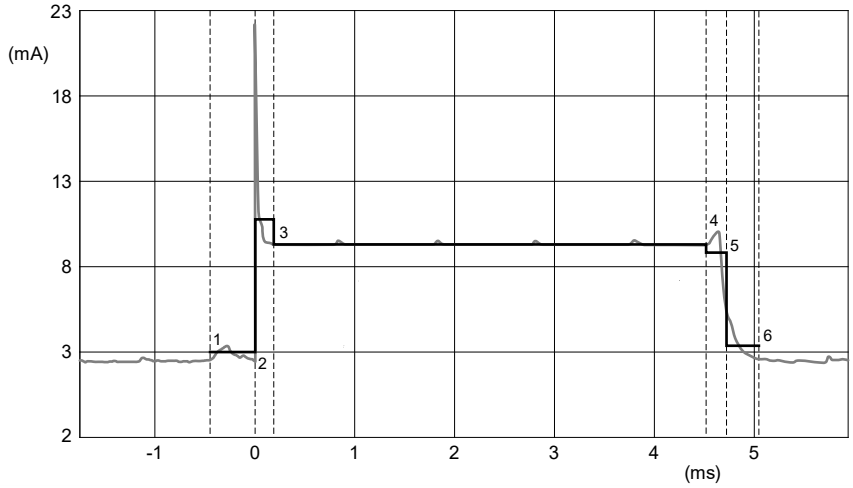

Figure 55. Scan profile in bypass mode, DSM2 (MCU DSM2, flash doze)

Table 64. Scan current consumption in bypass mode, DSM2 (MCU DSM2, flash doze)

Scanning				
Bypass	**Scanning windows**	**4 ms**		
	State	**Time(ms)**	**Current(mA)**	**mA x mS**
Scan	Scan pre-processing	1.900 ms	5.760 mA	10.944 mA-ms
	RX warm-up	0.080 ms	39.900 mA	3.192 mA-ms
	RX Scan	4.000 ms	15.783 mA	63.131 mA-ms
	RX warm-down	0.020 ms	39.900 mA	0.798 mA-ms
	Scan Post-process	0.150 ms	7.800 mA	1.170 mA-ms
	Active Consumption	6.150 ms	Avg= 21.829 mA	**79.235 mA-ms**
Charge Integral: 22.01 nAh				

Summary:

Table 65. Scan current timing (MCU DSM2, Flash Doze)

Radio/Profile Timing Parameters (ms)	**Buck mode Consumption (3.6 V)**	**Bypass mode consumption (3.6 V)**
	DSM2	
48 MHz FEE Mode using 32 kHz crystal	**T= 25 °C**	
Scan Preprocessing Time	1.900 ms	1.900 ms
Scan Postprocessing Time	0.150 ms	0.150 ms

Table 66. Scan current consumption event

	Vdcdc_in=3.6 V	**DSM2 (ms)**	**DSM2 (mA)**	**DSM2 (nAh)**
Scan	buck	6.150 ms	5.672 mA	10.08 nAh
	bypass	6.150 ms	21.829 mA	22.01 nAh

5.3 Advertising extension

Bluetooth 5.x allows advert packets to be transmitted in the data channels (although the specification prefers to label them as secondary advert channels):

- Increases advertising data length
- Allows advertising on data channels
- Enables long-range connection establishment
- Enables chaining and periodic advertising

In this case, the new primary advert points to an auxiliary packet that specifies a “connectionless” train of packets that hop at a known Cadence.

That auxiliary packet provides the Cadence information and the access address code.

Table 67 and Figure 56 shows the current consumption during the advertising event at 1 Mbit/s, 2 Mbit/s, and coded and advertising extension event using data rate at 1 Mbit/s, 2 Mbit/s, and coded. For More details, see Figure 57 and Figure 64.

The binary file settings used:

- 48 MHz clock
- Advertising Extension with PDU 8 bytes for channels 37, 38, 39 and PDU Y bytes (X bytes payload) and connectable
- RF output +0 dBm

Buck mode: Wake-up from low-power mode `Deep Sleep mode 2`

Bypass mode: Wake-up from low-power mode `Deep Sleep mode 2`

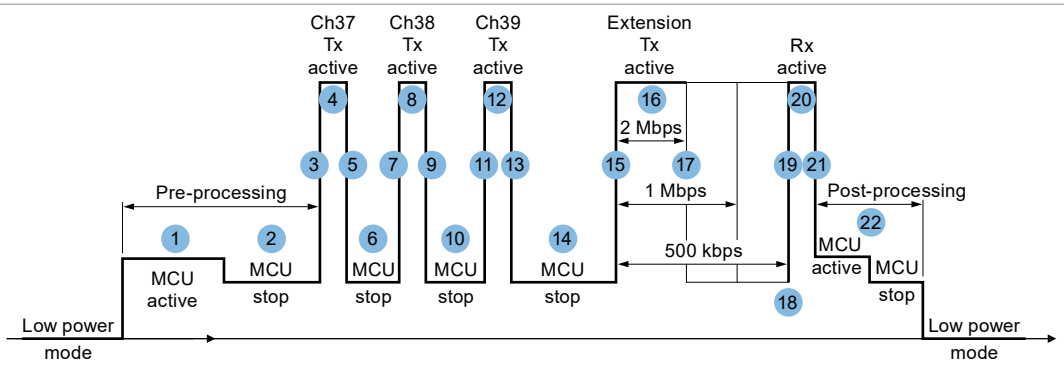

Figure 56. Current consumption - advertising event period

Table 67. Advertising extension event

No.	ADV event timing
1	Pre-processing / MCU active
2	Post-processing / MCUstop
3	TX warm-down
4	TX active
5	TX warm-down
6	MCU stop
7	TX warm-up
8	TX active

Table 67. Advertising extension event*...continued*

No.	ADV event timing
9	TX warm-down
10	MCU stop
11	TX warm-up
12	TX active
13	TX warm-down
14	MCU stop
15	TX warm-up
16	TX active
17	TX warm-down
18	TX to RX
19	RX warm-up
20	RX active
21	RX warm-down
22	Post-processing

Test environment: Advertising extension 1 Mbit/s 1 Mbit/s

Table 68. Test environment

DC-to-DC mode	Buck	Bypass
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s 1 Mbit/s	
Payload	For CH37.38 and39 : PDU size 2 bytes (2 bytes payload), For Secondary CH: PDU size 2, payload size Tx 31bytes, Rx 0bytes	
Connectable	Yes	
Flash	Doze	
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

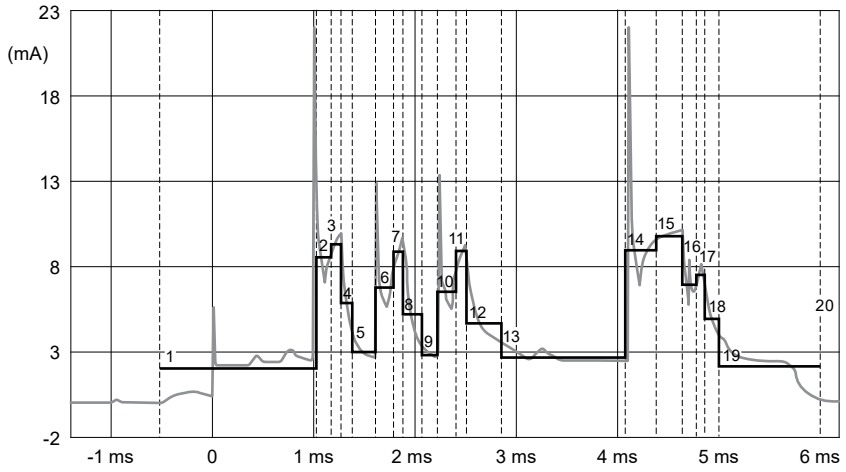

Figure 57. Advertising extension current profile event after DSM2 mode, Bypass mode, 1 Mbit/s 1 Mbit/s

Table 69. Advertising extension current consumption in Bypass mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s 1 Mbit/s

	Bypass mode	Idd_REG (total consumption)		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADVERTISING	Pre-Processing	0.900 ms	2.400 mA	2.160 mA-ms
	TX1 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX1 Level	0.096 ms	14.401 mA	1.383 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.117 ms	2.900 mA	0.338 mA-ms
	TX2 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX2 Level	0.096 ms	14.401 mA	1.383 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.429 ms	2.900 mA	1.244 mA-ms
	TX3 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX3 Level	0.096 ms	14.401 mA	1.383 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.117 ms	2.900 mA	0.338 mA-ms
	TX Aux Channel Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX Aux Channel Level	0.328 ms	14.401 mA	4.724 mA-ms
	TX to RX1 Transition	0.050 ms	13.400 mA	0.670 mA-ms
	RX Aux Channel Level	0.080 ms	14.612 mA	1.169 mA-ms
	RX Aux Channel Fall	0.020 ms	13.400 mA	0.268 mA-ms
	Post-Processing	0.560 ms	4.000 mA	2.240 mA-ms
	Active Consumption	3.268 ms	10.943 mA	22.390 mA-ms
	Charge Integral: 6.22 nAh			

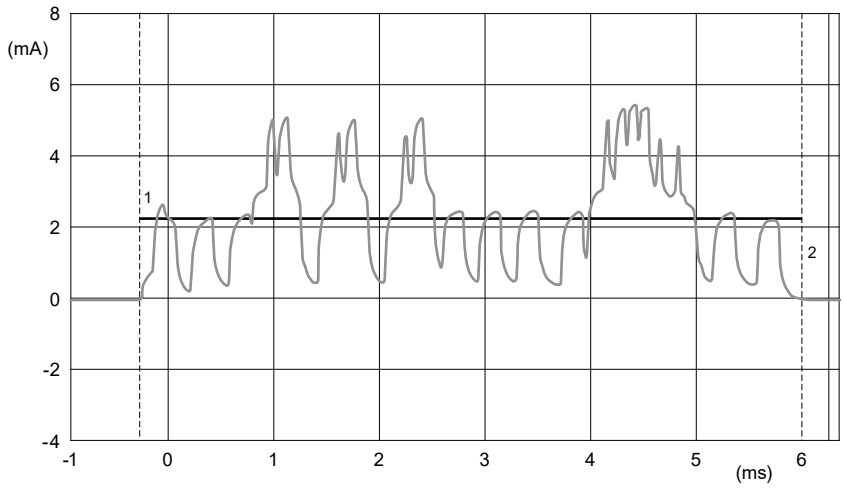

Figure 58. Advertising extension current profile event after DSM2 mode, Buck mode, 1 Mbit/s 1 Mbit/s

Table 70. Advertising extension current consumption in Buck mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s 1 Mbit/s

	Buck mode	Idd_REG (total consumption)		
	State	Time (ms)	Current (mA)	mA x mS
ADV	Active Consumption	2.421 ms	4.598 mA	11.132 mA-ms
Charge Integral: 3.09 nAh				

Test environment: Advertising extension 1 Mbit/s 2 Mbit/s

Table 71. Test environment

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	Vdd_RF = 3 V Vdd_LDO_Core=3 V
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s 2 Mbit/s	
Payload	For CH37.38 and39 : PDU size 2 bytes (2 bytes payload), For Secondary CH: PDU size 2, payload size Tx 31bytes, Rx 0 bytes.	
Connectable	Yes	
Flash	Doze	
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

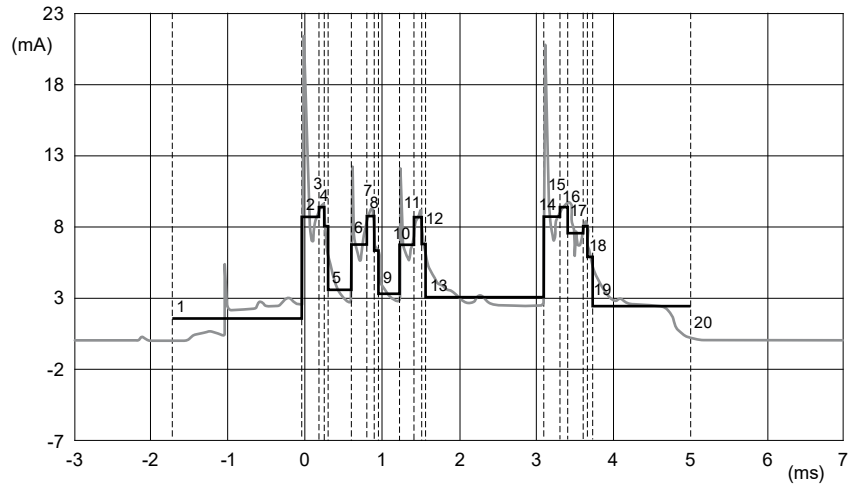

Figure 59. Advertising extension current profile event after DSM2 mode, Bypass mode, 1 Mbit/s 2 Mbit/s

Table 72. Advertising extension current consumption in Bypass mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s 2 Mbit/s

	Bypass mode	**Idd_REG (total consumption)**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADVERTISING	Pre-Processing	0.900 ms	2.400 mA	2.160 mA-ms
	TX1 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX1 Level	0.052 ms	14.401 mA	0.749 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.161 ms	2.900 mA	0.465 mA-ms
	TX2 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX2 Level	0.052 ms	14.401 mA	0.749 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.161 ms	2.900 mA	0.465 mA-ms
	TX3 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX3 Level	0.052 ms	14.401 mA	0.749 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.161 ms	2.900 mA	0.465 mA-ms
	TX Aux Channel Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX Aux Channel Level	0.168 ms	14.401 mA	2.419 mA-ms
	TX to RX1 Transition	0.050 ms	13.400 mA	0.670 mA-ms
	RX Aux Channel Level	0.044 ms	14.612 mA	0.643 mA-ms
	RX Aux Channel Fall	0.020 ms	13.400 mA	0.268 mA-ms
	Post-Processing	0.560 ms	4.000 mA	2.240 mA-ms
	Active Consumption	2.760 ms	6.210 mA	17.135 mA-ms
	Charge Integral; 4.76 nAh			

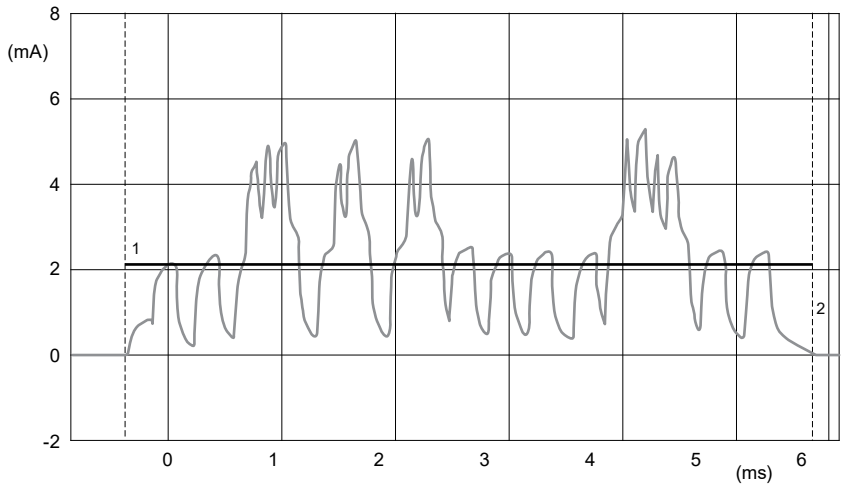

Figure 60. Advertising extension current profile event after DSM2 mode, Buck mode, 1 Mbit/s 2 Mbit/s

Table 73. Advertising extension current consumption in Buck mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s 2 Mbit/s

	Buck mode	Idd_REG (total consumption)		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADV	Active Consumption	2.225 ms	4.097 mA	**9.116 mA-ms**
-	**Charge Integral:** 2.53 nAh			

Test environment: Advertising extension, 1 Mbit/s coded

Table 74. Test environment

DC-to-DC mode	BUCK	BYPASS
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128 k	
Data rate	1 Mbit/s coded	
Payload	For CH37.38 and39: PDU size 2 bytes (2 payload), For secondary CH: PDU size 2 bytes, payload size 31 bytes.	
Connectable	Yes	
Flash	Doze	
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

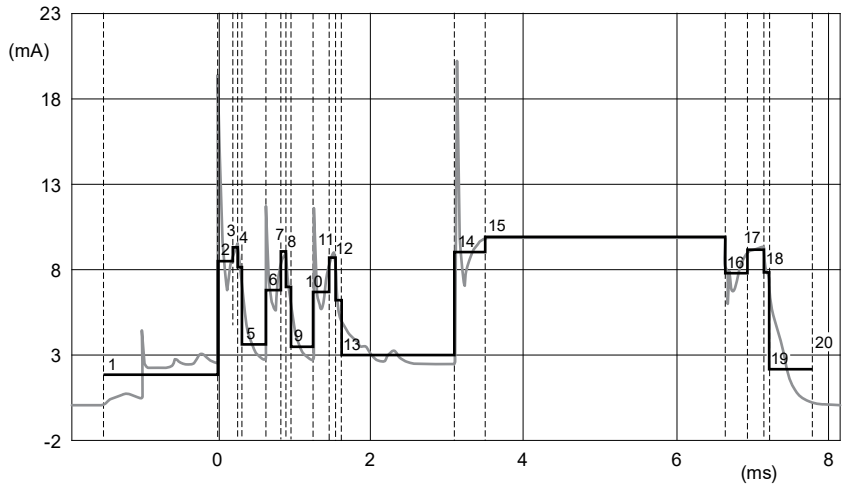

Figure 61. Advertising extension current profile event after DSM2 mode, Bypass mode, 1 Mbps coded

Table 75. Advertising Extension current consumption in DSM2 mode, Bypass mode, 1 Mbps coded

	Bypass mode	**Idd_REG (total consumption)**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADVERTISING	Pre-Processing	0.900 ms	2.400 mA	2.160 mA-ms
	TX1 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX1 Level	0.192 ms	14.401 mA	2.765 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.021 ms	2.900 mA	0.059 mA-ms
	TX2 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX2 Level	0.192 ms	14.401 mA	2.765 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.021 ms	2.900 mA	0.059 mA-ms
	TX3 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX3 Level	0.192 ms	14.401 mA	2.765 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.021 ms	2.900 mA	0.059 mA-ms
	TX Aux Channel Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX Aux Channel Level	0.656 ms	14.401 mA	9.447 mA-ms
	TX to RX1 Transition	0.050 ms	13.400 mA	0.670 mA-ms
	RX Aux Channel Level	0.160 ms	14.612 mA	2.338 mA-ms
	RX Aux Channel Fall	0.020 ms	13.400 mA	0.268 mA-ms
	Post-Processing	0.560 ms	4.000 mA	2.240 mA-ms
	Active Consumption	3.364 ms	9.124 mA	30.688 mA-ms
	Charge Integral: 8.52 nAh			

Table 76. Advertising Extension current consumption in Buck mode, DSM2 (MCU DSM2, flash doze), 1 Mbps coded

	Buck mode	Idd_REG (total consumption)		
	State	Time (ms)	Current (mA)	mA x mS
ADV	Active Consumption	2.829 ms	5.442 mA	15.395 mA-ms
Charge Integral: 4.28 nAh				

Test environment: Advertising extension coded 1 Msps

Table 77. Test environment

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	Vdd_RF = 3 V Vdd_LDO_Core=3 V
RF output power	+0 dBm	
MCU clock mode	48 MHz	
RAM size	128 k	
Data rate	Coded 1 Msps	
Payload	For CH37.38 and39 : PDU size 2 bytes (payload 31 bytes), For Secondary CH: PDU size 2 bytes, payload size 2 bytes	
Connectable	Yes	
Flash	Doze	
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

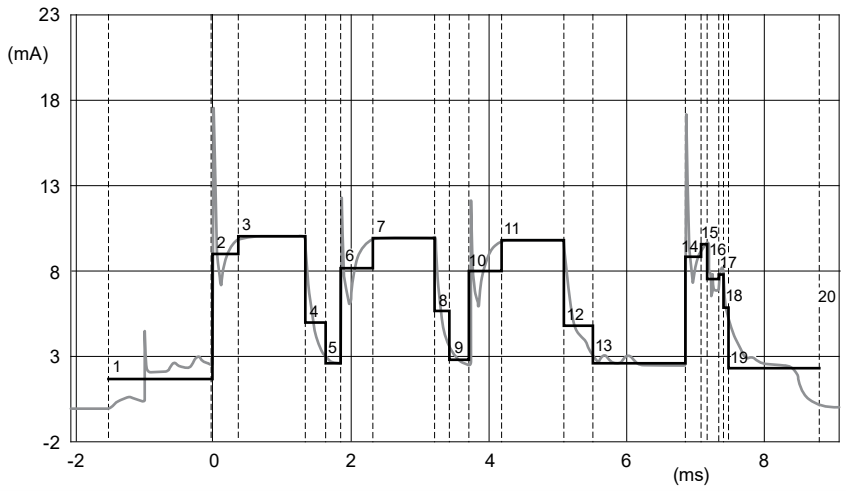

Figure 62. Advertising extension current profile event after DSM2 mode, bypass mode, coded 1 Mbit/s

Table 78. Advertising extension current consumption in Bypass mode, DSM2 mode, coded 1 Mbit/s

	Bypass mode	Idd_REG (total consumption)		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADVERTISING	Pre-Processing	1.500 ms	2.400 mA	3.600 mA-ms
	TX1 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX1 Level	0.328 ms	14.401 mA	4.724 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.197 ms	2.900 mA	0.571 mA-ms
	TX2 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX2 Level	0.328 ms	14.401 mA	4.724 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.197 ms	2.900 mA	0.571 mA-ms
	TX3 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX3 Level	0.328 ms	14.401 mA	4.724 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.197 ms	2.900 mA	0.571 mA-ms
	TX Aux Channel Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX Aux Channel Level	0.096 ms	14.401 mA	1.382 mA-ms
	TX to RX1 Transition	0.050 ms	13.400 mA	0.670 mA-ms
	RX Aux Channel Level	0.080 ms	14.612 mA	1.169 mA-ms
	RX Aux Channel Fall	0.020 ms	13.400 mA	0.268 mA-ms
	Post-Processing	1.330 ms	4.000 mA	5.320 mA-ms
	Active Consumption	5.031 ms	6.636 mA	33.386 mA-ms
	Charge Integral: 9.27 nAh			

Table 79. Advertising extension current consumption in Bypass mode, DSM2 (MCU DSM2, flash doze), coded 1 Mbit/s

	Buck mode	Idd_REG (total consumption)		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADV	Active Consumption	5.031 ms	3.998 mA	20.114 mA-ms
Charge Integral: 5.59 nAh				

Test environment: Advertising extension coded 2 Mbit/s

Table 80. Test environment

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	Vdd_RF = 3 V Vdd_LDO_Core=3 V
RF output power	+0 dBm	
MCU clock mode	48 MHz	

Table 80. Test environment*...continued*

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	Vdd_RF = 3 V Vdd_LDO_Core=3 V
RAM size	128k	
Data rate	Coded 2 Mbit/s	
Payload	For CH37.38 and39 : PDU size 2 bytes (payload 31 bytes), For Secondary CH: PDU size 2 bytes, payload size 2 bytes	
Connectable	Yes	
Flash	Doze	
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

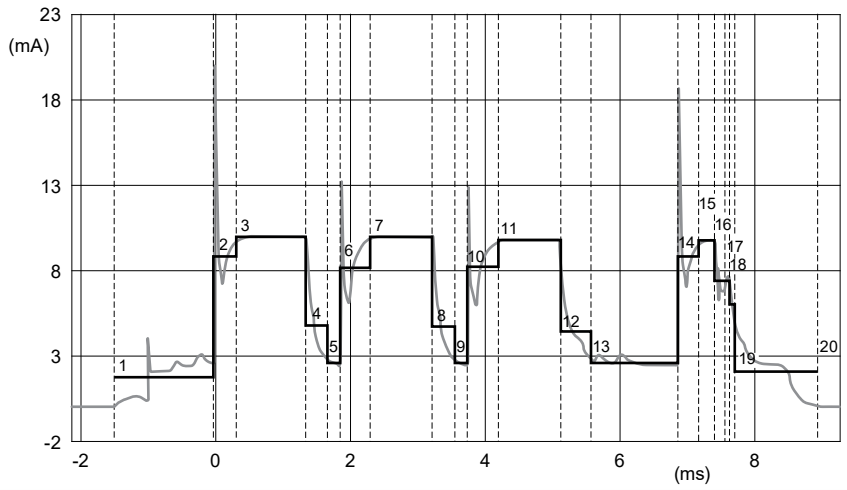

Figure 63. Advertising Extension current profile event after DSM2 mode, Bypass mode, coded 2 Mbit/s

Table 81. Advertising extension current consumption in Bypass mode, DSM2 mode, coded 2 Mbit/s

	Bypass mode	Idd_REG (total consumption)		
	State	Time(ms)	Current(mA)	mA x mS
Advertising	Pre-Processing	1.500 ms	3.621 mA	5.432 mA-ms
	TX1 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX1 Level	0.168 ms	14.401 mA	2.419 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.045 ms	2.900 mA	0.129 mA-ms
	TX2 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX2 Level	0.168 ms	14.401 mA	2.419 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.045 ms	2.900 mA	0.129 mA-ms
	TX3 Rise	0.080 ms	13.400 mA	1.072 mA-ms

Table 81. Advertising extension current consumption in Bypass mode, DSM2 mode, coded 2 Mbit/s*...continued*

	Bypass mode	Idd_REG (total consumption)		
	State	**Time(ms)**	**Current(mA)**	**mA x mS**
	TX3 Level	0.168 ms	14.401 mA	2.419 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.045 ms	2.900 mA	0.129 mA-ms
	TX Aux Channel Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX Aux Channel Level	0.052 ms	14.401 mA	0.749 mA-ms
	TX to RX1 Transition	0.050 ms	13.400 mA	0.670 mA-ms
	RX Aux Channel Level	0.044 ms	14.612 mA	0.643 mA-ms
	RX Aux Channel Fall	0.020 ms	13.400 mA	0.268 mA-ms
	Post-Processing	1.330 ms	4.000 mA	5.320 mA-ms
	Active Consumption	4.014 ms	6.433 mA	25.819 mA-ms
	Charge Integral: 7.17 nAh			

Table 82. Advertising extension current consumption in Bypass mode, DSM2 (MCU DSM2, flash doze), coded 2 Mbit/s

	Buck mode	Idd_REG (total consumption)		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADV	Active Consumption	4.014 ms	3.851 mA	15.458 mA-ms
Charge Integral: 4.29 nAh				

Test environment: Advertising extension coded coded

Table 83. Test environment: Advertising extension Coded Coded

DC-to-DC mode	Buck	Bypass
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	+10 dBm	
MCU clock mode	48 MHz	
RAM size	128 k	
Data rate	Coded Coded	
Payload	For CH37.38 and39 : PDU size 6 bytes (payload 31 bytes), For Secondary CH: PDU size 2 bytes, payload size Tx:31 bytes; Rx:2 bytes	
Connectable	Yes	
Flash	Doze	
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

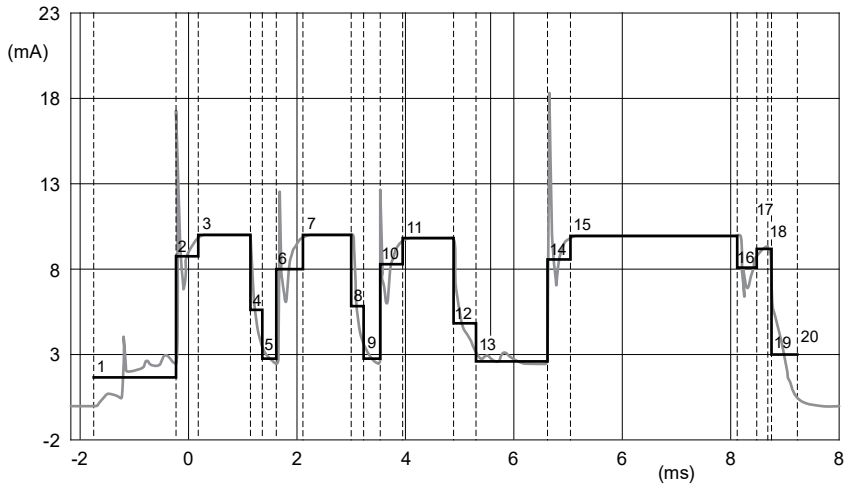

Figure 64. Advertising extension current profile event after DSM2 mode, Bypass mode, coded coded

Table 84. Advertising extension current consumption in Bypass mode, DSM2 mode, coded coded

	Bypass mode	Idd_REG (total consumption)		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Advertising	Pre-Processing	1.500 ms	3.653 mA	5.480 mA-ms
	TX1 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX1 Level	0.656 ms	14.401 mA	9.447 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.182 ms	2.900 mA	0.526 mA-ms
	TX2 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX2 Level	0.656 ms	14.401 mA	9.447 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.182 ms	2.900 mA	0.526 mA-ms
	TX3 Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX3 Level	0.656 ms	14.401 mA	9.447 mA-ms
	TX1 Fall	0.020 ms	13.400 mA	0.268 mA-ms
	MCU Stop	0.182 ms	2.900 mA	0.526 mA-ms
	TX Aux Channel Rise	0.080 ms	13.400 mA	1.072 mA-ms
	TX Aux Channel Level	0.656 ms	14.401 mA	9.447 mA-ms
	TX to RX1 Transition	0.050 ms	13.400 mA	0.670 mA-ms
	RX Aux Channel Level	0.160 ms	14.612 mA	2.338 mA-ms
	RX Aux Channel Fall	0.020 ms	13.400 mA	0.268 mA-ms
	Post-Processing	1.330 ms	4.000 mA	5.320 mA-ms
	Active Consumption	6.609 ms	8.857 mA	58.535 mA-ms
	Charge Integral:16.26 nAh			

Table 85. Advertising extension current consumption in bypass mode, DSM2 (MCU DSM2, flash doze), Coded Coded

	Buck mode	Idd_REG (total consumption)		
	State	Time (ms)	Current (mA)	mA x mS
ADV	Active Consumption	6.609 ms	4.720 mA	31.194 mA-ms
Charge Integral: 8.67 nAh				

Summary table:

Table 86. Advertising Extension summary table

		Idd_REG (total consumption)			
Advertising	State	Time (ms)	Current (mA)	mA x mS	Charge Integral
1 Msps 1 Msps	Buck mode	2.421 ms	4.598 mA	11.132 mA-ms	3.09 nAh
-	Bypass mode	3.268 ms	6.851 mA	3.092 mA-ms	6.22 nAh
1 Msps 2 Msps	Buck mode	2.225 ms	4.097 mA	9.116 mA-ms	2.53 nAh
-	Bypass mode	2.760 ms	6.210 mA	17.135 mA-ms	4.76 nAh
1 Msps coded	Buck mode	2.829 ms	5.442 mA	15.395 mA-ms	4.28 nAh
-	Bypass mode	3.364 ms	9.124 mA	30.688 mA-ms	8.52 nAh
Coded 1 Msps	Buck mode	5.031 ms	3.998 mA	20.114 mA-ms	5.59 nAh
-	Bypass mode	5.031 ms	6.636 mA	33.386 mA-ms	9.27 nAh
Coded 2 Msps	Buck mode	4.014 ms	3.851 mA	15.458 mA-ms	4.29 nAh
-	Bypass mode	4.014 ms	6.433 mA	25.819 mA-ms	7.17 nAh
Coded coded	Buck mode	6.609 ms	4.720 mA	31.194 mA-ms	8.67 nAh
-	Bypass mode	6.609 ms	8.857 mA	58.535 mA-ms	16.26 nAh

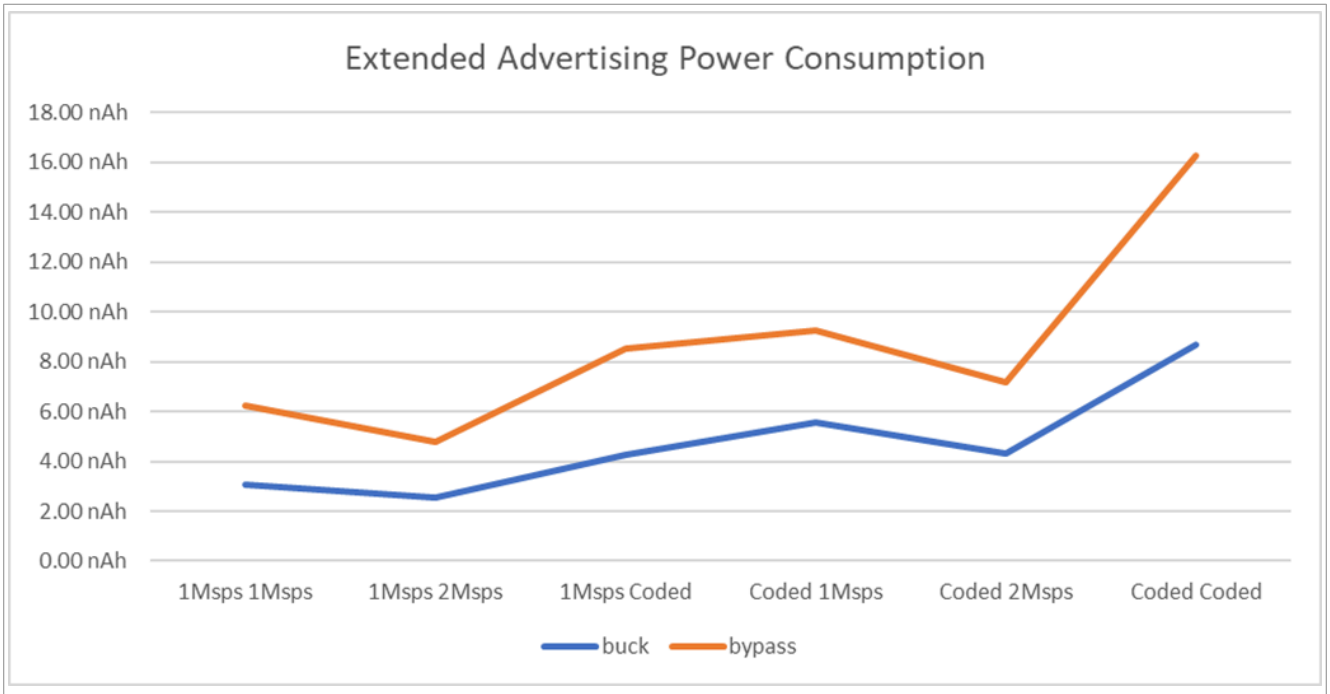

Figure 65. Advertising extension power consumption versus data rate modes

Summary data:

Table 87. Advertising Extension consumption summary table

Advertising Extension	Unit: nAh	Vdd_Reg (V) power supply (Ambient, 25 °C)							
-		1.7 V	1.8 V	2.1 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V
1 Mbit/s 1 Mbit/s	Buck	8.66 nAh	8.34 nAh	4.22 nAh	3.58 nAh	3.39 nAh	3.09 nAh	2.86 nAh	1.81 nAh
-	Bypass	4.56 nAh	4.63 nAh	4.93 nAh	5.39 nAh	5.81 nAh	6.22 nAh	6.54 nAh	6.70 nAh
1 Mbit/s 2 Mbit/s	Buck	7.92 nAh	7.31 nAh	3.73 nAh	3.13 nAh	2.88 nAh	2.53 nAh	2.42 nAh	1.67 nAh
-	Bypass	3.45 nAh	3.50 nAh	3.71 nAh	4.03 nAh	4.38 nAh	4.76 nAh	5.06 nAh	5.39 nAh
1 Mbit/s coded	Buck	11.96 nAh	11.53 nAh	5.83 nAh	4.95 nAh	4.68 nAh	4.28 nAh	3.96 nAh	2.51 nAh
-	Bypass	6.25 nAh	6.34 nAh	6.75 nAh	7.39 nAh	7.96 nAh	8.52 nAh	8.96 nAh	9.18 nAh
Coded 1 Mbit/s	Buck	15.63 nAh	15.07 nAh	7.62 nAh	6.47 nAh	6.12 nAh	5.59 nAh	5.17 nAh	3.28 nAh
-	Bypass	6.80 nAh	6.90 nAh	7.35 nAh	8.04 nAh	8.67 nAh	9.27 nAh	9.75 nAh	9.99 nAh
Coded 2 Mbit/s	Buck	12.01 nAh	11.58 nAh	5.86 nAh	4.97 nAh	4.70 nAh	4.29 nAh	3.97 nAh	2.52 nAh
-	Bypass	5.26 nAh	5.33 nAh	5.68 nAh	6.22 nAh	6.70 nAh	7.17 nAh	7.54 nAh	7.72 nAh
Coded coded	Buck	24.23 nAh	23.36 nAh	11.81 nAh	10.03 nAh	9.49 nAh	8.67 nAh	8.02 nAh	5.08 nAh
-	Bypass	11.93 nAh	12.09 nAh	12.88 nAh	14.09 nAh	15.19 nAh	16.26 nAh	17.09 nAh	17.51 nAh

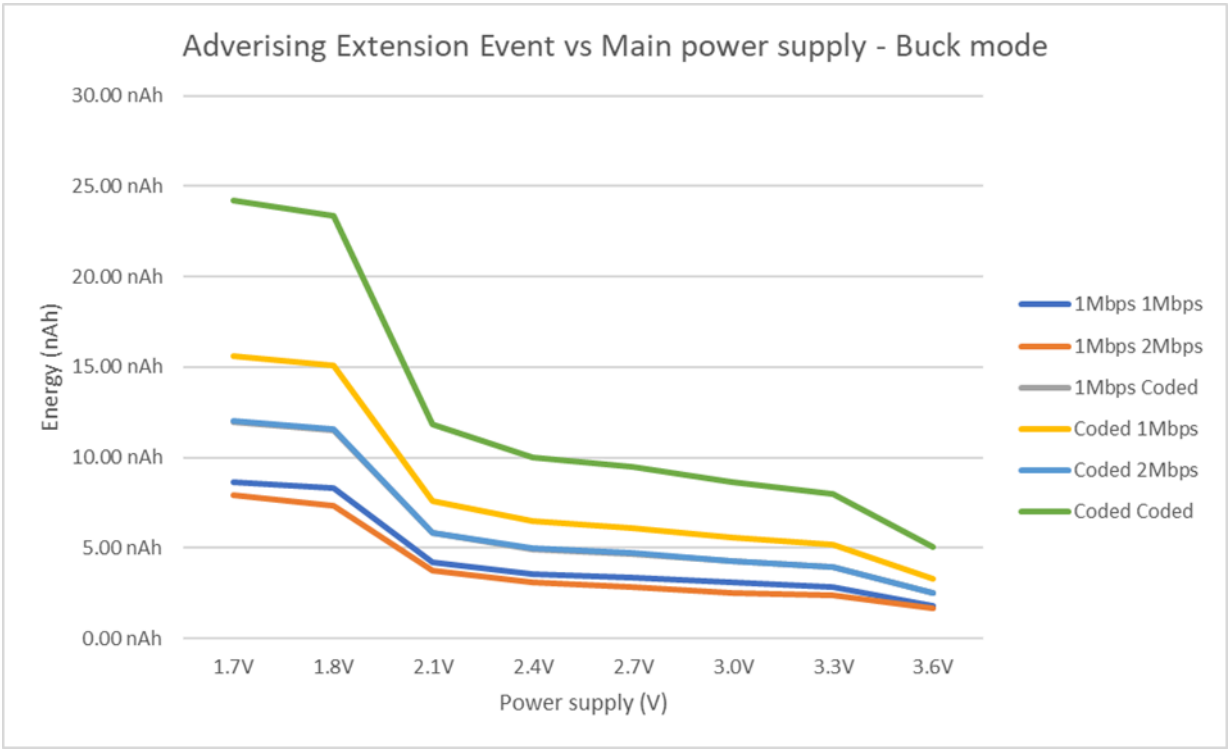

Figure 66. Advertising extension consumption event, buck mode

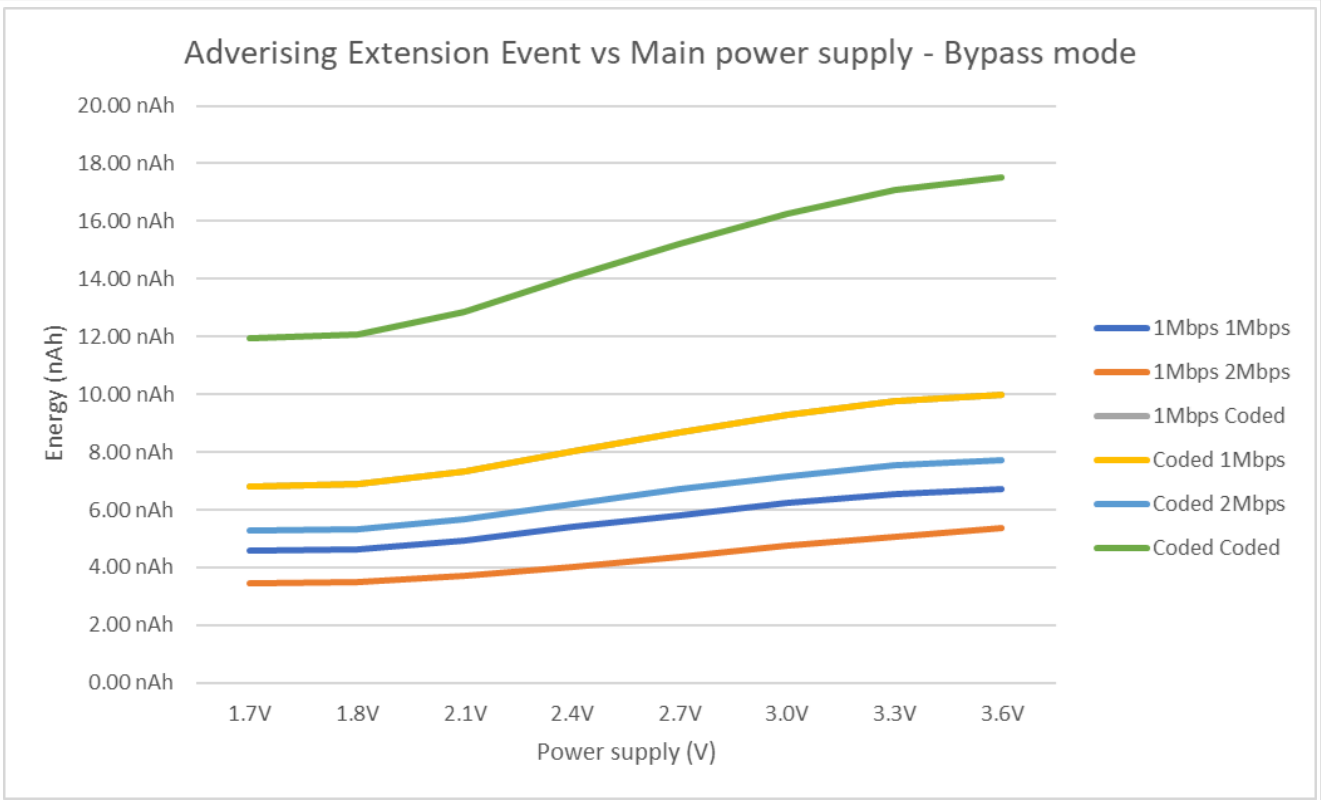

Figure 67. Advertising extension consumption event, bypass mode

5.4 Scan extension

Using the steps listed in Section 4.2, partial Bluetooth LE scenario (Low-power application) has captured, as shown in Figure 68. The main events and phases are listed in Table 88 including all the plots that follows depicts current.

Both use cases are used:

- DSM2 Mode is activated between the scan events.

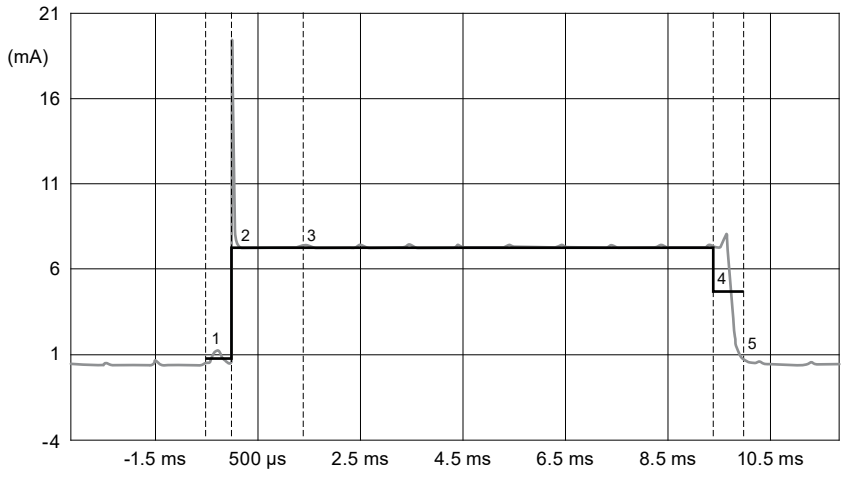

Figure 68. Current consumption - Scan extension event period

Table 88. Scan extension events

No.	Event
1	Pre-processing
2	RX warmup
3	Active RX
4	RX warm down
5	Post-processing

Figure 69 shows the current consumption during the Scan extension event using data rate at 1Mbps and coded (S2, 500 kbit/s). Buck made and Bypass mode graphs are provided as example.

The binary file settings used are:

- 48 MHz clock
- Scan extension
- Connectable

Buck mode: Wake-up from Low-power mode `Deep Sleep mode 2`

Bypass mode: Wake-up from Low-power mode `Deep Sleep mode 2`

Test environment: Scan extension 1 Mbit/s 1 Mbit/s

Table 89. Test environment

DC-to-DC mode	Buck	Bypass
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	na	
MCU clock mode	48 MHz	
RAM size	128 k	
Data rate	1 Msps 1 Mbit/s	
Payload	empty	
Connectable	Yes	
Flash	Doze	
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

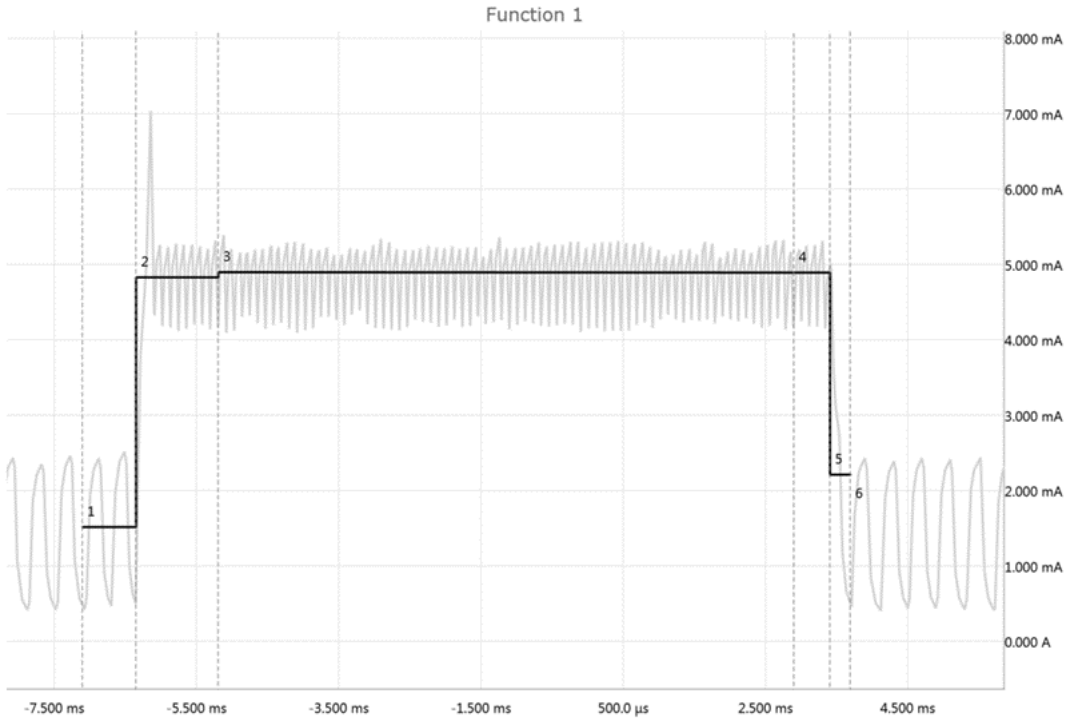

Figure 69. Scan extension current profile event after DSM2 mode, Buck mode, 1 Mbit/s 1 Mbit/s

Table 90. Scan extension current consumption in Buck mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s 1 Msps

Scanning				
Buck	**Scanning windows**	**4.00 ms**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Scan	Scan pre-processing	1.550 ms	2.660 mA	4.123 mA-ms
	RX warm-up	0.160 ms	9.260 mA	1.482 mA-ms
	RX Scan	4.000 ms	4.860 mA	19.440 mA-ms
	RX warm-down	0.200 ms	8.900 mA	1.780 mA-ms
	Scan Post-process	0.700 ms	3.530 mA	2.471 mA-ms
	Active Consumption	6.610 ms	Avg= 5.842 mA	29.296 mA-ms
Charge Integral: 8.14 nAh				

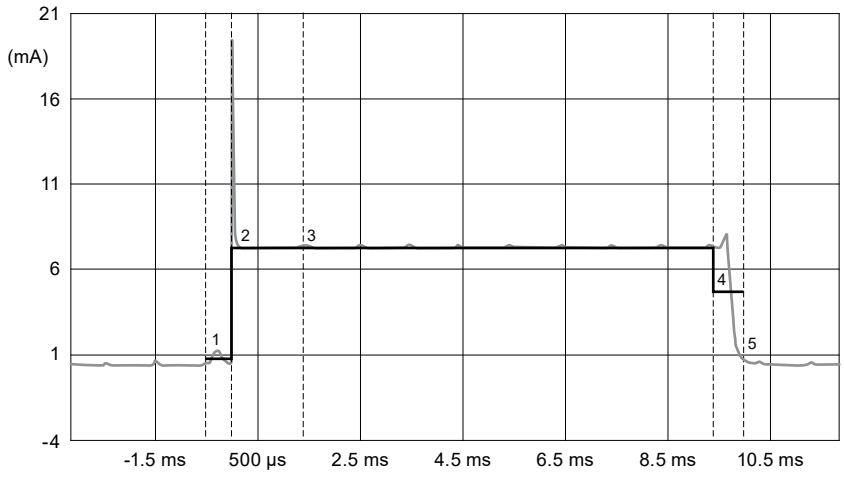

Figure 70. Scan extension current profile event after DSM2 mode, Bypass mode, 1 Mbit/s 1 Mbit/s

Figure 76:

Table 91. Scan extension current consumption in Bypass mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s 1 Msps

Scanning				
Buck	**Scanning windows**	**4.000 ms**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Scan	Scan pre-processing	2.000 ms	2.170 mA	4.340 mA-ms
	RX warm-up	0.160 ms	13.930 mA	2.229 mA-ms
	RX Scan	4.000 ms	9.700 mA	38.800 mA-ms
	RX warm-down	0.200 ms	8.130 mA	1.626 mA-ms
	Scan Post-process	0.850 ms	2.700 mA	2.295 mA-ms
	Active Consumption	7.210 ms	Avg= 7.326 mA	49.290 mA-ms
Charge Integral: 13.69 nAh				

Test environment: Scan extension 1 Mbit/s Coded

Table 92. Test environment

DC-to-DC mode	**Buck**	**Bypass**
Supply	**Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V**	**Vdd_RF = 3 V Vdd_LDO_Core=3 V**
RF output power	na	
MCU clock mode	48 MHz	
RAM size	128 k	
Data rate	1 Msps Coded (LR S2)	
Payload	empty	
Connectable	Yes	
Flash	Doze	

Table 92. Test environment*...continued*

DC-to-DC mode	Buck	Bypass
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	Vdd_RF = 3 V Vdd_LDO_Core=3 V
MCU	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low-power (PRC2 RC2 release)	

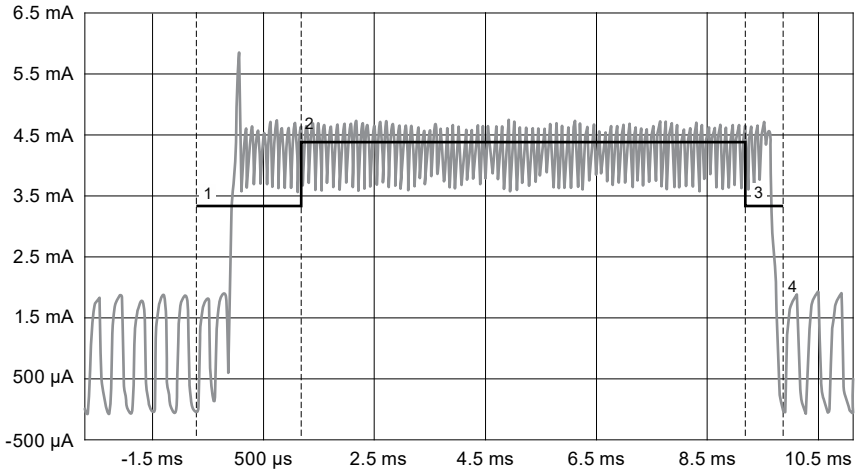

Figure 71. Scan extension current profile event after DSM2 mode, Buck mode, 1 Mbit/s Coded

Table 93. Scan extension current consumption in Buck mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s Coded

Scanning				
Buck	**Scanning Windows**	**4.000 ms**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Scan	Scan pre-processing	1.550 ms	2.690 mA	4.170 mA-ms
	RX warm-up	0.160 ms	9.800 mA	1.568 mA-ms
	RX Scan	4.000 ms	4.860 mA	19.440 mA-ms
	RX warm-down	0.200 ms	6.270 mA	1.254 mA-ms
	Scan Post-process	0.700 ms	1.947 mA	1.363 mA-ms
	Active Consumption	6.610 ms	Avg= 5.113 mA	27.794 mA-ms
Charge Integral: 7.72 nAh				

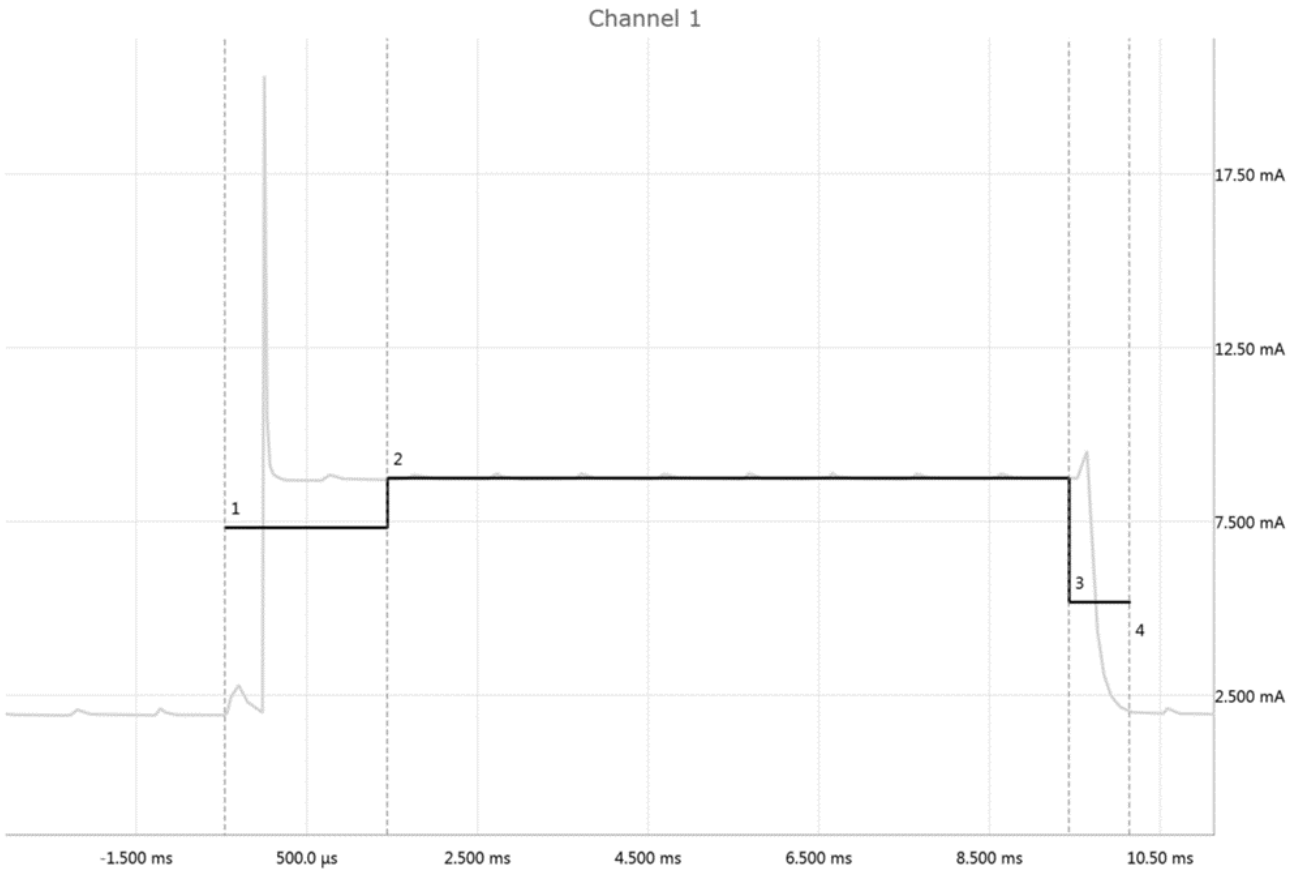

Figure 72. Scan extension current profile event after DSM2 mode, Bypass mode, 1 Mbit/s Coded

Table 94. Scan extension current consumption in Bypass mode, DSM2 (MCU DSM2, flash doze), 1 Mbit/s Coded

Scanning				
Buck	**Scanning windows**	**4.000 ms**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Scan	Scan pre-processing	2.000 ms	2.183 mA	4.366 mA-ms
	RX warm-up	0.160 ms	12.900 mA	2.064 mA-ms
	RX Scan	4.000 ms	9.880 mA	39.520 mA-ms
	RX warm-down	0.200 ms	5.300 mA	1.060 mA-ms
	Scan Post-process	0.850 ms	2.100 mA	1.785 mA-ms
	Active Consumption	7.210 ms	Avg= 6.473 mA	48.795 mA-ms
Charge Integral: 13.55 nAh				

Timing data:

Table 95. Scanning extension timing table

No.	State	Timing (ms)			
		Buck		Bypass	
		DSM2		DSM2	
		1M1M	1MCoded	1M1M	1MCoded
1	Pre processing	1.550 ms	1.550 ms	2.000 ms	2.000 ms
2	RX warm-up	0.160 ms	0.160 ms	0.160 ms	0.160 ms
3	RX active	4.000 ms	4.000 ms	4.000 ms	4.000 ms
4	RX warm down	0.200 ms	0.200 ms	0.200 ms	0.200 ms
5	Post-processing	0.700 ms	0.700 ms	0.850 ms	0.850 ms
6	Total	6.610 ms	6.610 ms	7.210 ms	7.210 ms

Table 96. Scanning extension consumption table

No.	State	Consumption (mA)			
		Buck		Bypass	
		DSM2		DSM2	
		1M1M	1MCoded	1M1M	1MCoded
1	Pre processing	2.660 mA	2.690 mA	2.170 mA	4.340 mA
2	RX warm-up	9.260 mA	9.800 mA	13.930 mA	2.229 mA
3	RX active	8.800 mA	8.900 mA	9.700 mA	38.800 mA
4	RX warm down	8.900 mA	6.270 mA	8.130 mA	1.626 mA
5	Post-processing	3.530 mA	1.947 mA	2.700 mA	2.295 mA
6	Total	6.630 mA	5.921 mA	7.326 mA	49.290 mA

Summary data:

Table 97. Scanning extension consumption summary table

Scan	Unit: nAh	1.7 V	1.8 V	2.1 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V
Scan 1 Mbit/s	Buck	7.55 nAh	7.54 nAh	7.44 nAh	7.62 nAh	7.30 nAh	6.54 nAh	6.01 nAh	5.62 nAh
	Bypass	12.94 nAh	12.89 nAh	12.79 nAh	13.10 nAh	12.78 nAh	12.38 nAh	12.34 nAh	12.32 nAh
Scan Ext. 1 Mbit/s	Buck	9.34 nAh	9.38 nAh	9.32 nAh	9.45 nAh	9.08 nAh	8.14 nAh	7.49 nAh	7.00 nAh
	Bypass	14.31 nAh	14.26 nAh	14.14 nAh	14.49 nAh	14.13 nAh	13.69 nAh	13.67 nAh	13.64 nAh
Scan Ext. Coded 500 kbit/s	Buck	8.89 nAh	8.92 nAh	8.81 nAh	9.00 nAh	8.62 nAh	7.72 nAh	7.17 nAh	6.68 nAh
	Bypass	14.00 nAh	13.95 nAh	13.88 nAh	14.17 nAh	13.85 nAh	13.55 nAh	13.47 nAh	13.48 nAh

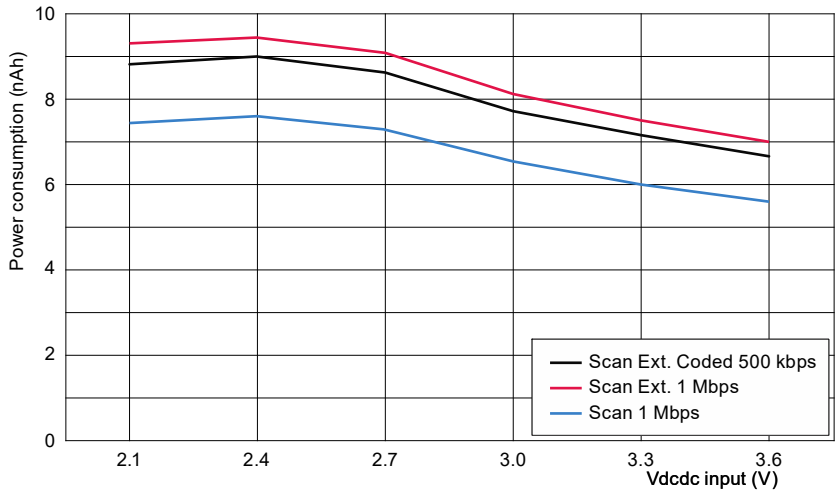

Figure 73. Scanning extension consumption event, buck mode

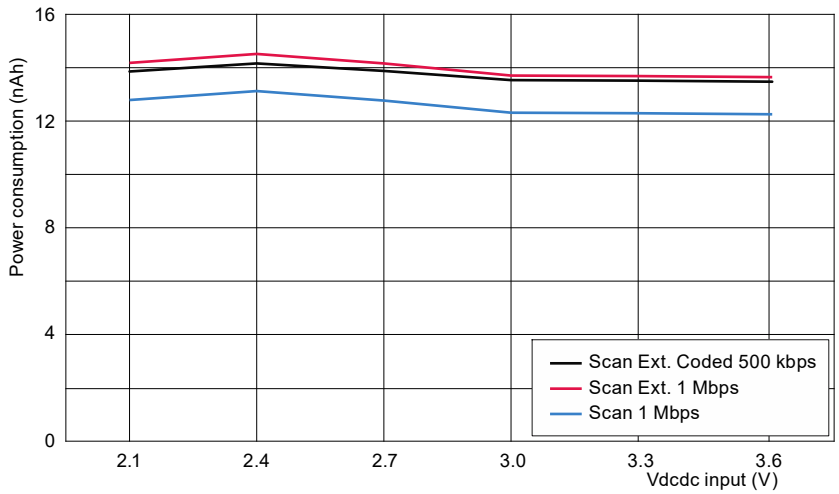

Figure 74. Scanning extension consumption event, bypass mode

5.5 Channel selection algorithm #1 and #2

Channel selection algorithm #1 is the legacy method that only supports channel selection for connection events. Channel selection algorithm #1 consists of two stages: calculation of the unmapped channel index followed by mapping this index to a data channel index from the set of used channels.

Channel selection algorithm #2 supports channel selection for both connection events and periodic advertising packets. At the start of an event, which can be a connection event or a periodic advertising packet, the algorithm described here generates an event channel index (which is a data channel index or secondary advertising channel index, as appropriate). Some of the CSA #2 claims are

- Channel selection algorithm #2 (CSA #2) is a more complex and harder to track algorithm for obtaining the channel index for the next event.
- It is more effective at avoiding interference and multi-path fading effects than Channel Selection Algorithm #1, especially in high-throughput use cases.

5.6 High duty cycle advertising

High-duty cycle advertising able faster connection setup. No specific power consumption is done for this mode.

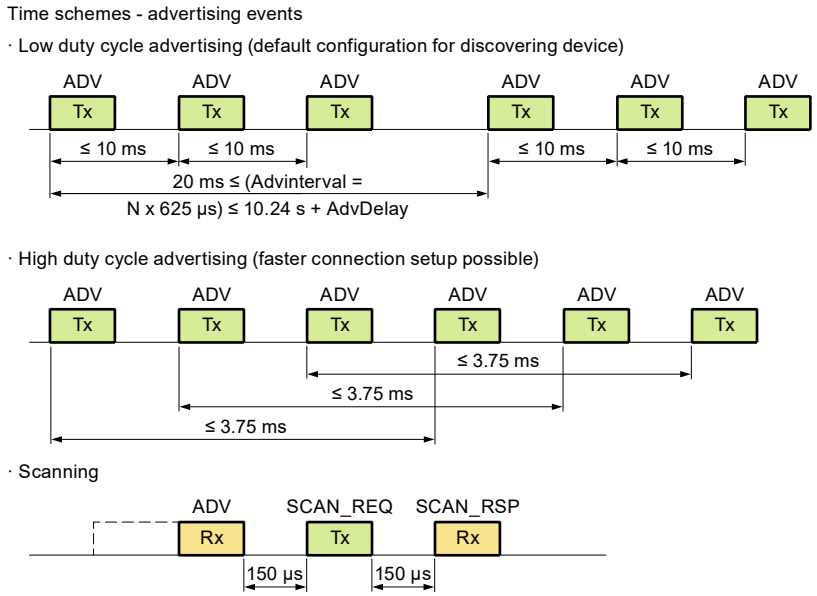

Figure 75. Low and high duty cycle advertising

5.7 Reports

Table 98 provide power consumption at 3.0 V in buck and bypass modes, at ambient temperature (+25 °C)

Table 98. SoC measurements summary table (ambient temperature, 3 V)

Deep sleep mode	Regul.	RAM retention	Core Main Power domain	Core Wake up power domain	Core RF power domain	Peripherals	DC-to-DC	Current consumption at 3 V
Deep Sleep 1	all are in Low-power mode	16 K RAM retained	Deep Sleep	Deep Sleep	Deep Sleep	Disabled	Buck	1.99 µA
Deep Sleep 1	all are in Low-power mode	16 K RAM retained	Deep Sleep	Deep Sleep	Deep Sleep	Disabled	Bypass	3.6 µA

Note: **Active mode: Buck mode (Vdcdc_in=3 V,), clock 48 MHz, CM33* `Deep Sleep mode 2`

Note: *Condition of measurement: Vdcdc_in=3 V, 25 °C (Ambient)*

Table 99. Wake-up timing summary table

Type of wake-up	Timing (ms) (HW+SW initialization)	Power consumption (mA) (HW+SW initialization)
First Reset (POR)	900 ms	4.8 mA
Other reset	108 ms	7.65 mA

Power consumption summary tables:

Table 100. Event power consumption summary table

1 event, Vdcdc_in=3 V, 25 °C		DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
Advertising	buck	3.458 ms	4.973 mA	4.78 nAh
	bypass	3.993 ms	6.677 mA	7.41 nAh
MCU	buck	0.280 ms	1.800 mA	0.14 nAh
	bypass	0.280 ms	2.900 mA	0.23 nAh
Connect-1Mbps	buck	1.536 ms	4.361 mA	1.86 nAh
	bypass	1.536 ms	5.598 mA	2.39 nAh
Connect-2Mbps	buck	1.456 ms	3.383 mA	1.37 nAh
	bypass	1.456 ms	4.071 mA	1.65 nAh
Connect-500 kbit/s	buck	1.712 ms	4.626 mA	2.20 nAh
	bypass	1.712 ms	7.716 mA	3.67 nAh
Connect-125 kbit/s	buck	2.768 ms	5.495 mA	4.23 nAh
	bypass	2.768 ms	10.310 mA	7.93 nAh
Scan	buck	6.150 ms	5.672 mA	10.08 nAh
	bypass	6.150 ms	21.829 mA	22.01 nAh

Table 101. Advertising Power consumption summary table

48 MHz clock using 32MHx Crystal	Buck mode Consumption (3 V)	Bypass mode consumption (3 V)
	DSM2	DSM2
	T= 25 °C	
Advertising consumption on 1 event at +0 dBm	3.458 ms	3.993 ms
	4.973 mA	6.677 mA
	4.78 nAh	7.41 nAh
Advertising consumption details at +0 dBm		
TX Active (+0 dBm) – MCU stop	5.060 mA	11.501 mA
RX Active - MCU STOP	5.148 mA	11.712 mA
TX Warm-up - MCU STOP	5.040 mA	10.500 mA
TX Warm-down - MCU STOP	5.040 mA	10.500 mA
RX warm-up - MCU STOP	5.040 mA	10.500 mA
RX warm-down - MCU STOP	5.040 mA	10.500 mA
TX to RX transition - MCU STOP (advertising event)	5.040 mA	10.500 mA

Table 102. Pre-Post processing, MCU consumption summary table

48 MHz FEE Mode using 32MHx Crystal	Buck mode Consumption (3 V)	Bypass mode Consumption (3 V)
	DSM2	
	T= 25 °C	
ADV pre-processing	2.900 mA	2.400 mA
CONN pre-processing - 1 Mbit/s	4.361 mA	5.598 mA
CONN pre-processing - 2 Mbit/s	3.383 mA	4.071 mA
CONN pre-processing - LRS2	4.626 mA	7.716 mA

Table 102. Pre-Post processing, MCU consumption summary table...*continued*

48 MHz FEE Mode using 32MHx Crystal	Buck mode Consumption (3 V)	Bypass mode Consumption (3 V)
	DSM2	
	T= 25 °C	
CONN pre-processing - LRS8	5.495 mA	10.310 mA
Radio Post-processing	2.750 mA	4.000 mA
MCU STOP	1.800 mA	2.900 mA

Table 103. MCU power consumption summary table

MCU DSM2 consumption	Buck mode consumption (3 V)	Bypass mode consumption (3 V)
	DSM2	
	T= 25 °C	
Timing period (ms)	0.280 ms	0.280 ms
Consumption (mA)	1.800 mA	2.900 mA
MCU DSM2consumption (nAh)	0.140 nAh	0.225 nAh

Timings summary table:

Table 104. Advertising and connection timing summary table

Radio/Profile Timing Parameters (ms)	Buck mode Consumption (3 V)	Bypass mode consumption (3 V)
48 MHz clock using 32 MHz crystal	DSM2	DSM2
	T= 25 °C	
ADV Pre-processing Time - 1 Mbit/s	0.650 ms	0.650 ms
ADV Post-processing Time - 1 Mbit/s	0.275 ms	0.275 ms
Conn Pre-processing Time – 1 Mbit/s	0.750 ms	0.750 ms
Conn Post-processing Time - 1 Mbit/s	0.360 ms	0.360 ms
Conn Pre-processing Time - 2 Mbit/s	0.750 ms	0.750 ms
Conn Post-processing Time - 2 Mbit/s	0.360 ms	0.360 ms
Conn Pre-processing Time - 500 kbit/s	0.750 ms	0.750 ms
Conn Post-processing Time - 500 kbit/s	0.360 ms	0.360 ms
Conn Pre-processing Time - 125 kbit/s	0.750 ms	0.750 ms
Conn Post-processing Time - 125 kbit/s	0.360 ms	0.360 ms
SCAN Pre-processing Time - 125 kbit/s	1.900 ms	1.900 ms
SCAN Post-processing Time - 125 kbit/s	0.150 ms	0.150 ms

6 Revision history

Table 105 summarizes the revisions to this document.

Table 105. Revision history

Revision number	Release date	Description
1	18 September 2023	Tables are updated with new figures, DSM1 is changed to DSM2.
0	21 December 2022	Initial public release

7 Legal information

7.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. - NXP B.V. is not an operating company and it does not distribute or sell products.

7.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com

Date of release: 18 September 2023
Document identifier: AN13230