AN12776

PSI5 Normal Mode Initialization and Main Features for the FXLS93xxx

Rev. 2.1 — 8 January 2021 Application note

1 Introduction

The purpose of this document is to describe the PSI5 Normal Mode initialization and main features for the FXLS93xx0 single channel and the FXLS93xxx dual channel inertial sensors.

2 Applicable Parts

This document applies to the following NXP sensors:

Table 1. Applicable parts

FLXS93xxx	uThornapple	Dual Channel PSI5 Inertial Sensor
FLXS93xxx	uLaurel	Single Channel PSI5 Inertial Sensor

3 Definition List

Table 2. Definition list

Term	Definition
Analog Self-Test	A method to test the acceleration signal chain by electrostatically deflecting the transducer proof mass and measuring the device output.
Digital Self-Test	A method to test the digital portion of the acceleration signal chain by forcing a value or a sequence of values at the output of the analog to digital converter and measuring the device output.
DSP	Digital Signal Processing Block
POR	Power On Reset
PSI5	Peripheral Sensor Interface, 5th Generation. A single master, multiple slave communication interface that provides both slave power and communication on a 2-wire bus.

4 Further Assistance

For further assistance please contact a local NXP sales representative.

5 References

- FXLS93xxx Data sheet, latest revision: uThornapple Datasheet
- FXLS93xxx Data sheet, latest revision: uLaurel Datasheet
- PSI5 Technical Specification Version 2.1, Dated October 8, 2012

6 Revision History

Table 3. Revision history

Rev. No.	Date	Description
1.0	20200311	Initial Release.
2.0	20200401	Added Daisy Chain Mode Diagram Section 12.
2.1	20210108	Corrected Default COMMTYPE from 5 to 1 in Section 7. Corrected Typo in Section 10.2.

7 Device Type

To use a device using the PSI5 Normal Mode, the device must be ordered as a PSI5 communication device with the COMMTYPE register set to 0x01.

Un-programmed FXLS93xxx PSI5 devices include a default PSI5 transmission mode. The devices will respond to PSI5 sync pulses and transmit data in PSI5-P16C-500/2L mode with the minimum user gain and the default 400Hz, 4-Pole low pass filter.

Device can be programmed using PSI5 Programming Mode (refer to AN12162). A table of possible part numbers are listed in Table 4 below.

Table 4. FXLS93xxx device type part numbers

Part number	Description
FXLS93322	Dual Channel, X-Axis, Medium g, Y-Axis, Medium g, PSI5 Enabled
FXLS93422	Dual Channel, X-Axis, Medium g, Z-Axis, Medium g, PSI5 Enabled
FXLS93722	Dual Channel, Y-Axis, Medium g, Z-Axis, Medium g, PSI5 Enabled
FXLS93333	Dual Channel, X-Axis, High g, Y-Axis, High g, PSI5 Enabled
FXLS93433	Dual Channel, X-Axis, High g, Z-Axis, High g, PSI5 Enabled
FXLS93433	Dual Channel, Y-Axis, High g, Z-Axis, High g, PSI5 Enabled
FXLS93220	Single Channel, X-Axis, Medium g, PSI5 Enabled
FXLS93230	Single Channel, X-Axis, High g, PSI5 Enabled
FXLS93120	Single Channel, Z-Axis, Medium g, PSI5 Enabled
FXLS93130	Single Channel, Z-Axis, High g, PSI5 Enabled
FXLS93620	Single Channel, Y-Axis, Medium g, PSI5 Enabled
FXLS93630	Single Channel, ZY-Axis, High g, PSI5 Enabled

8 Application Schematics

8.1 FXLS93xxx PSI5 universal/parallel mode application schematic

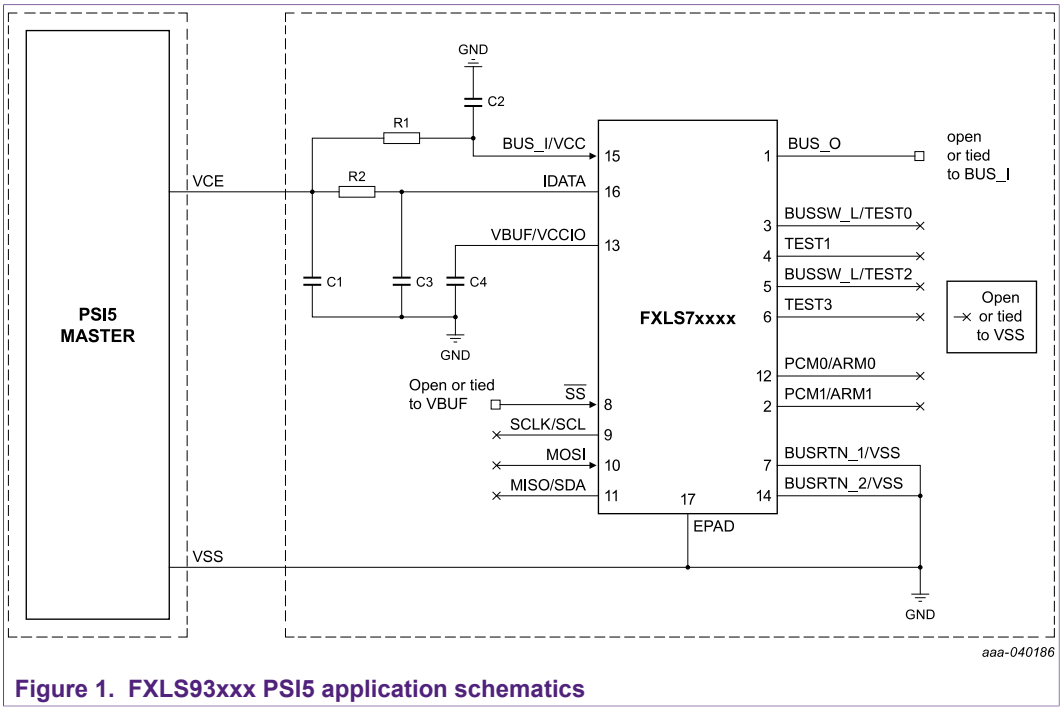

Figure 1. FXLS93xxx PSI5 application schematics

Table 5. Recommended external components for PSI5 mode

Reference designator	Component type	Description	Comment
R1	General Purpose	82 Ω, 5%, 200ppm	The optimal value of this component should be determined by the system level communication, EMC and ESD testing.For proper device function the minimum value can be 0 Ohms. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 89.0 Ohms.
R2	General Purpose	27 Ω, 5%, 200ppm	The optimal value of this component should be determined by the system level communication, EMC and ESD testing.For proper device function the minimum value can be 0 Ohms. The maximum value is determined by the minimum bus voltage provided at the module pin To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 66.6 Ohms. If the low response current is used, the maximumresistance including all tolerances is 133 Ohms.
C1	Ceramic	2.2 nF, 10%, 10V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing.
C2	Ceramic	15 nF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication and EMC testing.

Reference designator	Component type	Description	Comment
C3	Ceramic	470 pF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication and EMC testing.
C4	Ceramic	0.47 µF, 10%, 50V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22µF. The maximum specified value including all tolerances is 2µF.

9 Apply Power to the FXLS93xxx

Power must be applied to the FXLS93xxx with the ramp rates specified in the datasheet. The device is verified to properly startup with ramp rates from 10 V/s to 10 V/µs.

The supply voltage for the device is applied through the PSI5 network shown in Figure 1. As specified in the datasheet, the voltage at the BUS_I pin during PSI5 must be between 4.2 V and 16.5 V excluding PSI5 synchronisation pulse.

The example in this document uses a supply voltage of 11.0 V with a current limit of 125 mA. The supply ramp is shown in Figure 2.

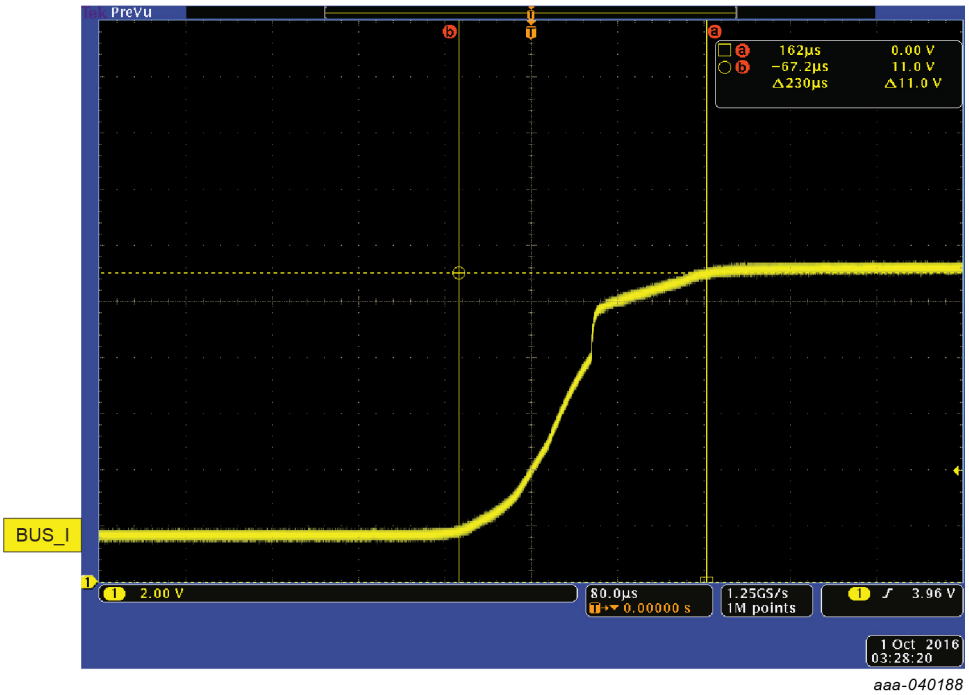

Figure 2. Example PSI5 supply ramp

10 PSI5 Initialization Phases

Following power-up, the device proceeds through an initialization process which is divided into three phases:

- Initialization Phase 1: No Data transmissions occur
- Initialization Phase 2: Sensor self test and transmission of configuration information

- Initialization Phase 3: Transmission of the Sensor Busy and/or Sensor Ready/Sensor Defect messages

Once initialization is completed the device begins Normal Mode operation, which continues as long as the supply voltage remains within the specified limits.

Figure 3 shows the timing for internal and external initialization in synchronous mode.

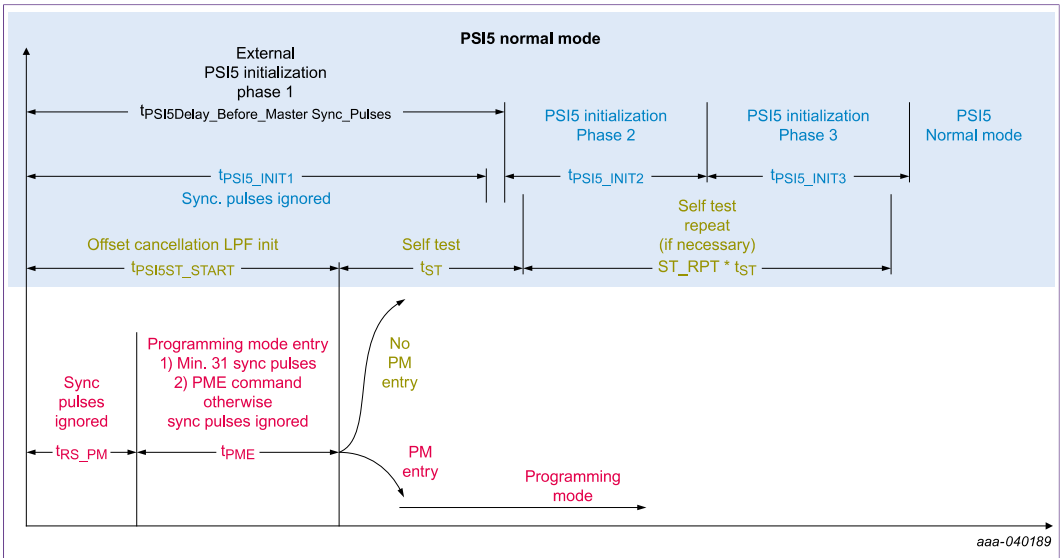

Figure 3. Example PSI5 initialization timing diagram

10.1 Initialization Phase 1

During PSI5 Initialization Phase 1, the device begins internal initialization and self checks, but transmits no data. Initialization begins with the sequence below:

- Internal Delay to ensure analog circuitry has stabilized.
- Offset Cancellation Low Pass Filter Initialization begins.

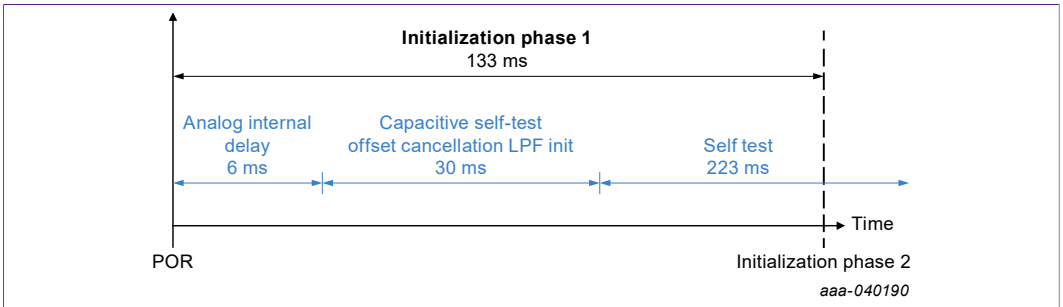

Figure 4. Initialization Phase 1 timing diagram

In Initialization Phase 1 for normal mode, sensor can accept but ignore synchronisation pulse.

10.2 Initialization Phase 2

During Initialization Phase 2, sensor identification data are transmitted. Figure 5 shows the timing for Initialization Phase 2. Self test is repeated up to ST_RPT times if a failure occurs during Initialization Phase 1 in order to avoid the type of invalid inputs that may

occur during initialization. Self test terminates successfully after one successful self test sequence.

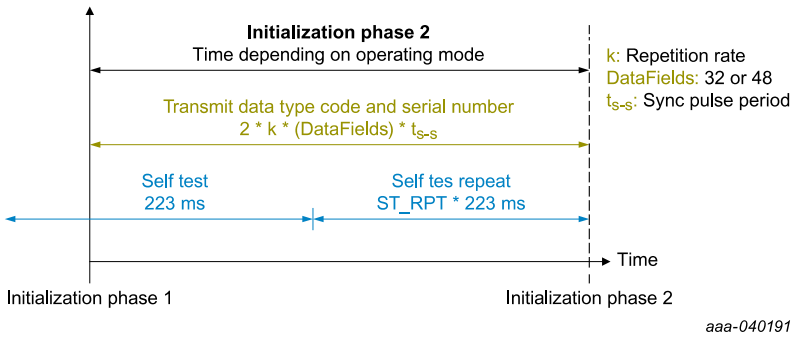

Figure 5. Initialization Phase 2 timing

Table 6 and Table 7 show the data formatting for Initialization Phase 2.

Table 6. Dual axis device: Initialization Phase 2 data formatting

16-bit data value	10-bit data value	Description
87C0	21F	Initialization Data Codes 10-Bits Status Data Nible 1-16
. . .	. . .	
8400	210	
83C0	20F	Initialization Data IDs Block ID 1-16
. . .	. . .	
8000	200	

Table 7. Single axis device: Initialization Phase 2 data formatting

16-bit data value	10-bits data value	Description
87FF	21F	Initialization Data Codes 10-Bits Status Data Nible 1-16
. . .	. . .	
8400	210	
83FF	20F	Initialization Data IDs Block ID 1-16
. . .	. . .	
8000	200	

Using 10-bit data

Block ID goes from 0x200 to 0x20F – four last LSB correspond to the ID number.

Data Nibbles goes from 0x210 to 0x21F – four last LSB correspond to the Data Nibble.

Data Decoding Example

Block ID = 0x200 = 0b10 0000 0000 → ID Number = 0b0000 = 0

Data Nibble = 0x214 = 0b10 0001 0100 → Data Nibble = 0b0100 = 4

Using 16-bit data

Block ID goes from 0x8000 to 0x83C0 – Bits[9-6] correspond to the ID number.

Data Nibbles goes from 0x8400 to 0x87C0 – Bits[5-2] correspond to the Data Nibble.

Data Decoding Example

Block ID = 0x83C0 = 0b1000 0011 1100 0000 → ID Number = 0b1111 = 15

Data Nibble = 0x8784 = 0b1000 0111 1000 0100 → Data Nibble = 0b0001 = 1

The number of nibbles transmitted (DataFields) during Initialization Phase 2 depends on the configuration INIT2_EXT bit in register PSI5_CFG at address 0x25. By default this bit is set to 0 and 32 data nibbles are transmited. If this bit is set to 1, phase 2 data is extended to 48 data nibbles.

PSI5 Field ID #	PSI5 Nibble ID #	Page Address	PSI5 Nibble Address	Register Address	Description	Value
F1	D1	0	0000	USERDATA_0[7:4]	User Specific Data	User
F2	D2, D3		0001, 0010	NA	Number of Data Blocks: 32: INIT2_EXT=0, 48: INIT2_EXT=1	0010 0000 or 0011 0000
F3	D4, D5		0011, 0100	USERDATA_9[3:0], USERDATA_9[7:4]	User Specific Data	User
F4	D6, D7		0101, 0110	USERDATA_A[3:0], USERDATA_A[7:4]	User Specific Data	User
F5	D8		0111	USERDATA_B[3:0]	User Specific Data	User
	D9		1000	USERDATA_B[7:4]	User Specific Data	User
F6	D10		1001	USERDATA_C[3:0]	User Specific Data	User
	D11		1010	USERDATA_C[7:4]	User Specific Data	User
F7	D12		1011	USERDATA_D[3:0]	User Specific Data	User
	D13		1100	USERDATA_D[7:4]	User Specific Data	User
	D14		1101	USERDATA_E[3:0]	User Specific Data	User
F8	D15		1110	USERDATA_7[3:0]	User Specific Data	User
	D16		1111	USERDATA_7[7:4]	User Specific Data	User
	D17	1	0000	USERDATA_8[3:0]	User Specific Data	User
	D18		0001	USERDATA_8[7:4]	User Specific Data	User
F9	D19		0010	SN4[7:4] or USERDATA_6[7:4]	Data determined by PSI5_INIT2_D19 in TIMING_CFG2 register	User
	D20		0011	SN4[3:0] or USERDATA_6[3:0]	Data determined by PSI5_INIT2_D19 in TIMING_CFG2 register	User
	D21		0100	SN3[7:4]	Device Serial Number	Factory
	D22		0101	SN3[3:0]	Device Serial Number	Factory
	D23		0110	SN2[7:4]	Device Serial Number	Factory
	D24		0111	SN2[3:0]	Device Serial Number	Factory
	D25		1000	SN1[7:4]	Device Serial Number	Factory
	D26		1001	SN1[3:0]	Device Serial Number	Factory
	D27		1010	SN0[7:4]	Device Serial Number	Factory
	D28		1011	SN0[3:0]	Device Serial Number	Factory
	D29		1100	PN1[3:0]	Device Part Number	Factory
	D30		1101	PN0[7:4]	Device Part Number	Factory
	D31		1110	PN0[3:0]	Device Part Number	Factory
	D32		1111	USERDATA_E[7:4]	User Specific Data	User
F10	D33	2	0000	CH0_STAVG_P[7:4]	Channel 0 Positive Self Test, High Nibble	Varies
	D34		0001	CH0_STAVG_P[3:0]	Channel 0 Positive Self Test, Low Nibble	Varies
	D35		0010	CH0_STOFFSET_P[7:4]	Channel 0 Post Positive Self Test Offset, High Nibble	Varies
	D36		0011	CH0_STOFFSET_P[3:0]	Channel 0 Post Positive Self Test Offset, Low Nibble	Varies
	D37		0100	CH0_STAVG_N[7:4]	Channel 0 Negative Self Test, High Nibble	Varies
	D38		0101	CH0_STAVG_N[3:0]	Channel 0 Negative Self Test, Low Nibble	Varies
	D39		0110	CH0_STOFFSET_N[7:4]	Channel 0 Post Negative Self Test Offset, High Nibble	Varies
	D40		0111	CH0_STOFFSET_N[3:0]	Channel 0 Post Negative Self Test Offset, Low Nibble	Varies
	D41		1000	CH1_STAVG_P[7:4]	Channel 1 Positive Self Test, High Nibble	Varies
	D42		1001	CH1_STAVG_P[3:0]	Channel 1 Positive Self Test, Low Nibble	Varies
	D43		1010	CH1_STOFFSET_P[7:4]	Channel 1 Post Positive Self Test Offset, High Nibble	Varies
	D44		1011	CH1_STOFFSET_P[3:0]	Channel 1 Post Positive Self Test Offset, Low Nibble	Varies
	D45		1100	CH1_STAVG_N[7:4]	Channel 1 Negative Self Test, High Nibble	Varies
	D46		1101	CH1_STAVG_N[3:0]	Channel 1 Negative Self Test, Low Nibble	Varies
	D47		1110	CH1_STOFFSET_N[7:4]	Channel 1 Post Negative Self Test Offset, High Nibble	Varies
	D48		1111	CH1_STOFFSET_N[3:0]	Channel 1 Post Negative Self Test Offset, Low Nibble	Varies

D33-D48 Transmitted if INIT2_EXT = 1

Figure 6. Dual axis device: Initialization Phase 2 data

Table 8 shows repetition rate according to the selected operating mode

Table 8. Repetition rate

Operating mode	Repetition rate
Synchronous	4
Asynchronous	8

Initialization Phase 2 Time Calculation Example

INIT2_EXT = 1

Synchronous Mode

t_{S_S} = Synchronisation Pulse Period = 500 µs

T_{Phase2} = *2 * repetition rate* # of transmitted data * t_{S_S} = 2 * 4 * 48 * 500* = 192 ms

10.3 Initialization Phase 3

During PSI5 Initialization Phase 3, the device completes its internal self checks and transmits a combination of Sensor Busy or Sensor Ready messages as defined in Table 9 and Table 10. The number of Sensor Busy messages transmitted in Initialization Phase 3 varies, depending on the mode of operation and the number of self test repetitions.

Once the internal self-test completes, the device transmits two Sensor Ready commands.

Note: self-test repeats are handled independently for each channel. However, both channels exit Initialization Phase 3 simultaneously. If only one channel is repeating self-tests, both channels transmit Sensor Busy commands until either self-test has passed on both channels or the total number of repeats have completed.

Table 9. Dual axis device: Initialization data Phase 3

16-bits data values	10-bit data values	Description
7A00	1E8	Sensor Busy
79C0	1E7	Sensor Ready
7980	1E6	Sensor Ready, but Unlocked

Table 10. Single axis device: Initialization data Phase 3

16-bit data values	10-bit data values	Description
7A00	1E8	Sensor Busy
79FF	1E7	Sensor Ready
7980	1E6	Sensor Ready, but Unlocked

10.4 PSI5 Normal Mode

Once Initialization Phase 3 completes, the device enters into Normal Mode and starts sending sensor or status data according to Table 11 and Table 12.

Table 11. Dual axis device: Normal Mode PSI5 data values

16-bit data values	10-bit data values	Description	
		EMSG_EXT = 1[1]	EMSG_EXT = 0
7D00	1F4	Sensor Defect Error	Sensor Defect Error
7BC0	1EF	Communication Error	Mapped to 0x1F4
7B80	1EE	Test Mode Enabled	
7B40	1ED	Offset Error	
7B00	1EC	Temperature Error	
7AC0	1EB	Memory Error	
7A80	1EA	Sensor Self Test Error	Sensor Self Test Error
7800	1E0	Maximum positive sensor value	Maximum positive sensor value
. . .	. . .	Positive Sensor Value	Positive Sensor Value
0000	0	Zero	Zero
. . .	. . .	Negative Sensor Value	Negative Sensor Value
8800	220	Maximum negative sensor value	Maximum negative sensor value

[1] When set, the EMSG_EXT bit in register PSI5_CFG enables additonnal PSI5 error message information

Table 12. Single axis device: Normal Mode PSI5 data values

16-bit data values	10-bit data values	Description	
		EMSG_EXT = 1[1]	EMSG_EXT = 0
7D00	1F4	Sensor Defect Error	Sensor Defect Error
7BFF	1EF	Communication Error	Mapped to 0x1F4
7B80	1EE	Test Mode Enabled	
7B40	1ED	Offset Error	
7B00	1EC	Temperature Error	
7AFF	1EB	Memory Error	
7A80	1EA	Sensor Self Test Error	Sensor Self Test Error
7800	1E0	Maximum positive sensor value	Maximum positive sensor value
. . .	. . .	Positive Sensor Value	Positive Sensor Value
0000	0	Zero	Zero
. . .	. . .	Negative Sensor Value	Negative Sensor Value
8800	220	Maximum negative sensor value	Maximum negative sensor value

[1] When set, the EMSG_EXT bit in register PSI5_CFG enables additonnal PSI5 error message information

11 PSI5 Normal Mode Configuration Example

Section 11 "PSI5 Normal Mode Configuration Example" covers some of the main PSI5 features supported by PSI5 standard V2.3.

- 10-bit Data
- 16-bit Data
- Message Error Detection
  - 1-bit Parity
  - 3-bit CRC
- Current response
  - Normal
  - Low
- Baud Rate
  - 125 kHz
  - 189 khz
- Time Slot and Command Blocking
- Dual Response Transmission Mode

11.1 PSI5 10-bit data with parity

This section cover the configuration using 10-bit data responses with 1-bit Parity message error detection.

Table 13 and Table 14 show the formatting of the Data Response.

Table 13. PSI5-x10P transmission mode

Start bits		Sensor data										Parity
S2	S1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	P

Bits PDMFORMAT[2:0] in register SOURCEID_0 control the PSI5 response format as shown below.

Table 14. PSI5 data field configuration

PDCMFORMAT[2:0]			Data field size (bits)
0	0	0	10
0	0	1	10
0	1	0	10
0	1	1	10
1	0	0	16
1	0	1	16
1	1	0	16
1	1	1	16

Bit P_CRC in register PSI5_CFG control the message error detection mode.

Table 15. PSI5 data field configuration

P_CRC	Parity or CRC
0	Parity
1	CRC

When parity error detection is selected, even parity is employed. The number of logic 1 bits in the transmitted message must be an even number.

Figure 7 shows a typical 10-bit PSI5 response using 1-bits parity as error detection.

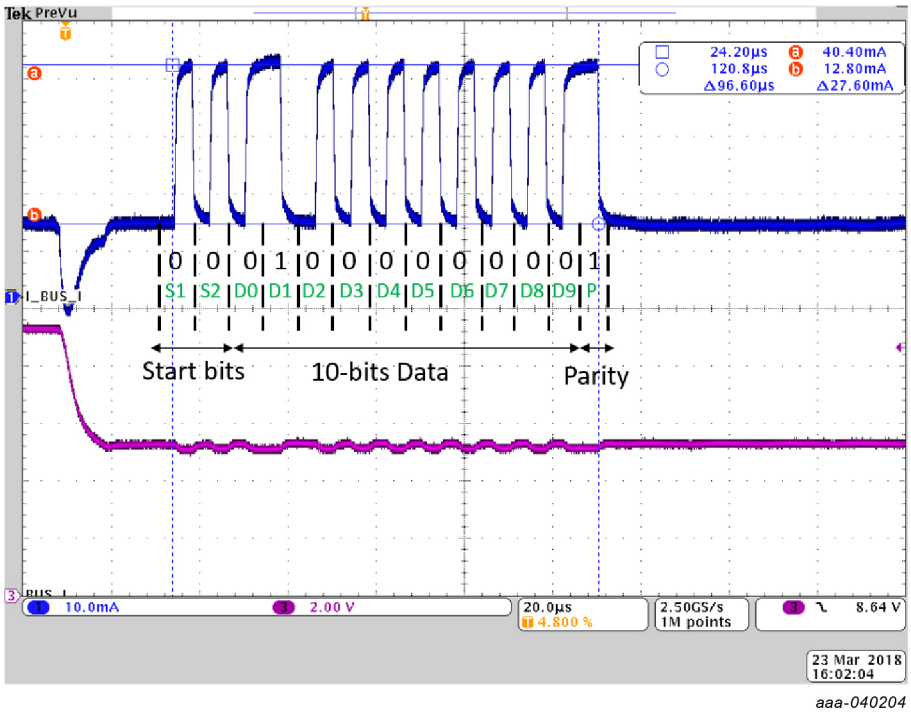

Figure 7. PSI5 10-bit response with parity

11.2 PSI5 16-bit data with CRC

This section cover the configuration using 16-bit data response with 3-bit CRC as message error detection.

Table 16 and Figure 8 show the formatting of the Data Response.

Table 16. PSI5-x16C transmission mode

Start bits		Sensor data																CRC		
S2	S1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	C2	C1	C0

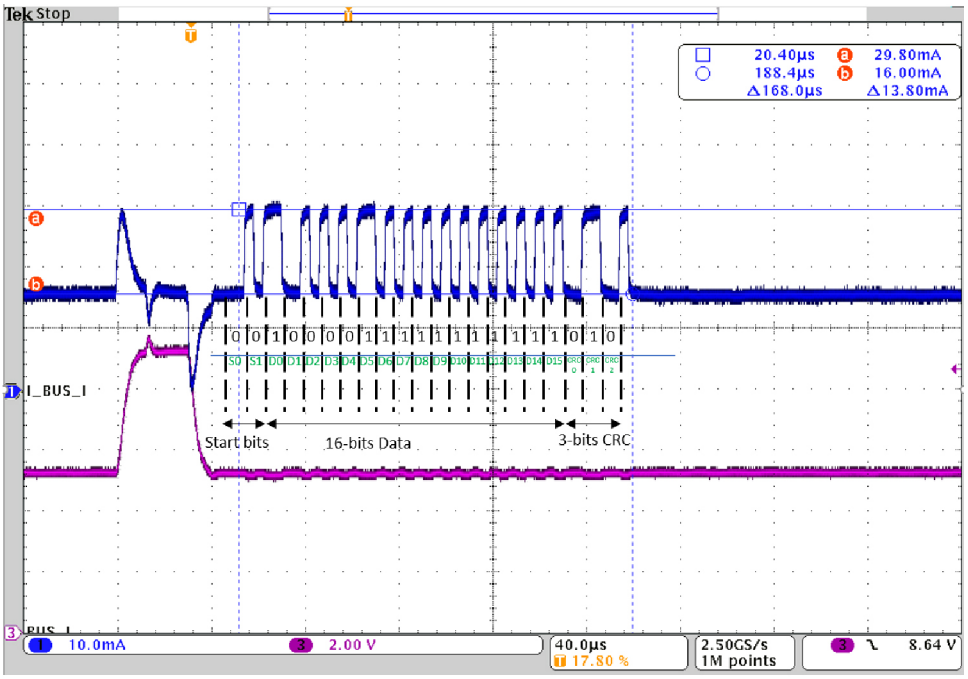

Figure 8. PSI5 16-bit response with CRC

11.3 PSI5 current response

Current response mode is selected by bit PSI5_ILOW in register PSI5_CFG.

When set to 0, Normal current response is selected; when set to 1, Low current mode is selected, as defined by Table 17.

Table 17. PSI5 current response level

Characteristic	Symbol	Min	Typ	Max
Quiescent Supply Current				
• V_{bus_I} = 4 V, Single Channel	$I_{q\_4\_1}$	4.0 mA	-	6.0 mA
• V_{bus_I} = 20 V, Single Channel	$I_{q\_20\_1}$	4.0 mA	-	6.0 mA
• V_{bus_I} = 4 V, Dual Channel	$I_{q\_4\_2}$	4.0 mA	-	10.0 mA
• V_{bus_I} = 20 V, Dual Channel	$I_{q\_20\_2}$	4.0 mA	-	10.0 mA
Response Current				
• Normal Current Response	I_{R_PSI5}	I_q + 22 mA	I_q + 26 mA	I_q + 30 mA
• Low Current Response	$I_{R\_PSI\_LOW}$	I_q + 11 mA	I_q + 13 mA	I_q + 15 mA

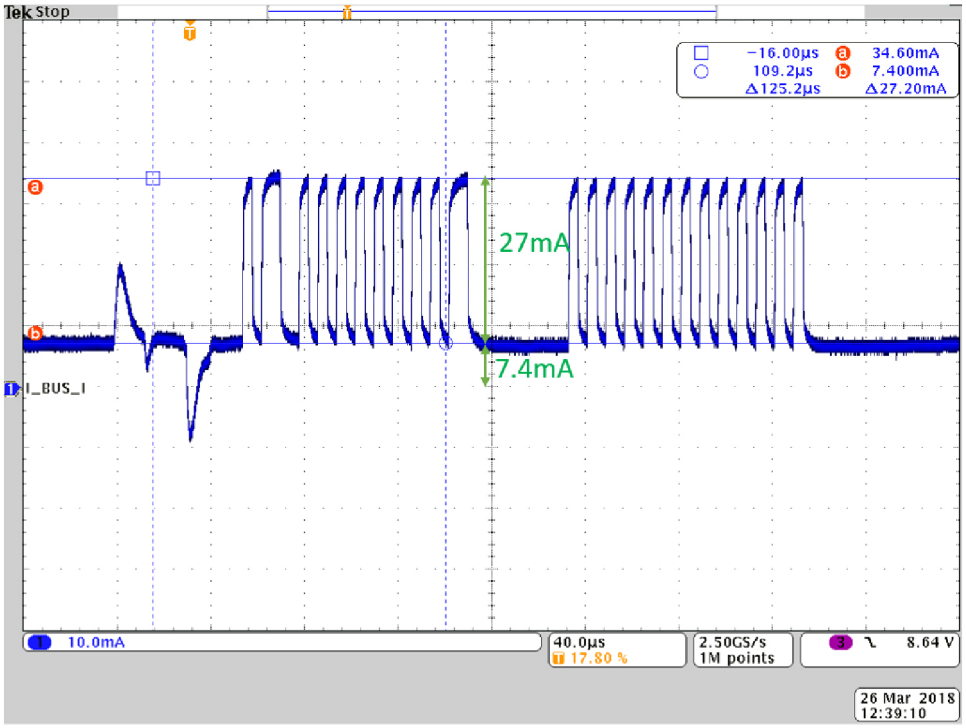

Figure 9. Normal current PSI5 response

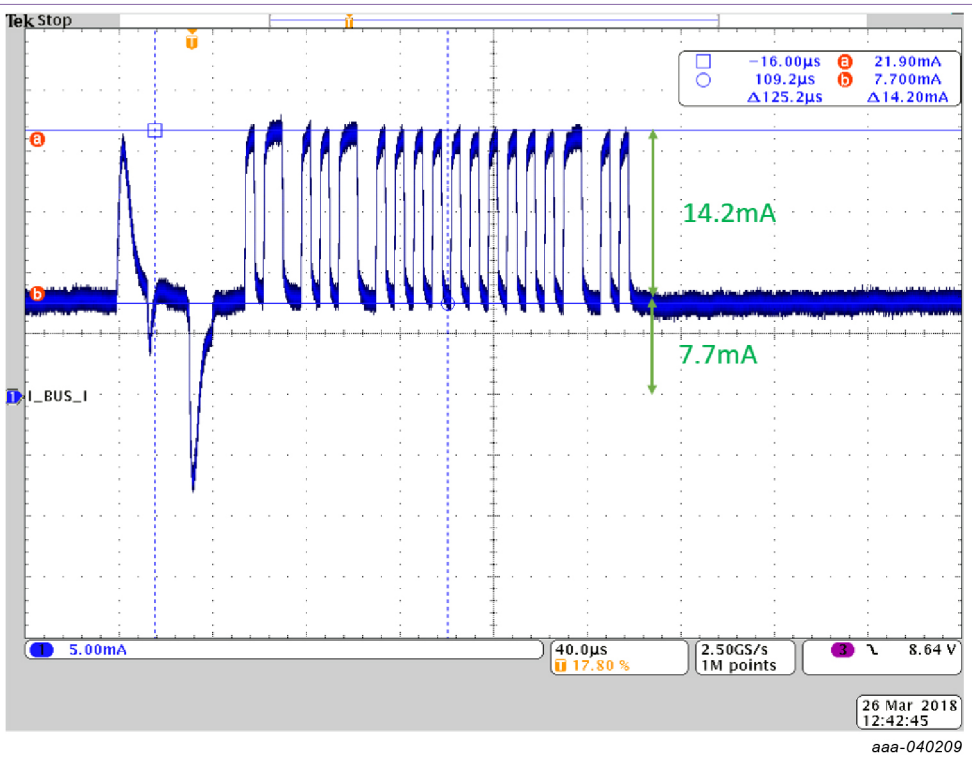

Figure 10. Low current PSI5 response

11.4 PSI5 baud rate

Bits CHIPTIME[3-0] control the bit times for PSI5 response data, thus allowing the response Baud Rate to be selected as defined in Table 18 below.

Table 18. PSI5 baud rate configuration

CHIPTIME[3]	CHIPTIME[2]	CHIPTIME[1]	CHIPTIME[0]	PSI5		
				Period time	Baud rate	Slew control
0	0	0	0	5.3 µs	189 kHz	Enabled
0	0	0	1	5.3 µs	189 kHz	Enabled
0	0	1	0	5.3 µs	189 kHz	Enabled
0	0	1	1	5.3 µs	189 kHz	Enabled
0	1	0	0	5.3 µs	189 kHz	Enabled
0	1	0	1	5.3 µs	189 kHz	Enabled
0	1	1	0	5.3 µs	189 kHz	Enabled
0	1	1	1	5.3 µs	189 kHz	Enabled
1	0	0	0	8.0 µs	125 kHz	Enabled
1	0	0	1	8.0 µs	125 kHz	Enabled
1	0	1	0	8.0 µs	125 kHz	Enabled
1	0	1	1	8.0 µs	125 kHz	Enabled
1	1	0	0	8.0 µs	125 kHz	Enabled
1	1	0	1	8.0 µs	125 kHz	Enabled
1	1	1	0	8.0 µs	125 kHz	Enabled
1	1	1	1	8.0 µs	125 kHz	Enabled

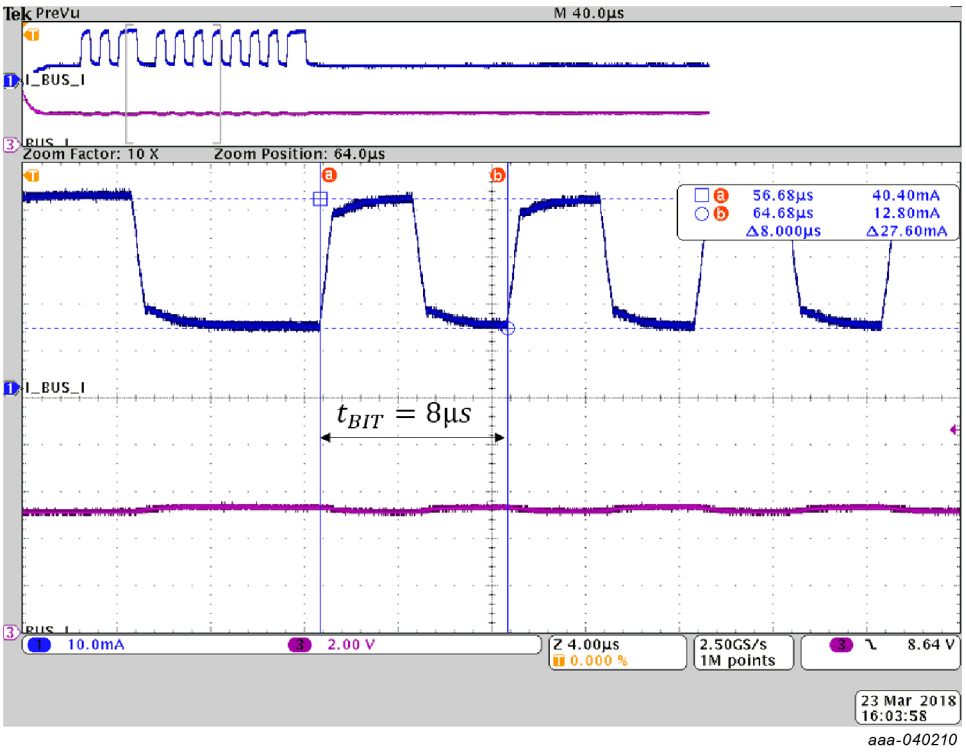

Figure 11. PSI5 response 125 kHz baud rate

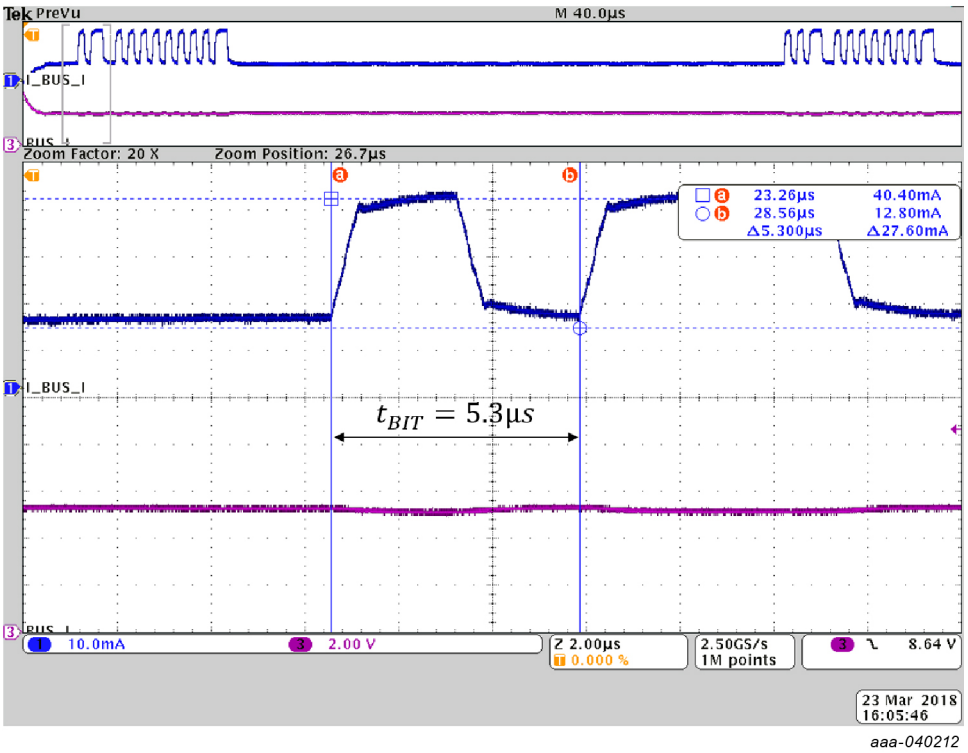

Figure 12. PSI5 response 189 kHz baud rate

The time to transmit a current response is computed using below formula:

$$t_{TRAN} = t_{BIT} * (2 + DATASIZE + 1)$$

if Parity is used

$$t_{TRAN} = t_{BIT} * (2 + DATASIZE + 3)$$

if CRC is used

With

t_{BIT} = *Bit Period Time = 8 µs* for 125 kHZ or *5.3 µs* for 189 kHZ for 125 kHz or for 189 kHz.

Table 19 shows transmission time examples.

Table 19. PSI5 current response transmission time summary

Baud rate	Data size	Error detection	t_{TRAN}(µs)
125 kHz	10-bits	Parity	104
		CRC	120
	16-bits	Parity	152
		CRC	168
189 kHz	10-bits	Parity	68.9
		CRC	79.5
	16-bits	Parity	100.7
		CRC	111.3

11.5 Time slot and command blocking configuration

PSI5 Synchronous systems support a Time-division multiple access capability that allows the connection of up to three sensors (at 125 kbit/s) or four sensors (at 189 kbits/s).

Bit ASYNC in register PSI5_CFG controls configuration of the operating mode. If set to 0 by default, the selected operating mode is synchronous. If set to 1, asynchronous mode is selected.

In synchronous mode, PSI5 response time is set by using registers PDCM_RSPSTx. The value is stored in 1 µs increments with 0 as the default value of 20 µs.

Table 20. PDCM Response start time configuration

PDCM_RSPSTx[12:0]	PDCM response start time
0>PDCM_RSPSTx[12:0]>20	20.0 µs
20> PDCM_RSPSTx[12:0]	Response Start Time = PDCM_RSPSTx[12:0] * 1 µs

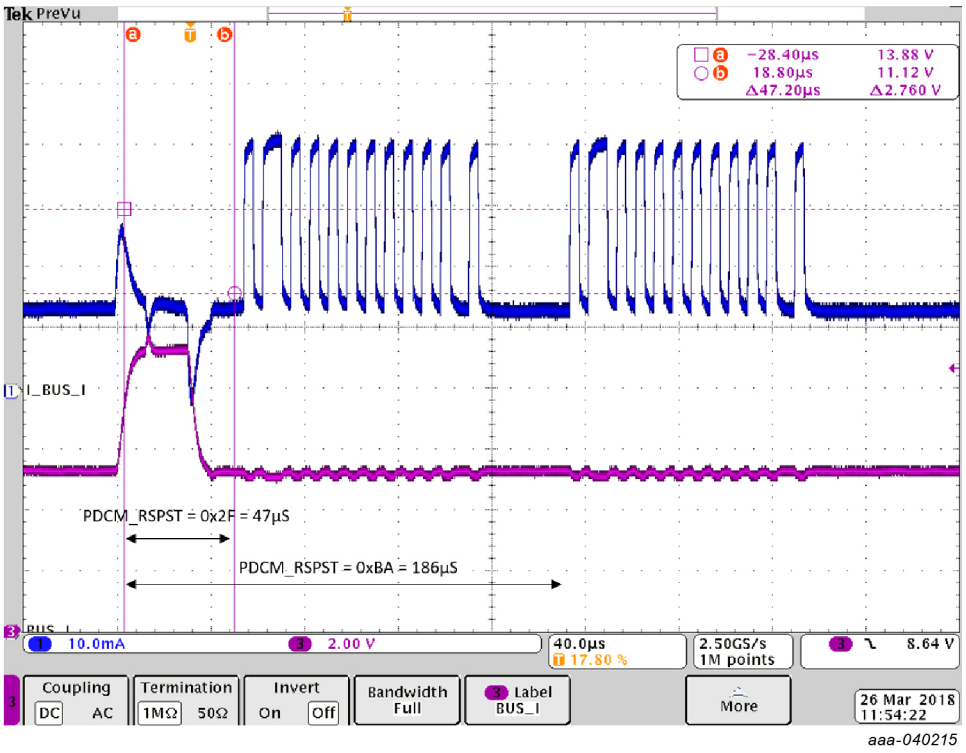

Figure 13. PSI5 PDCM start time response

In asynchronous mode, PSI5 response start time is fixed at 228 µs.

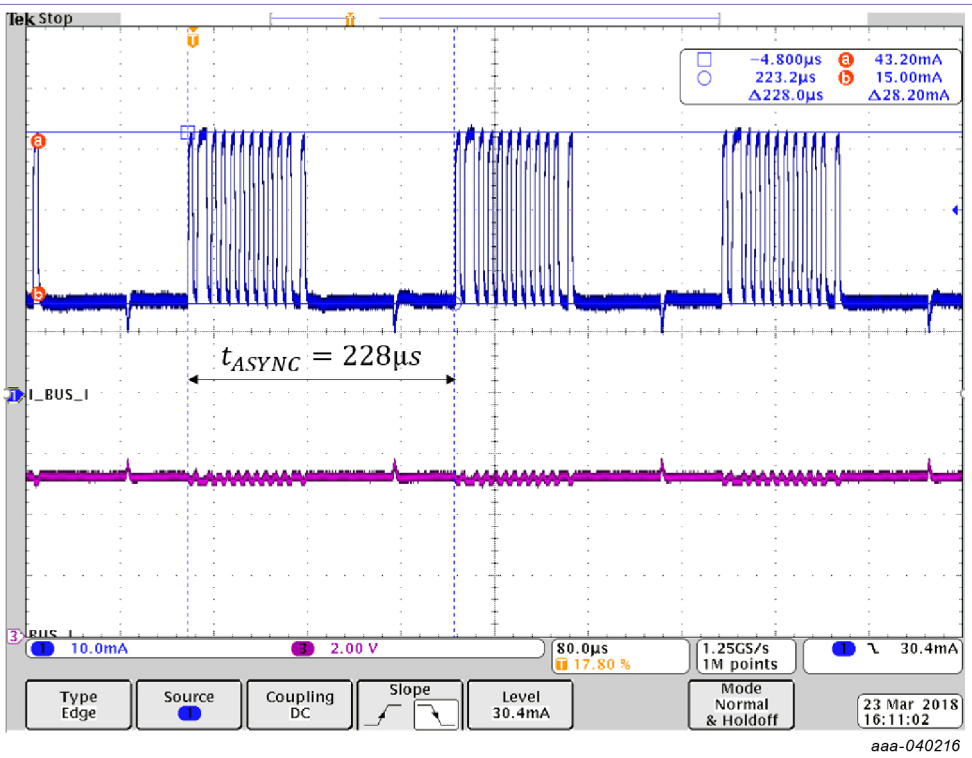

Figure 14. PSI5 response time using asynchronous mode

Along with the response start time configuration, command blocking time is set by register PDCM_CMD_B[12:0]. The value is stored in 1 µs increments with zero as the default value of 450 µs. When programming command blocking, users should take care that the programming does not prevent proper pulse decoding synchronization. Figure 15 illustrates a correct synchronization pulse detection; Figure 16 illustrates an incorrect synchronization pulse detection due to the command blocking not being properly set according to the pulse rate.

Table 21. PDCM blocking time configuration

PDCM_CMD_B[12:0]	Sync pulse blocking time
PDCM_CMD_B[12:0]<=9	450.0 µs
PDCM_CMD_B[12:0]>9	Response Start Time = PDCM_CMD_B[12:0]* 1 µs

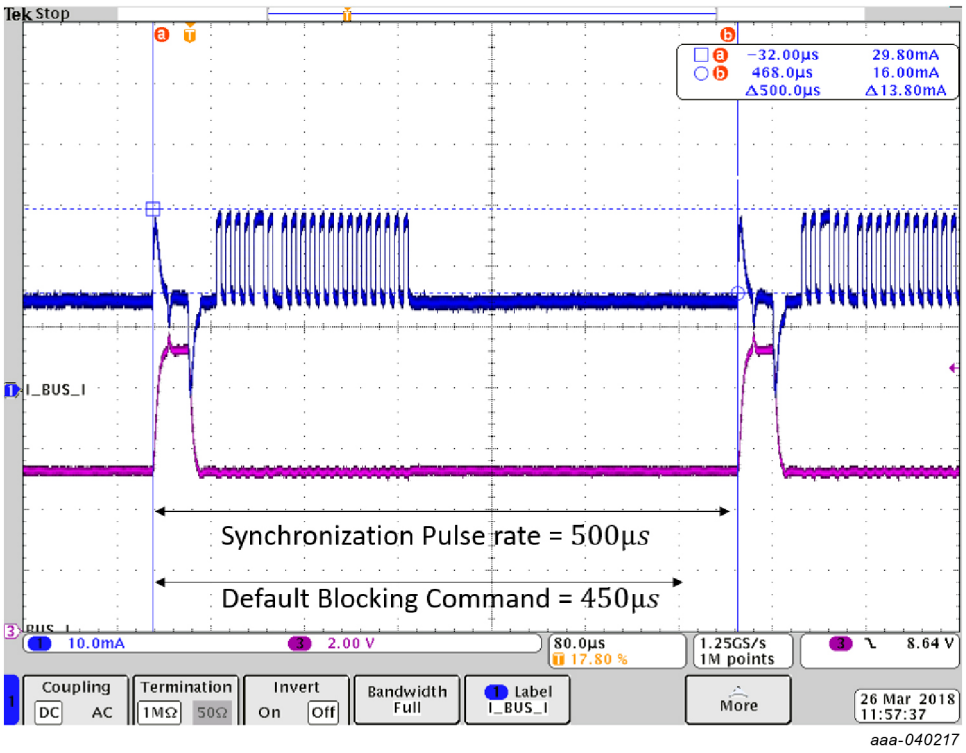

Figure 15. Default 450 µs blocking command with 500 µs sync pulse rate

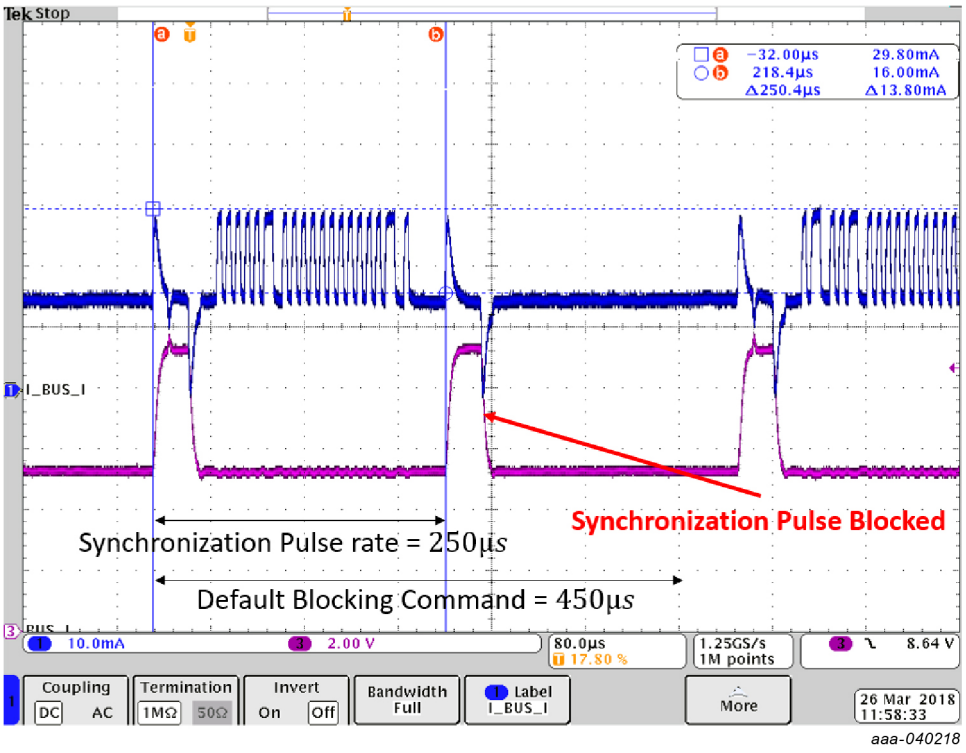

Figure 16. Default 450 µs blocking command with 250 µs sync pulse rate

11.6 Dual Response mode

PSI5 synchronous mode allows dual transmission mode to be enabled by using the DUALTRANS bit in register PSI5_CFG. This mode allows contatenated CH0 and CH1 data to be transmitted using one time slot. Table 15 summarize Dual transmission mode configuration.

Table 22 illustrate an example of Dual Response mode with only SID-EN0 enabled.

Table 22. Dual transmission mode configuration

DUAL TRANS	SID_EN				Operating Mode	Response PDCM_ RSPST0	Response PDCM_ RSPST1	Response PDCM_ RSPST2	Response PDCM_ RSPST3
	SID-EN3	SID-EN2	SID-EN1	SID-EN0					
1	x	x	0	0	No Transmision	None	None	None	None
	x	x	0	1	Dual Data Transmission Mode, Single transmission T	Concatenate (CH1_ SNSDATA0, CH0_ SNSDATA0)	None	None	None
	x	x	1	0	Dual Data Transmission Mode, Single Transmission	None	Concatenate (CH1_ SNSDATA0, CH0_ SNSDATA0)	None	None
	x	x	1	1	Dual Data Transmission Mode, Double Transmission	Concatenate (CH1_ SNSDATA0, CH0_ SNSDATA0)	Concatenate (CH1_ SNSDATA1, CH0_ SNSDATA)	None	None

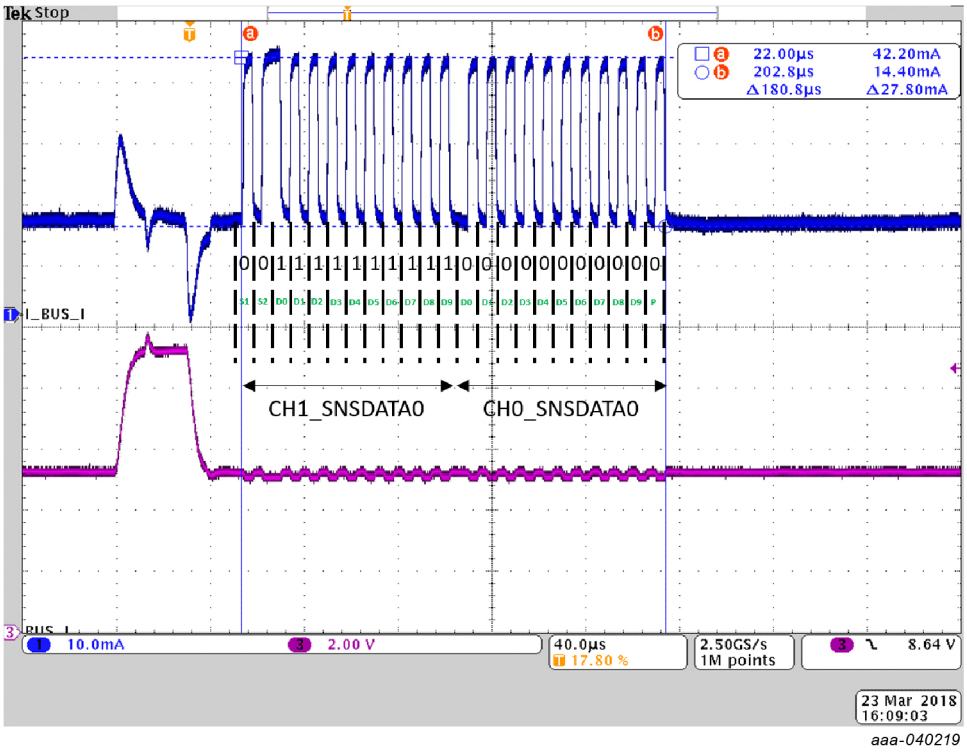

Figure 17. PSI5 dual transmission mode response

11.7 Data Type configuration

Data Type is configured using DATATYPE0[1:0] and DATATYPE[2:0] repectively for SOURCEID_0/ SOURCEID_1 and SOURCEID_1/ SOURCEID_3. Table 23 and Table 24 summarize the different Data Type configurations.

Table 23. Data Type 0 configuration

CHxDATA TYPE0[1]	CHxDATA TYPE0[0]	Data transmitted			
		Data transmitted	Offset cancelled?	Moving average ?	Interpolation?
0	0	Chx Sensor Data	Selected by OC_FILT	Selected by MOVEAVG	Selected by MOVEAVG
0	1	Chx Sensor Data	No	Selected by MOVEAVG	Selected by MOVEAVG
1	0	Temperature			
1	1				

Table 24. Data Type 1 configuration

CHxDATA TYPE1[2]	CHxDATA TYPE1[1]	CHxDATA TYPE1[0]	Data transmitted			
			Data transmitted	Offset cancelled?	Moving average ?	Interpolation?
0	0	0	Chx Sensor Data	Selected by OC_FILT	Selected by MOVEAVG	No
0	0	1	Chx Sensor Data	No	Selected by MOVEAVG	No
0	1	0	Temperature			
0	1	1				
1	0	0	Chx Sensor Data	Selected by OC_FILT	No	No
1	0	1	Chx Sensor Data	No	Selected by MOVEAVG	No
1	1	0	Temperature			
1	1	1				

11.7.1 PSI5 temperature data

Figure 23 shows an example of PSI5 10-bit temperature data derived by setting CH0DATATYPE[1:0] = 0b11.

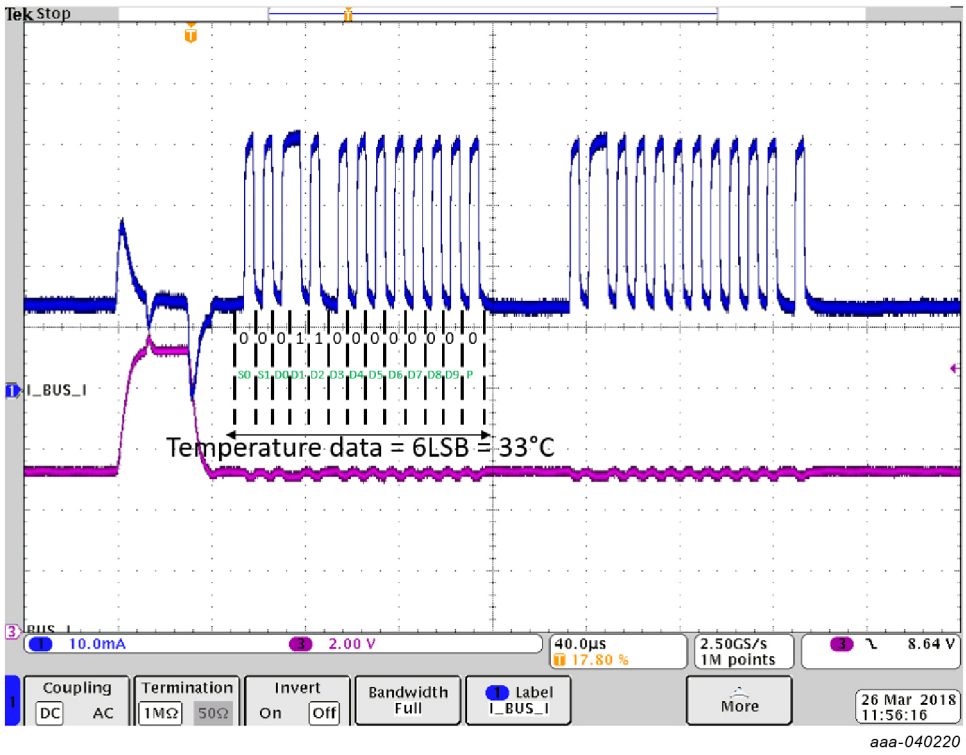

Figure 18. PSI5 10-bit temperature data

The equation below converts an LSB temperature reading into °C temperature.

$$T_{DEGC} = \frac{T_{LSB} - T0_{LSB}}{T_{Sense}}$$

T_{DEGC} = Temperature output in °C

T_{LSB} = Temperature output in LSB

$T0_{LSB}$ = Temperature output in LSB at 0°C

T_{SENSE} = Expected Temperature sensitivity in LSB/°C

Table 25. PSI5 temperature data reading

Data reading	$T0_{LSB}$	T_{SENSE}
16-bit PSI5 Sensor Data	-1728	70.4
10-bit PSI5 sensor Data	-27	1.1

12 Daisy Chain Mode

The device can be programmed to operate in Daisy Chain Mode by setting the DAISY_CHAIN bit in the PSI5_CFG register using the PSI5 Programming procedure described in AN12162.

Figure 19 describes the daisy chain initialization procedure for an application programmed to operate in Daisy Chain Mode with two sensors connected.

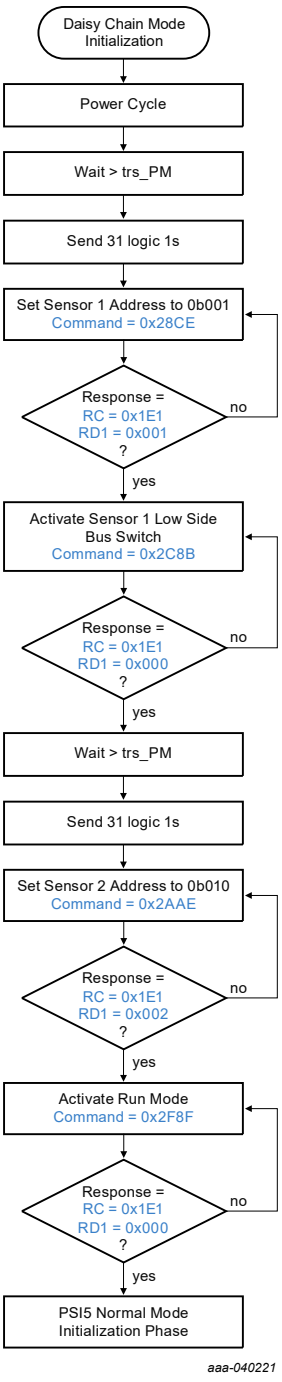

Figure 19. Daisy chain initialization procedure

13 Summary and Conclusion

This application note describes the PSI5 normal mode initialization and main features for FXLS93xx devices.

14 Appendix

14.1 PSI5 State Transition Diagram

Figure 20 shows a state transition diagram for the internal PSI5 controller.

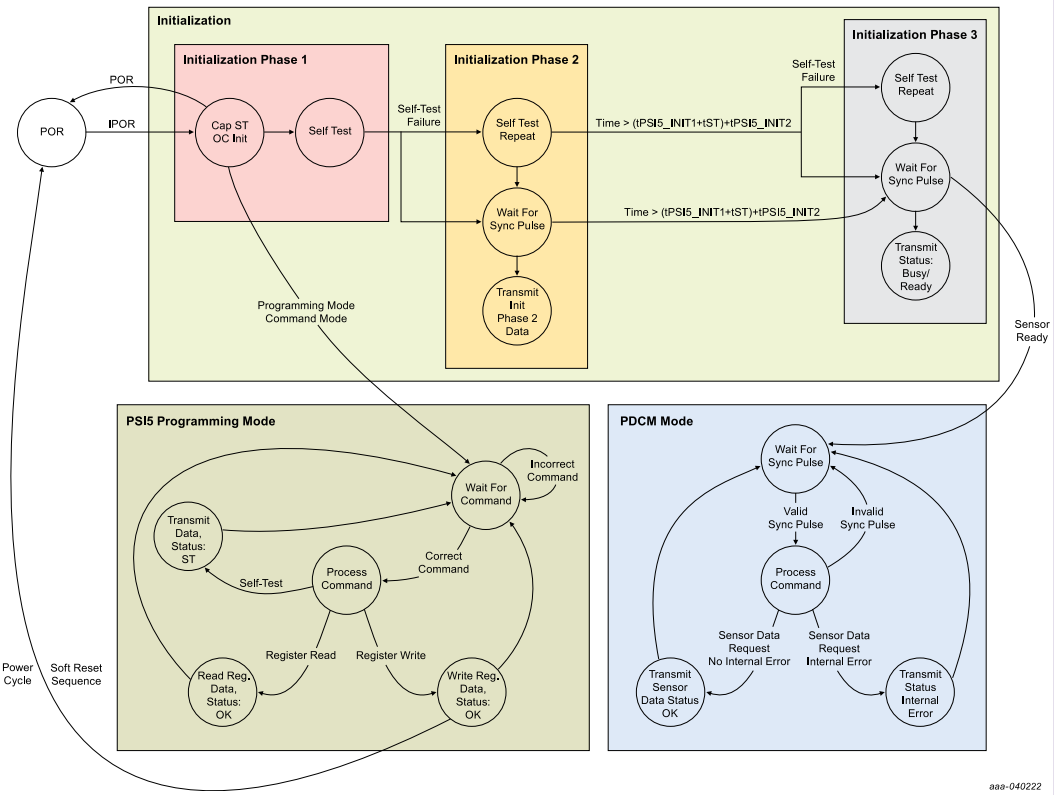

Figure 20. PSI5 state transition diagram

14.2 CRC Calculation Examples

14.2.1 3-bit CRC

Figure 26 shows a Visual Basic code example that calculates the PSI5 3-bit CRC.

- Function SPICRC3(Data32 As String, Poly As String, SEED As String) As String
  - Data32 is the 29-bit message in binary to be verified with 3 zeroes appended in place of the CRC

Example: Command = 0x8040270x: Data32 = 1000 0000 0100 0000 0010 0111 0000 0000

- Poly is the 9-bit CRC polynomial in binary

Example: Polynomial = X^3+X+1 Poly = 1011

- SEED is the 8-bit CRC Initial value in binary

Example: Seed = 0x7 SEED = 111

In this example, the CRC = 0x5

```
Function SPICRC3(Data32 As String, Poly As String, SEED As String) As String
Dim i As Integer
Dim m As Integer
Dim n As Integer
Dim k As Integer
Dim bit As Integer
i = 1
m = 1
n = 1
k = 1
bit = 0
Dim CRC(1 To 3) As String
Dim CRC_old(1 To 3) As String
For i = 1 To 3
    CRC(i) = Mid(SEED, i, 1)
    CRC_old(i) = Mid(SEED, i, 1)
Next i

For n = 1 To 32
    bit = Mid(Data32, n, 1)
    For k = 1 To 3
        CRC_old(k) = CRC(k)
    Next k
    For m = 1 To 3
      If Mid(Poly, m + 1, 1) = 0 Then
        If m = 3 Then
          CRC(m) = bit
        Else
          CRC(m) = CRC_old(m + 1)
        End If
      Else
        If m = 3 Then
          If CRC_old(1) = 1 Then
            If bit = 1 Then
              CRC(m) = 0
            Else
              CRC(m) = 1
            End If
          Else
            If bit = 1 Then
              CRC(m) = 1
            Else
              CRC(m) = 0
            End If
          End If
        Else
          If CRC_old(1) = 1 Then
            If CRC_old(m + 1) = 1 Then
              CRC(m) = 0
            Else
              CRC(m) = 1
            End If
          Else
            If CRC_old(m + 1) = 1 Then
              CRC(m) = 1
            Else
              CRC(m) = 0
            End If
          End If

        End If
      End If
    Next m
Next n
SPICRC3 = CRC(1) & CRC(2) & CRC(3)
End Function
```

aaa-040223

Figure 21. PSI5, 3-bit CRC Visual Basic

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