

# AN10170

## Design guidelines for COG modules with NXP monochrome LCD drivers

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Application note

### Document information

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<b>Abstract</b>	This application note explains how to design the optimal ITO layout on the input side of the LCD driver IC. These design guidelines apply to all NXP monochrome LCD driver ICs unless otherwise stated. The guidelines help toward successful first-time module design and better overall display performance.



**Revision history**

Rev	Date	Description
v.4	20140804	revised version
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v.2	20030205	revised version
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## 1. Introduction

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In COG applications, the designer must not neglect the resistance of ITO tracks. Special attention must be paid to the ITO layout in order to keep the effects of track resistance to an acceptable level. This Application Note explains how to design the optimal ITO layout on the input side of the driver IC for various power supply lines.

### 1.1 Who should read this application note?

It is important that engineers in charge of the LCD module design and ITO layout design on the interface side read this application note. Both module maker and OEM (set-maker) will find this application note useful.

## 2. Guidelines for power supply lines $V_{SS}$ , $V_{DD}$ and $V_{LCD}$

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For COG applications, the power supply circuits of NXP LCD driver ICs are separated internally into  $V_{DD1}$ ,  $V_{DD2}$ ,  $V_{DD3}$ ,  $V_{SS1}$ ,  $V_{SS2}$  and sometimes  $V_{SS3}$  supply rails. This allows the module maker to connect these supply circuits using separate ITO tracks. In this way, the common (shared) part of the ITO track is minimized or eliminated. This reduces the amount of common-mode electrical noise.

For similar reasons, the LC drive supply circuits are separated internally into  $V_{LCDIN}$ ,  $V_{LCDOUT}$  and  $V_{LCDSENSE}$ . The shared part of the ITO supply track thus is kept to a minimum.

[Figure 1](#) and [Figure 2](#) represent the ITO and glass-to-PCB connection paths in two typical configurations. Suggested maximum resistance values of the power supply for a typical small display application (pixel size is in the order of 0.15 mm x 0.15 mm to 0.5 mm x 0.5 mm) are given in [Table 1](#). These limits depend on the display load and have to be revised for each particular application.

Excessive track resistance, especially common (shared) track and connection resistance results in:

- a deterioration of the display quality
- increased power consumption
- incorrect operation.

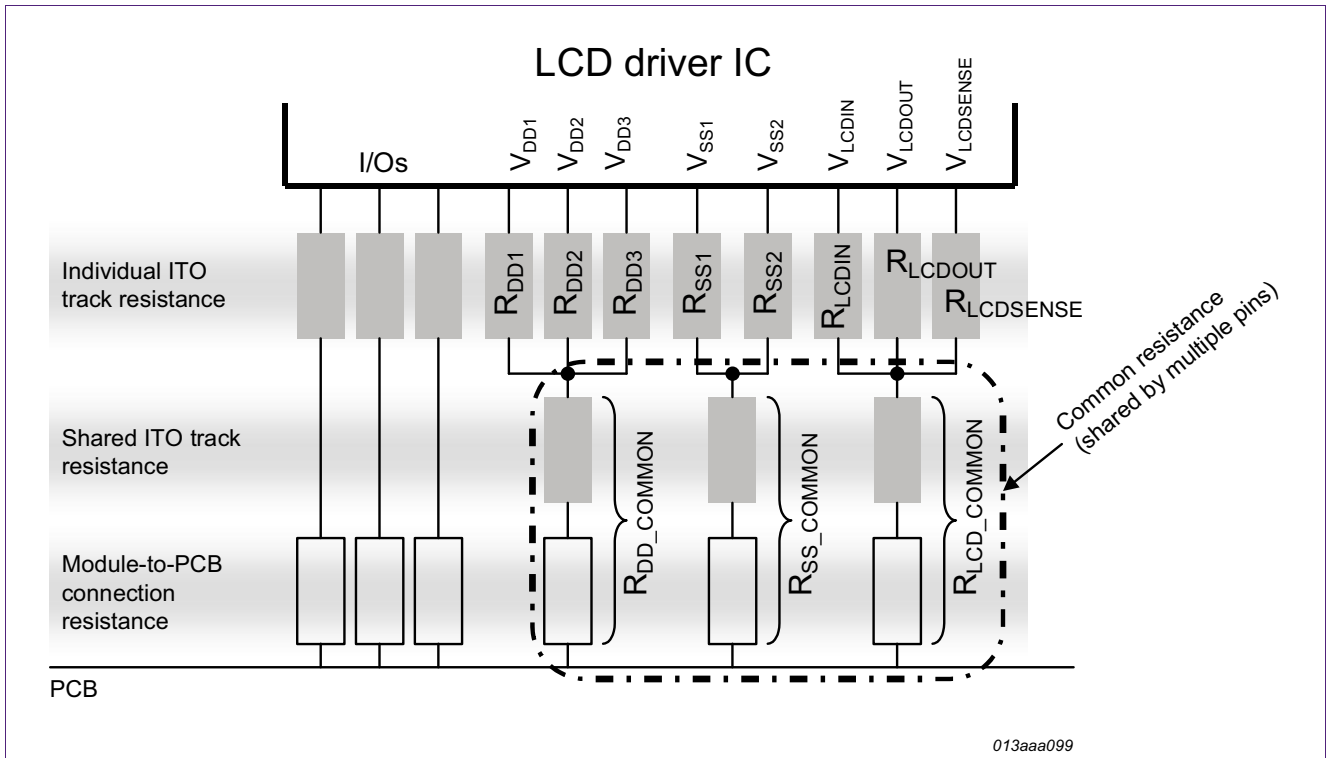


Fig 1.  $V_{DD1} = V_{DD2} = V_{DD3}$

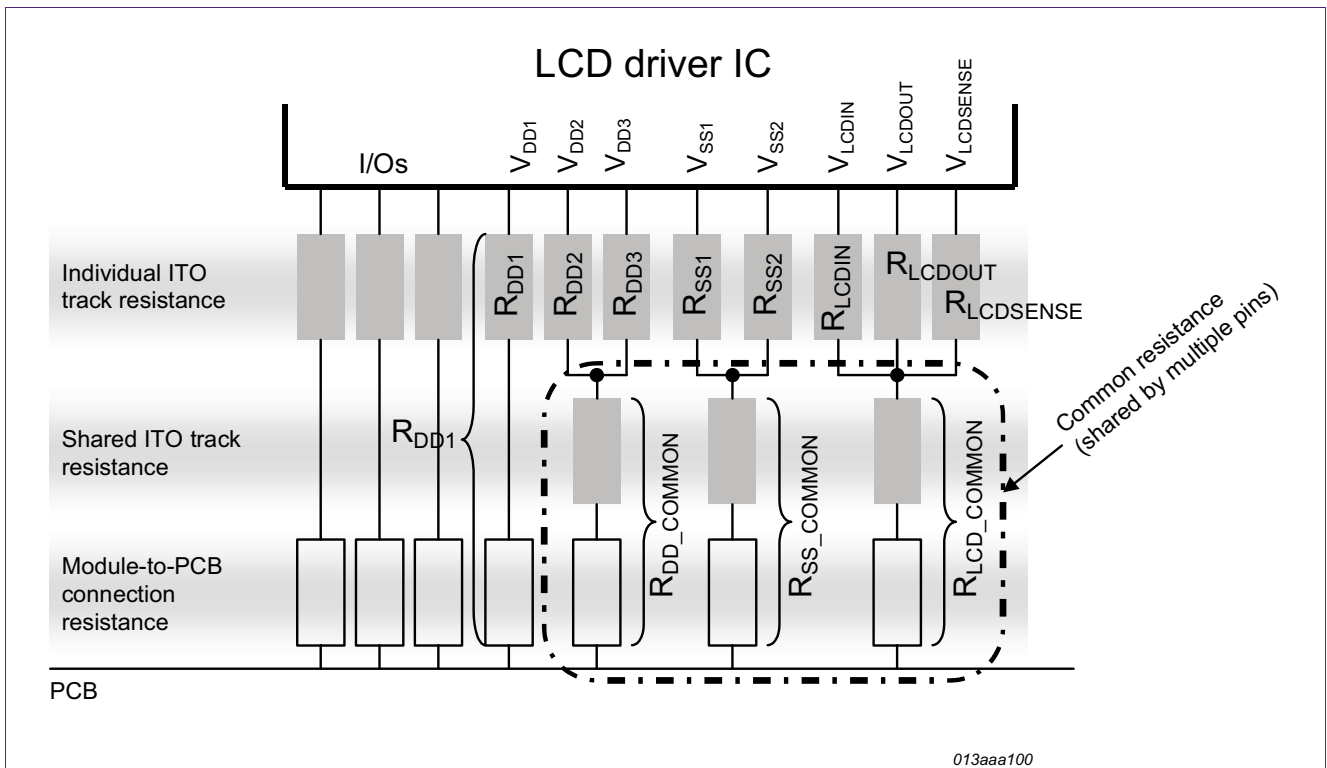


Fig 2.  $V_{DD1} \neq V_{DD2} = V_{DD3}$

Table 1. Maximum ITO track resistance for display drivers

Resistance path	Description	Maximum resistance ( $\Omega$ )
<b>With integrated charge pump</b>		
R <sub>DD_COMMON</sub>	common V <sub>DD</sub> track (including connector) <sup>[1]</sup>	40
R <sub>DD1</sub>	positive logic supply	500
R <sub>DD2</sub>	positive charge pump supply	200
R <sub>DD3</sub>	positive analog supply	2000
R <sub>SS_COMMON</sub>	common V <sub>SS</sub> track (including connector) <sup>[1]</sup>	40
R <sub>SS1</sub>	negative supply (excluding charge pump)	80
R <sub>SS2</sub>	negative charge pump supply	200
R <sub>LCD_COMMON</sub>	common V <sub>LCD</sub> track (including connector) <sup>[1]</sup>	60
R <sub>LCDOUT</sub>	generated output V <sub>LCD</sub>	100
R <sub>LCDIN</sub>	V <sub>LCD</sub> input to chip	500
R <sub>LCDSENSE</sub>	V <sub>LCD</sub> sense input	2000
<b>Without integrated charge pump</b>		
R <sub>LCD_COMMON</sub>	common V <sub>LCD</sub> track (including connector) <sup>[1]</sup>	500
R <sub>SS_COMMON</sub>	common V <sub>SS</sub> track (including connector) <sup>[1]</sup>	150
R <sub>OSC</sub>	oscillator select <sup>[2]</sup>	1 000
R <sub>DD_COMMON</sub>	common V <sub>DD</sub> track (including connector) <sup>[1][2]</sup>	500
R <sub>CLK</sub>	clock input and output <sup>[2]</sup>	1 000
R <sub>SCL</sub>	I <sup>2</sup> C-bus serial clock input <sup>[2]</sup>	2 000
R <sub>SDA</sub>	I <sup>2</sup> C-bus serial data input <sup>[2][3]</sup>	2 000
A <sub>n</sub>	subaddress inputs <sup>[2]</sup>	1 000
S <sub>An</sub>	I <sup>2</sup> C-bus slave address input <sup>[2]</sup>	1 000

[1] Common-mode resistance in supply circuits is the most critical element for optical display performance. It is most effectively minimized by connecting the separate ITO tracks outside of the LCD glass (on PCB, FPC, foil etc.) instead of at the connection point on the glass ledge. However this may not always be practical in the application.

[2] The ITO track recommendations are valid for both drivers with and without charge pump.

[3] The values of R<sub>SDA</sub> depend on the external pull-up resistors, see [Section 4](#).

Table 2. SYNC (cascade synchronization input and output) contact resistance

Number of devices	Maximum resistance ( $\Omega$ )
2	6000
3 to 5	2200
6 to 10	1200
11 to 16	700

**Remark:** In order to keep the ITO track resistance to a minimum, the pitch and position of the module connection to the outside must be selected such that the power tracks run as straight as possible to the glass edge. In order to minimize common connection resistance use low-ohmic elastomeric connection, metal pin connection or ACF bonded flat cable.

Figure 3 shows an example of how the ITO layout for the power supply tracks looks in practice.

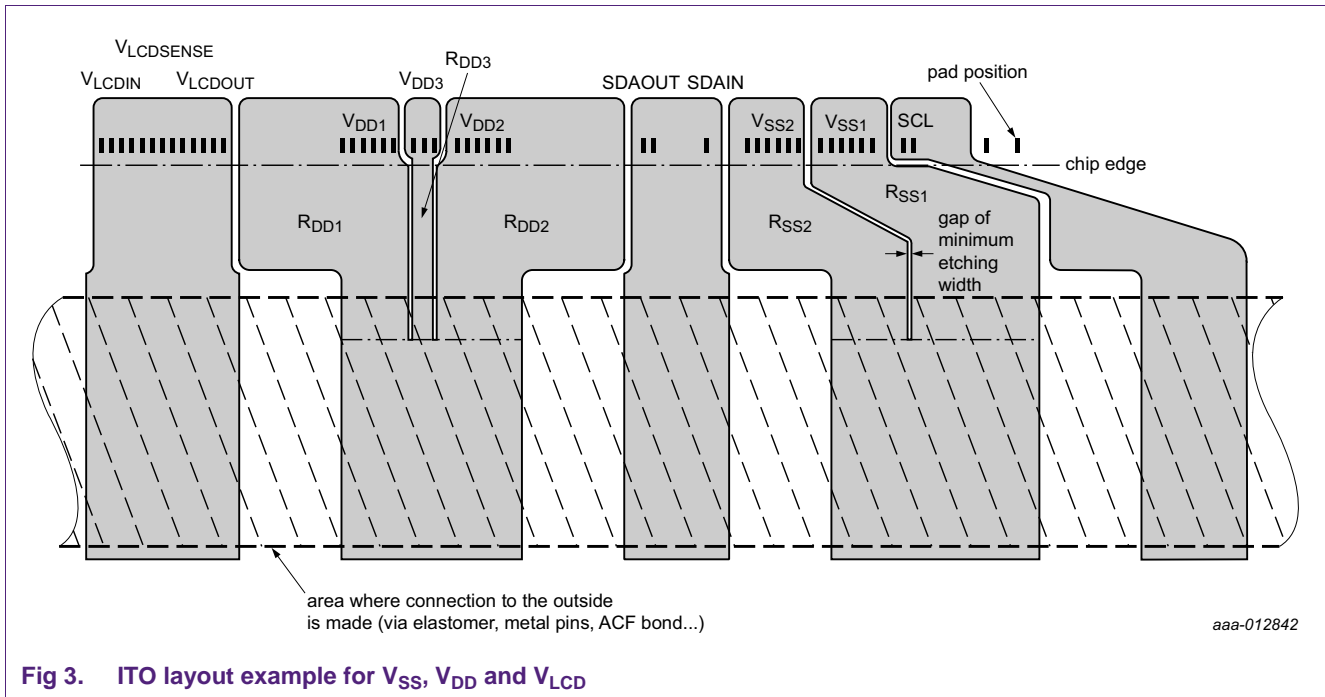


Fig 3. ITO layout example for V<sub>SS</sub>, V<sub>DD</sub> and V<sub>LCD</sub>

### 2.1 Exception to the general rule

The PCF8811 LCD driver uses a slightly different power architecture where the V<sub>LCD</sub> voltage generation is concerned. Because of this, the ITO layout guidelines for connecting pins V<sub>LCDIN</sub>, V<sub>LCDOUT</sub>, V<sub>LCDSENSE</sub> are also different (see Table 3).

Table 3. Exception

Resistance path	Description	Maximum resistance (Ω)
R <sub>LCD_COMMON</sub>	common V <sub>LCD</sub> track (including connector)	60
R <sub>LCDOUT</sub>	generated output V <sub>LCD</sub>	0 <sup>[1]</sup>
R <sub>LCDIN</sub>	V <sub>LCD</sub> input to chip	0 <sup>[1]</sup>
R <sub>LCDSENSE</sub>	V <sub>LCD</sub> sense input	0 <sup>[1]</sup>

[1] This means in practice, that V<sub>LCDIN</sub>, V<sub>LCDOUT</sub> and V<sub>LCDSENSE</sub> must be connected together with one thick ITO track.

### 3. Guidelines for I/O lines

ITO track impedance also affects the AC characteristics of the I/O lines. The ITO track resistance together with any parasitic capacitances adds RC-type delay constants which must be taken into account. NXP recommends that COG modules are not operated close to the limits of the interface timing requirements. Particular attention must be paid to open-drain outputs (see [Section 4](#)).

### 4. Guidelines for I<sup>2</sup>C-bus pins SDA and SCL

The SDA line in I<sup>2</sup>C devices is an open-drain output and therefore needs an external pull-up resistor. The ITO track resistance,  $R_{ITO}$ , together with the pull-up resistor,  $R_{PULL-UP}$ , forms a potential divider. Because of this, there is danger that the other device(s) on the I<sup>2</sup>C-bus will not see a valid logic LOW when the LCD driver IC drives the SDA line LOW e.g. during the ACKnowledge cycle or during read-back from the IC (see [Figure 4](#)).

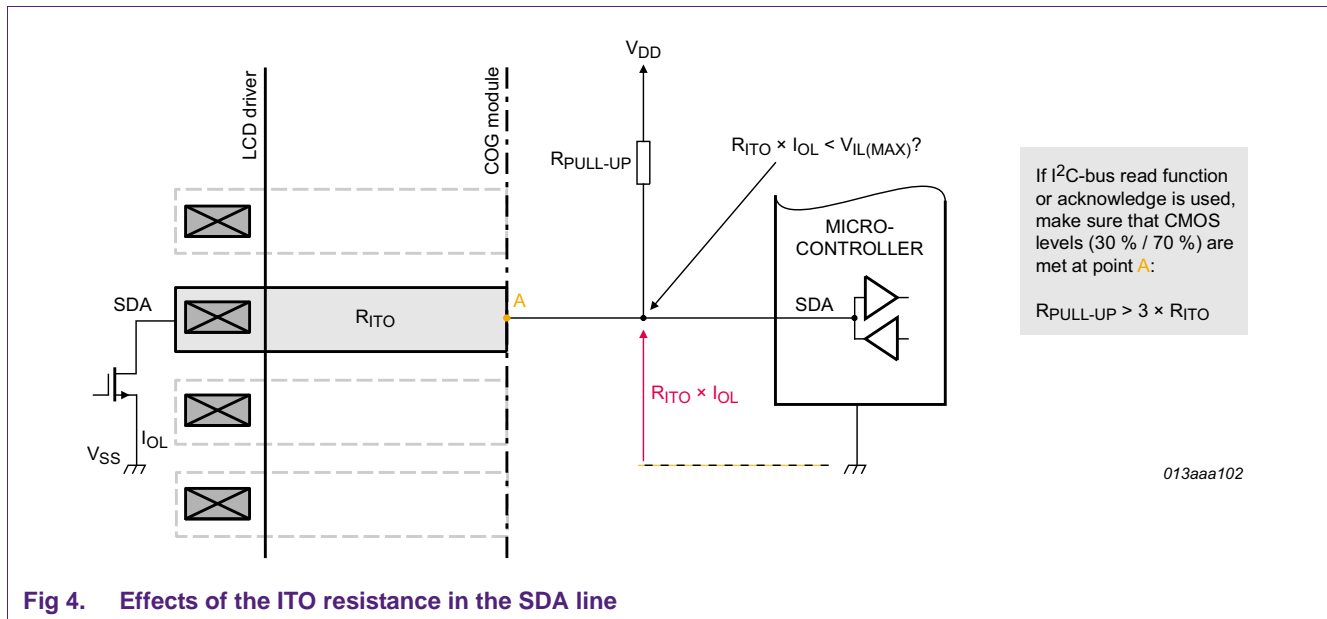


Fig 4. Effects of the ITO resistance in the SDA line

For this reason, the SDA signal in LCD driver ICs is sometimes split into SDAIN and SDAOUT or SDA and SDAACK. A number of possibilities for connecting an LCD driver to the host microcontroller exist, three examples are given.

- The I<sup>2</sup>C protocol is fully implemented in the system, i.e. the master-transmitter device (host microcontroller) expects an ACKnowledge after each byte. In this case connect LCD driver's SDAIN and SDAOUT pins on the glass with a single ITO trace, taking care to minimize track and connection resistance. Choose a pull-up resistor value that will ensure that the  $V_{IL}$  spec of the other device(s) on the I<sup>2</sup>C-bus is always met, under all conditions and including all tolerances.

Note that the value of  $R_{PULL-UP}$  directly affects the SDA signal rise time. If  $R_{PULL-UP}$  is too high, the maximum rise time limit is violated.

Design guidelines for COG modules with NXP monochrome drivers

A simple rule in this case is to make sure that  $(2 \times C_{SDA} \times R_{PULL-UP}) < t_{R(max)}$ , where  $C_{SDA}$  is the capacitance of the SDA bus rail, including the associated parasitic pad capacitances of all the devices connected to the I<sup>2</sup>C-bus and  $t_{R(max)}$  is the specified maximum rise time (see [Figure 5](#)).

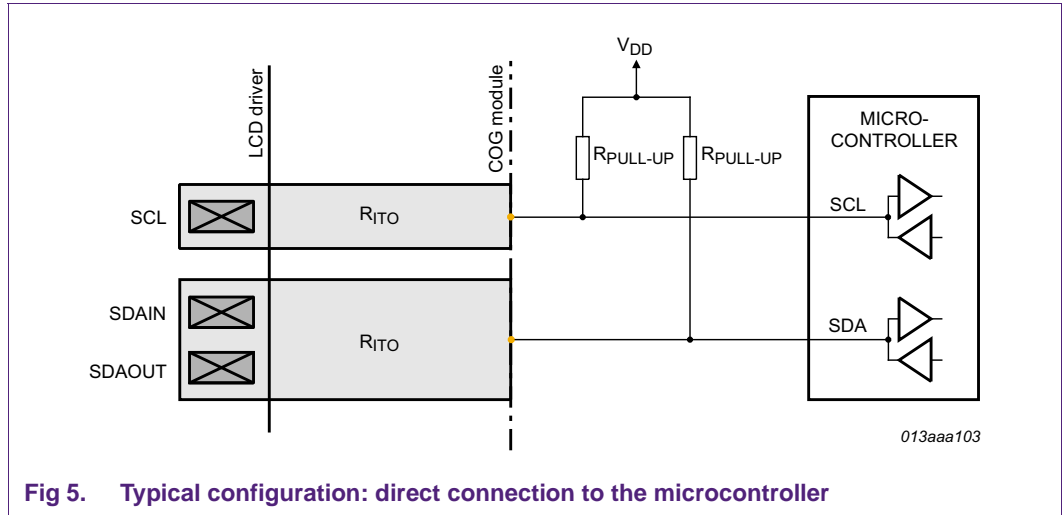


Fig 5. Typical configuration: direct connection to the microcontroller

- The I<sup>2</sup>C protocol is fully implemented in the system but the value of the pull-up resistor required to satisfy the maximum logic low-level requirement  $V_{IL(max)}$  is too high to satisfy simultaneously the maximum rise time requirement,  $t_R$ . In this case, the full SDA signal may be reconstituted using an external open-drain buffer (see [Figure 6](#)). The buffer isolates the SDAOUT pin from the capacitance of the I<sup>2</sup>C-bus and makes the rise time requirement easier to meet.

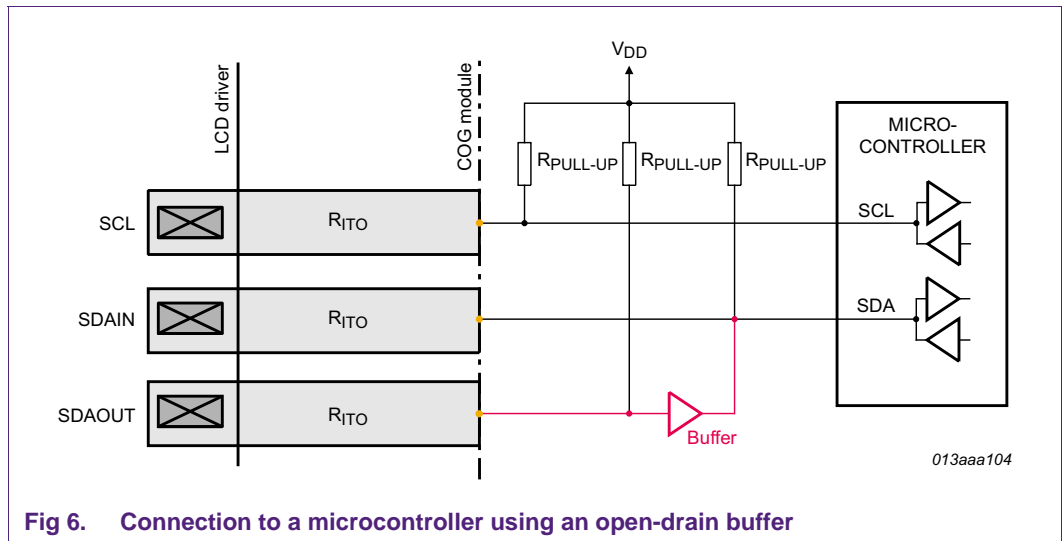
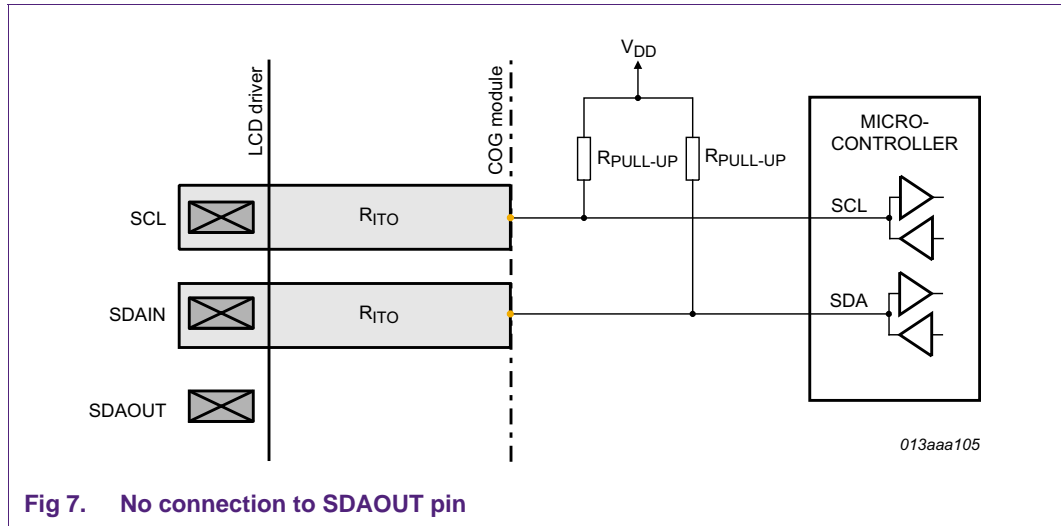


Fig 6. Connection to a microcontroller using an open-drain buffer

- It is possible to implement the I<sup>2</sup>C protocol partially, in a way that ignores the ACKnowledge bit after each byte.



In this case, the SDAOUT can be left unconnected (see [Figure 7](#)). Such a configuration may be desirable because it eliminates the common-mode noise that results from the ACKnowledge current flowing through the common resistance in the  $V_{SS}$  supply of the driver IC. Note, however, that in this case it is not possible to use any read-back function which may be implemented in the LCD driver IC.



## 5. Guidelines for ESD/EMC protection

### 5.1 Dummy pads

Dummy pads (test or reserve pads) must not be connected to ITO tracks. Connecting dummy pads may compromise the ESD protection of the LCD module because these pads have no ESD protection elements.

### 5.2 Hardware reset pad

In COG applications, the interface and supply lines have a higher impedance compared to COB, TCP, or COF. The resistance of individual lines may differ in value considerably from one ITO track to the next. This difference may be hundreds of ohms. As a result it is possible to generate a large differential voltage across the ITO tracks during an EMC event. The RESET pad recognizes such an EMI-induced voltage spike (of the order of 5 ns) as a reset command. To prevent this, a low-pass filter is built into the RESET pad of the LCD driver ICs.

### 5.3 Power supply tracks $V_{SS}$ and $V_{DD}$

To further increase EMC immunity NXP recommends that the resistance of the ITO tracks and connections for the power supply -  $V_{DD1}$ ,  $V_{DD2}$ ,  $V_{DD3}$ ,  $V_{SS1}$ ,  $V_{SS2}$  - must be reduced as much as possible.

### 5.4 Unused pins

When pins are not used in the application (e.g. test pins, unused interface pins etc.) it may be a requirement that these pins are tied to  $V_{DD1}$  or  $V_{SS1}$  (tied off). In this case, it is important to make the connection to  $V_{DD1}$  or  $V_{SS1}$  as direct as possible. Sometimes

so-called tie-off pads are provided for this purpose (called  $V_{xx1}$  TIEOFF or similar). If there are no tie-off pads, then the connection must be made directly to the  $V_{DD1}$  or  $V_{SS1}$  pads (see [Figure 8](#)).

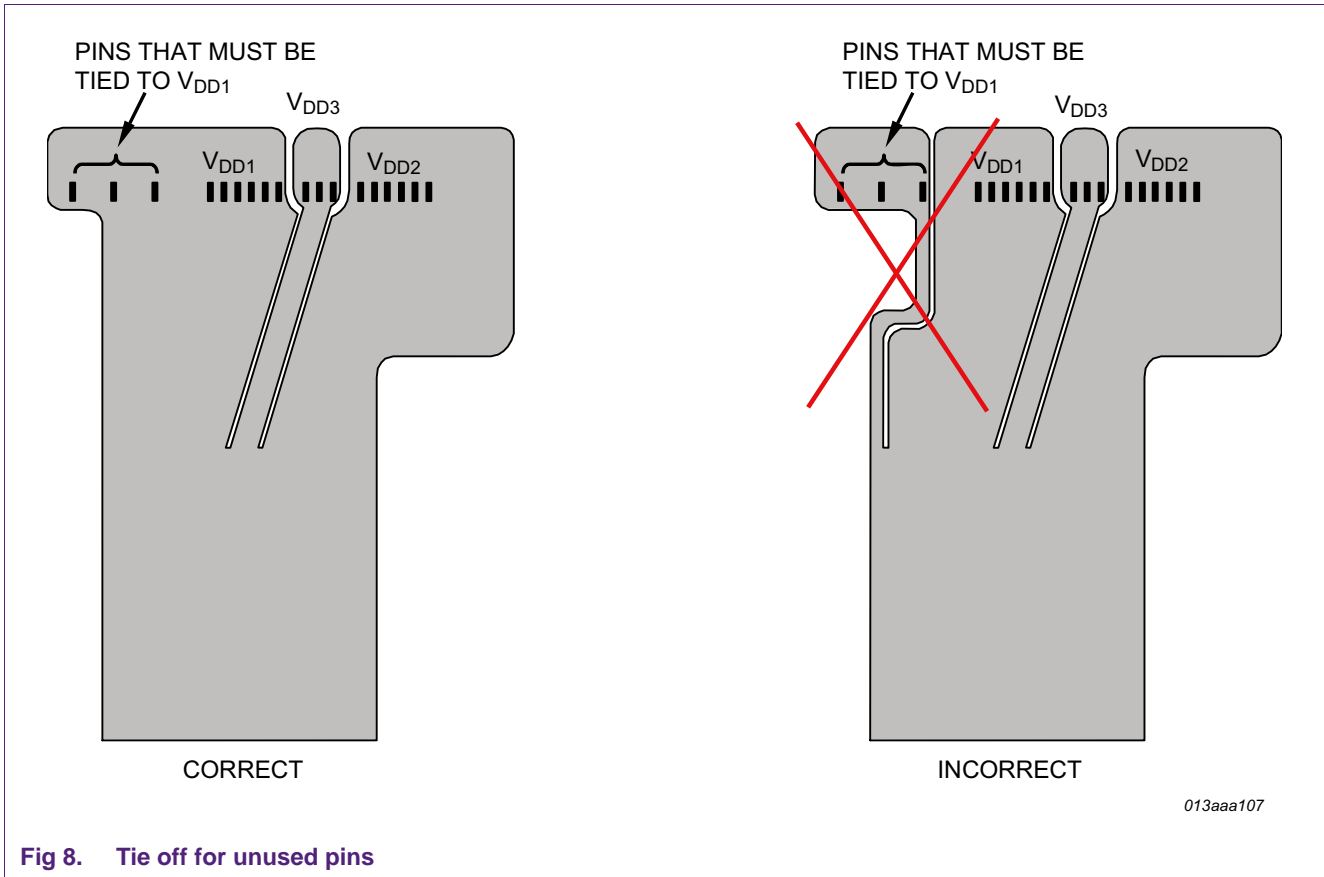


Fig 8. Tie off for unused pins

## 6. Hard and soft gold bumps

After conventional IC fabrication, the bonding pads of LCD drivers for COG application are plated with gold bumps, which allow the LCD driver to be bonded directly to contact pads on a flex foil, or on the display glass. Here the chip is mounted upside-down in what is known as 'flip chip' geometry. Gold ball bumping is an evolution of the more than 50 year old gold wire bonding process. Because of the maturity of the wire bonding process, these bump connections are very reliable.

In COG manufacturing, the chips are mounted on a glass substrate. The chip is bonded directly to the conductive ITO tracks on the glass, using Anisotropic Conductive Film (ACF), see [Figure 9](#). ACF is the name given to the combination of the conductive particles, metallic particles (as small as  $3\ \mu\text{m}$  to  $5\ \mu\text{m}$ ) or metal-coated polymer balls together with the adhesive resin. ACF is actually a non-conductive film containing dispersed microscopic conductive particles. Anisotropic refers to directionally different properties. The conductive adhesive becomes conductive only in the Z-direction, which is the direction in which it is being compressed during assembly of the COG module. The compressed adhesive is that which is trapped between the bump and the glass. When this is compressed, conductive particles inside the epoxy will align themselves and create a

conductive path between the die and the ITO tracks. There is no conductive path in the X or Y direction. This is of course also required as it would create a shorting path between the bumps.

Besides bonding to glass, the chip can be bonded to a foil as well (chip on foil, COF).

Gold bumps (also known as studs) can be divided in so called hard and soft bumps. The Au hardness is expressed in HV (Vickers). The border between soft and hard is not a very strict division and there is a small overlap in the definitions that are commonly used in the industry.

1. Soft bumps: 35 HV - 80 HV
2. Hard bumps: 60 HV - 120 HV

Whether to use hard or soft bumps depends on the application (assembly process. i.e COG or COF) and sometimes also a bit on user preference.

In general, for COG products, the bumps need to be harder because the harder bumps could bear/brake ACF particles which could be located below the gold bumps. When the bumps are harder, the connection will be established after breaking the ACF particles during the COG manufacturing process. If the bump is soft, it is difficult to bear/break the ACF particles. Experiments have shown that using gold bumps with a hardness of 70 HV leads to a lower contact resistance compared to a 40 HV gold bump. Also the pressure applied to the chip during bonding has an influence on the final contact resistance.

Therefore, with COG the typical hardness used is around 70 HV to 75 HV (50 HV ~ 100 HV or 55 HV ~ 95 HV).

For Chip-on-foil (COF) products, the hardness should be lower due to the assembly process. The typical hardness here is around 50 HV (35 HV ~ 65 HV).

Balls do have a non-conductive polymer layer which gets pushed away when they are trapped between the gold bump and the ITO.

The main reason for wanting hard bumps is that the particles are a kind of “hard” themselves. As a result, the particle will be pushed into the bump in case the bump is soft.

This again results in a larger increase in contact resistance over lifetime, as the particle has less compression when pushed into the bump compared to being squeezed between bump and substrate.

Also bump pitch and bump gap play a role in the choice. With decreasing gaps, this becomes more of an issue. Soft bumps will easily show bump deformation and hence reduction of resulting gap. If it was too small to start with, short circuits may be formed. Usually with hard bumps the gap between bumps needs to be at least three times the diameter of the conductive particles in order to prevent short circuiting. Using soft bumps results in a wider gap being required.

In addition, soft bumps need to be processed by annealing. This is not necessary for hard bumps. Annealing is a heat treatment that alters a material to make it more workable. It involves heating a material to above its critical temperature, maintaining a suitable temperature, and then cooling. It can a.o. soften material, relieve internal stresses, refine the structure by making it homogeneous, and improve cold working properties.

As a consequence of the above, hard bumps are more widely used than soft bumps in the manufacturing of COG display modules.

## 7. Guidelines for COG mounting

### 7.1 COG bonding conditions

The COG bonding conditions described are based on practical experience within NXP Semiconductors and must be used as a guideline. The COG bonding conditions in each application must be validated using reliability and reproducibility tests. Special care must be taken in analyzing the following parameters after COG bonding to prevent abnormalities:

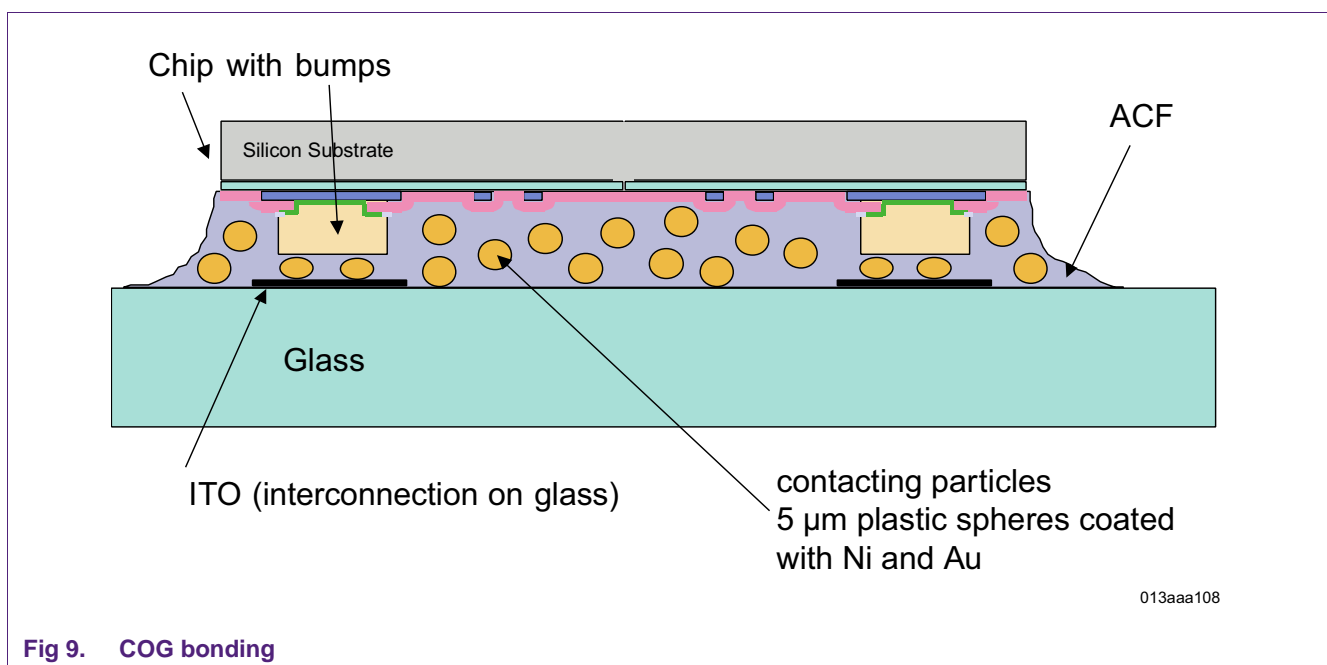
- bump height
- bump deformation
- bump roughness
- IC passivation integrity
- uniform ACF particle density.

Special care must be taken in the COG bonding production facility to:

- avoid dust and other alien particles interfering with the COG bonding process
- avoid ESD overstress during COG bonding.

### 7.2 COG Bonding parameters

[Figure 9](#) shows a drawing of COG bonding with ACF.



The following parameters apply to all COG bonding (Au bumps) processes:

- bonding pressure as a function of total bump area of the IC: 12 kg / mm<sup>2</sup>
- ACF temperature 220 °C ± 10 °C.

## 8. Sensitivity to light

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Semiconductors are sensitive to light. Any p-n junction, if illuminated, is potentially a photodiode. Semiconductor devices such as transistors and ICs contain p-n junctions, and will not function correctly if they are illuminated by unwanted electromagnetic radiation (light) of a wavelength suitable to produce a photocurrent.

Some LCD drivers contain a One Time Programmable (OTP) memory. UV radiation entering the driver could erase the OTP.

Therefore devices must be shielded against light. If this is not done properly, transistors and ICs can malfunction and will show increased current consumption due to induced photo-currents. In COG applications, the driver IC and the chip-on-glass bonds must therefore be sealed by coating the chip in black epoxy. To prevent light from entering the IC (especially important for backlit displays), a small black sticker is glued on the glass, underneath the driver IC.

## 9. References

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- [1] **AN11267** — EMC and system level ESD design guidelines for LCD drivers
- [2] **AN11494** — Cascading NXP LCD segment drivers
- [3] **PCA2117** — Automotive LCD driver for character displays
- [4] **PCF2113x** — LCD controllers/drivers
- [5] **PCF2116x** — LCD controllers/drivers
- [6] **PCF2119x** — LCD controllers/drivers
- [7] **PCF21219** — LCD driver for character displays
- [8] **PCA85132** — LCD driver for low multiplex rates
- [9] **PCA85133** — Automotive LCD driver for low multiplex rates
- [10] **PCA85232** — LCD driver for low multiplex rates
- [11] **PCA85233** — Automotive LCD driver for low multiplex rates
- [12] **PCA8538** — Automotive 102 x 9 Chip-On-Glass LCD segment driver
- [13] **PCA8576D** — Automotive 40 x 4 LCD segment driver for low multiplex rates
- [14] **PCA8576F** — Automotive LCD driver for low multiplex rates
- [15] **PCA9620** — 60 x 8 LCD high-drive segment driver for automotive and industrial
- [16] **PCF85132** — LCD driver for low multiplex rates
- [17] **PCF85133** — Universal LCD driver for low multiplex rates
- [18] **PCF8532** — Universal LCD driver for low multiplex rates
- [19] **PCF8533** — Universal LCD driver for low multiplex rates
- [20] **PCF8534A** — Universal LCD driver for low multiplex rates
- [21] **PCF8538** — Universal 102 x 9 Chip-On-Glass LCD segment driver
- [22] **PCF8576C** — Universal LCD driver for low multiplex rates
- [23] **PCF8576D** — Universal LCD driver for low multiplex rates
- [24] **PCF8576E** — Universal LCD driver for low multiplex rates
- [25] **PCF8577C** — LCD direct/duplex driver with I<sup>2</sup>C-bus interface
- [26] **R\_10015** — Chip-On-Glass (COG) - a cost-effective and reliable technology for LCD displays
- [27] **UM10204** — I<sup>2</sup>C-bus specification and user manual

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