

## Multimedia Applications Processors - HD Video, High-End, Advanced Applications, Arm® Cortex®-A8 Core

## i.MX537

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The i.MX53 family of processors represents NXP's next generation of advanced multimedia and power-efficient implementation of the Arm® Cortex®-A8 core. With core processing speeds up to 800 MHz, the i.MX537 is optimized for both performance and power to meet the demands of high-end, advanced applications. Integrated display controller, 1080p HD video decode and 720p video encode, enhanced graphics and connectivity features make the i.MX537 ideal for a wide range of applications such as Human Machine Interfaces (HMI) and patient monitors which require rich user interfaces with high color displays and user interaction.

The i.MX537 provides key environmental differentiators for the industrial market. These include 3.3V I/O support, a 0.8 mm pitch package to reduce PCB and manufacturing costs, extended temperature coverage for harsh environments, industrial qualification for extended reliability and a formal long product supply guarantee to support product life spans.

The i.MX537 is supported by a companion NXP power management IC (PMIC), MC34709.

## i.MX537 Multimedia Applications Processor Block Diagram Block Diagram

PWM x 2 EPIT x 2 GPU  Power Mgmt. and Analog  LDO Supply x 2 32 kHz Osc  x 2 VPU  Wideo Encode/	System Control		Core/Internal Memory			Standard Connectivity	
Smart DMA  System Buses  Neon  VFP  ROM  RAM  RAM  RAM  Advanced Connectivity  HS USB OTG + PHY  Ethernet + IEEE* 158  HS Host + PHY  CAN x2/MLB 50  HS ULPI Host x 2  Camera Interface  LDO Supply x2  PU  Video Encode/ Decode  PLL x 4  PU  Security  Fuses  RTIC  Sahara v4  SCC v2  ROM  RAM  RAM  I*C x 3  GPIO  Advanced Connectivity  HS USB OTG + PHY  Ethernet + IEEE* 158  HS Host + PHY  CAN x2/MLB 50  Fuse IPU  External Memory I/F  2 GB DDR2/DDR3/LV-DDR2/LP-DDR2  External Storage I/F  SLC/MLC NAND  SATA  NOR  MMC/SD	Clock Reset		ARM® Cortex™-A8			Fast IrDA	UART x 5
Timers  GPT Watchdog x 2  PWM x 2 EPIT x 2  Power Mgmt. and Analog LDO Supply x 2  PLL x 4  Security  Full x 4  Security  Full x 4  Full	Smart DMA		Cache	ETM		CSPI	Keypad
ROM RAM  Advanced Connectivity  HS USB OTG + PHY Ethernet + IEEE® 158  Multimedia HS Host + PHY CAN x2/MLB 50  HS ULPI Host x 2  Camera Interface  VPU Video Encode/ Decode TV Out  PLL x 4  Security FFuses RTIC Sahara v4 SCC v2  ROM RAM  Advanced Connectivity HS USB OTG + PHY Ethernet + IEEE® 158  HS Host + PHY CAN x2/MLB 50  HS ULPI Host x 2 Camera Interface  External Memory I/F  2 GB DDR2/DDR3/LV-DDR2/LP-DDR2  External Storage I/F SLC/MLC NAND SATA  NOR  Multimedia HS Host + PHY CAN x2/MLB 50  TV Out  External Storage I/F SLC/MLC NAND SATA  NOR  MINOR  MINOR  MOR  PMC/SD			Neon	VFP		I2C x 3	GPIO
PWM x 2 EPIT x 2	Watchdoo		POM	DOM DAM		Advanced Connectivity	
PWM x 2	GPT		NOW	rivi		HS USB OTG + PHY	Ethernet + IEEE® 1588
Power Mgmt. and Analog  LDO Supply x2  32 kHz Osc  PLL x 4  Security  Fuses  RTIC  Sahara v4  SCC v2  PoenGL ES 2.0  OpenVG 1.1  HS ULPI Host x 2  External Memory I/F  2 GB DDR2/DDR3/LV-DDR2/LP-DDR2  External Storage I/F  SLC/MLC NAND  SATA  NOR  MMC/SD	PWM x 2	EPIT x 2			,	HS Host + PHY	CAN x2/MLB 50
LDO Supply x 2 32 kHz Osc VPU External Memory I/F Video Encode/ Decode TV Out 2 GB DDR2/DDR3/LV-DDR2/LP-DDR2  PLL x 4 IPU External Storage I/F Security Enlancement Inversion and Camera Rotation Interface De-Interlacing/  Sahara v4 SCC v2 External Memory I/F  2 GB DDR2/DDR3/LV-DDR2/LP-DDR2  External Storage I/F SLC/MLC NAND SATA  NOR eMMC/SD	Power Mami	and Analog			Ē	HS ULPI Host x 2	Camera Interface
Video Encode/ Decode TV Out  PLL x 4  IPU  Resizing and Blending Enhancement Inversion and Rotation Interface  Sahara v4 SCC v2  Video Encode/ Decode TV Out  IPU  Resizing and Blending Enhancement Inversion and Camera Rotation Interface De-Interlacing/			VOL		1	External Memory I/F	
Security  EFuses  RTIC  Sahara v4  SCC v2  Resizing and Blending Enhancement Inversion and Rotation Interface  De-Interlacing/  Security  External Storage I/F  SLC/MLC NAND  SATA  NOR  eMMC/SD		32 kHz Osc	Video Encode/			2 GB DDR2/DDR3/LV-DDR2/LP-DDR2	
Security  EFuses  RTIC  Sahara v4  SCC v2  Resizing and Blending Enhancement Inversion and Camera Rotation Interface De-Interlacing/  De-Interlacing/	PLL x 4		IPU		1		
Blending Enhancement SLC/MLC NAND SATA  Inversion and Rotation Interface NOR eMMC/SD  De-Interlacing/	Security			Image	١.	External S	torage I/F
Sahara v4 SCC v2 Rotation Interface NOR eMMC/SD  De-Interlacing/						SLC/MLC NAND	SATA
De-Interlacing/		1000000				NOR	eMMC/SD
	TrustZone					PATA	
System Debug Audio Display I/F	System	Debug	Audio			Display I/F	
ESAI SPDIF Tx/Rx Analog VGA Out Parallel (from IPU			ESAI	SPDIF Tx/Rx		Analog VGA Out	Parallel (from IPU)
Secure JTAG SSI/I'S x 3 ASRC LVDS	Secure JTAG		SSI/I <sup>2</sup> S x 3	ASRC	Ī	LVDS	

View additional information for Multimedia Applications Processors - HD Video, High-End, Advanced Applications, Arm® Cortex®-A8 Core.

Note: The information on this document is subject to change without notice.

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