Mini High-Speed CAN System Basis Chip for Partial Networking

UJA1168ATK

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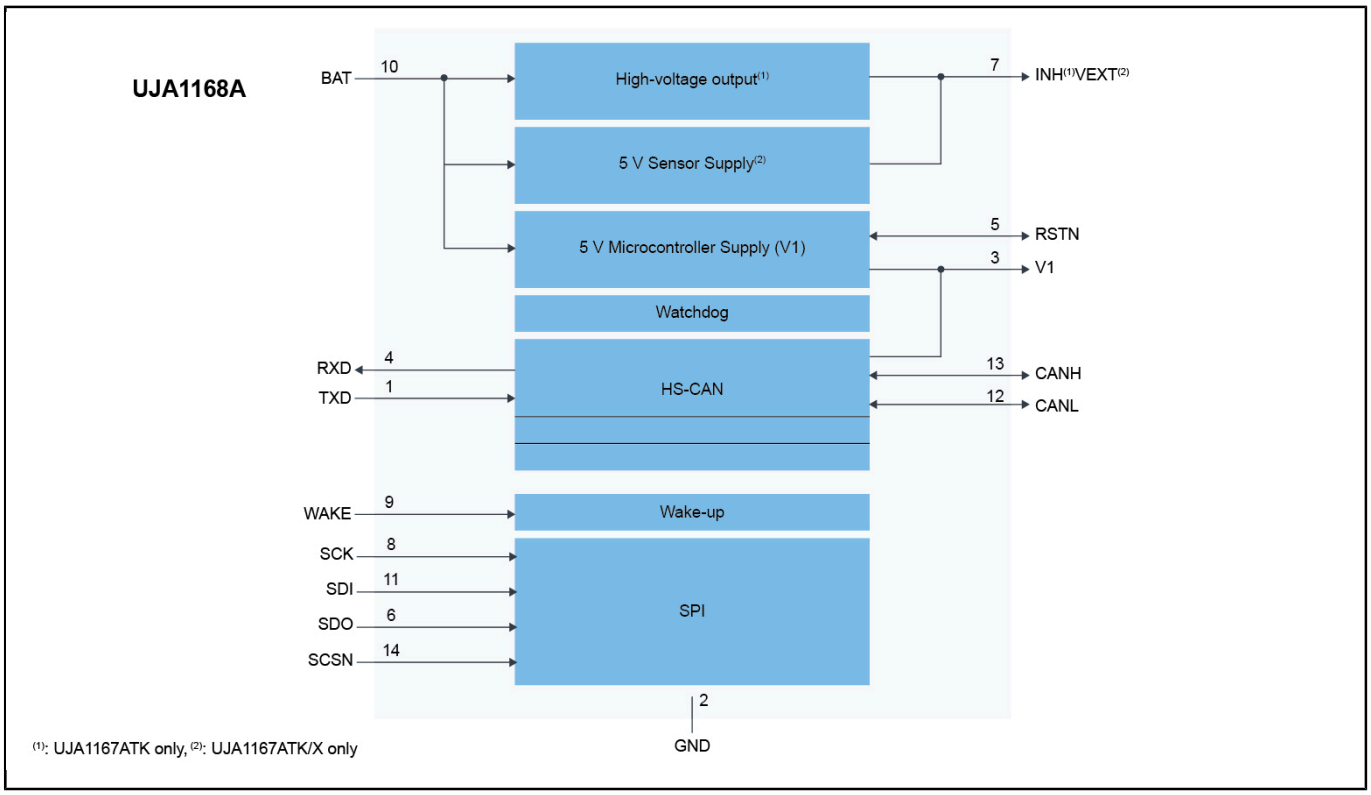
The UJA1168ATK is a mini high-speed CAN system basis chip (SBC) containing an ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant HS-CAN transceiver supporting CAN FD up to 5 Mbit/s together with a 5 V/100 mA supply for a microcontroller. It also features a watchdog and a serial peripheral interface (SPI).

The UJA1168ATK can be operated in very-low-current standby and sleep modes and supports CAN partial networking by means of a selective wake-up function. A dedicated implementation of the partial networking protocol called “FD-passive” has been embedded as well.

A number of configuration settings are stored in non-volatile memory, allowing the SBC to be adapted for use in a specific application.

UJA1168ATK Block Diagram Block Diagram



View additional information for Mini High-Speed CAN System Basis Chip for Partial Networking.

Note: The information on this document is subject to change without notice.