

8-Bit LVTTL-to-GTL Transceiver

GTL2018PW

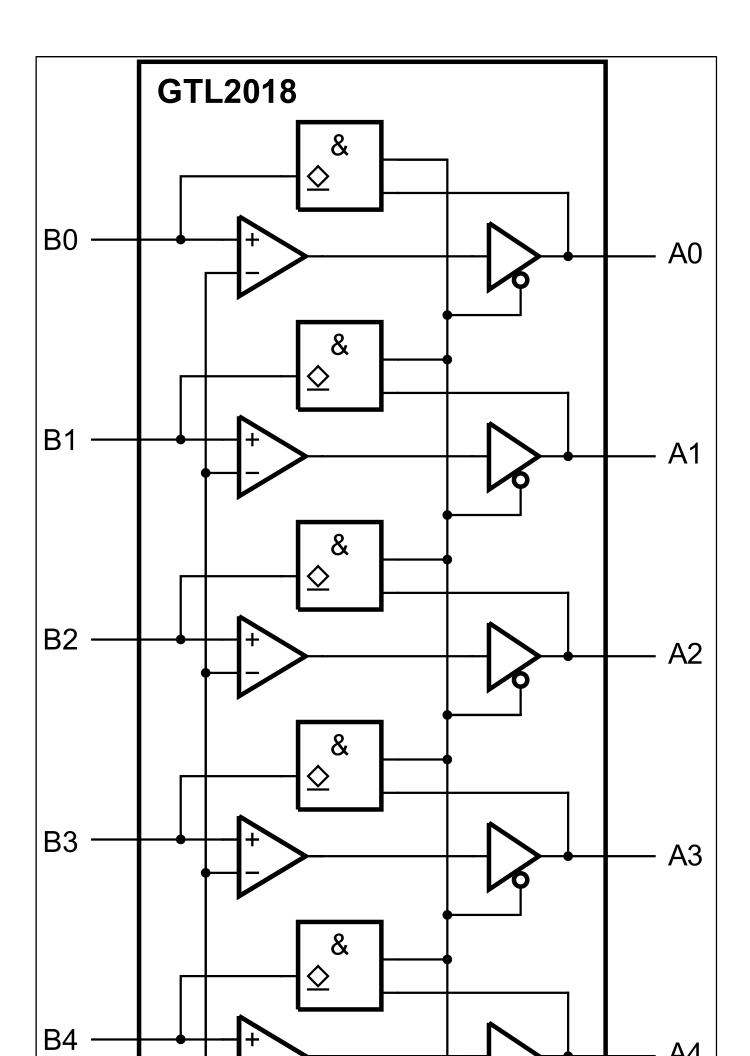
Last Updated: Mar 15, 2024

The GTL2018 is an octal translating transceiver designed for 3.3 V LVTTL system interface with a GTL-/GTL/GTL+ bus.

The direction pin (DIR) allows the part to function as either a GTL-to-LVTTL sampling receiver or as an LVTTL-to-GTL interface.

The GTL2018 LVTTL inputs (only) are tolerant up to 5.5 V, allowing direct access to TTL or 5 V CMOS inputs.

GTL2018 Block Diagram Block Diagram



Note: The information on this document is subject to change without notice.

www.nxp.com

View additional information for 8-Bit LVTTL-to-GTL Transceiver.

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2024 NXP B.V.