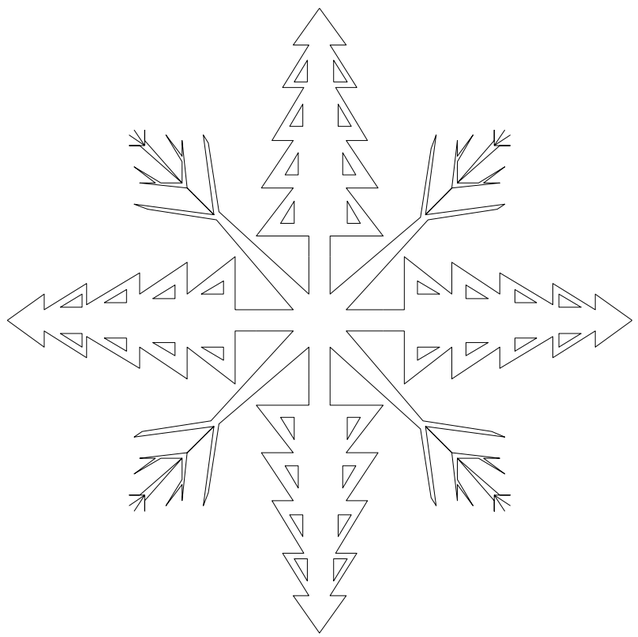
freescale™
semiconductor



High Performance Computing Platform II

SCH-20935

freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:15:18 am	Title: Cover Story		Page: 01
1	2	3	4	5	6	7	8

Schematic Notes

1. Unless otherwise specified:
   All resistors are SMD0402, in ohms, 0.08W, +/-5%
   All capacitors are SMD0402, in microfarads (uF), +/-20%.
   All inductances are in microhenries (uH).
   All ferrites are Z=50 ohms at 100 MHz.
   All fuses are self-resetting polyswitch (PTC) devices.
   Board impedance is 60 +/- 6 ohms.
   Pronunciation guide: tî gə
2. Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:

   VCC_3.3 VCC_2.5 GND VCC_3.3_REG
   VCC_5 VCC_1.2 VCORE
3. Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.
4. Freescale and the Freescale logo are registered trademarks of Freescale Semiconductor. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. Take off--it's a beauty way to go!
5. The sheet-to-sheet cross reference format is:
   Sheet VertZoneLetter HorizZoneNumber
6. Components with the label "No_Stuff" are not to be installed by default; they are for test or manufacturing purposes only.

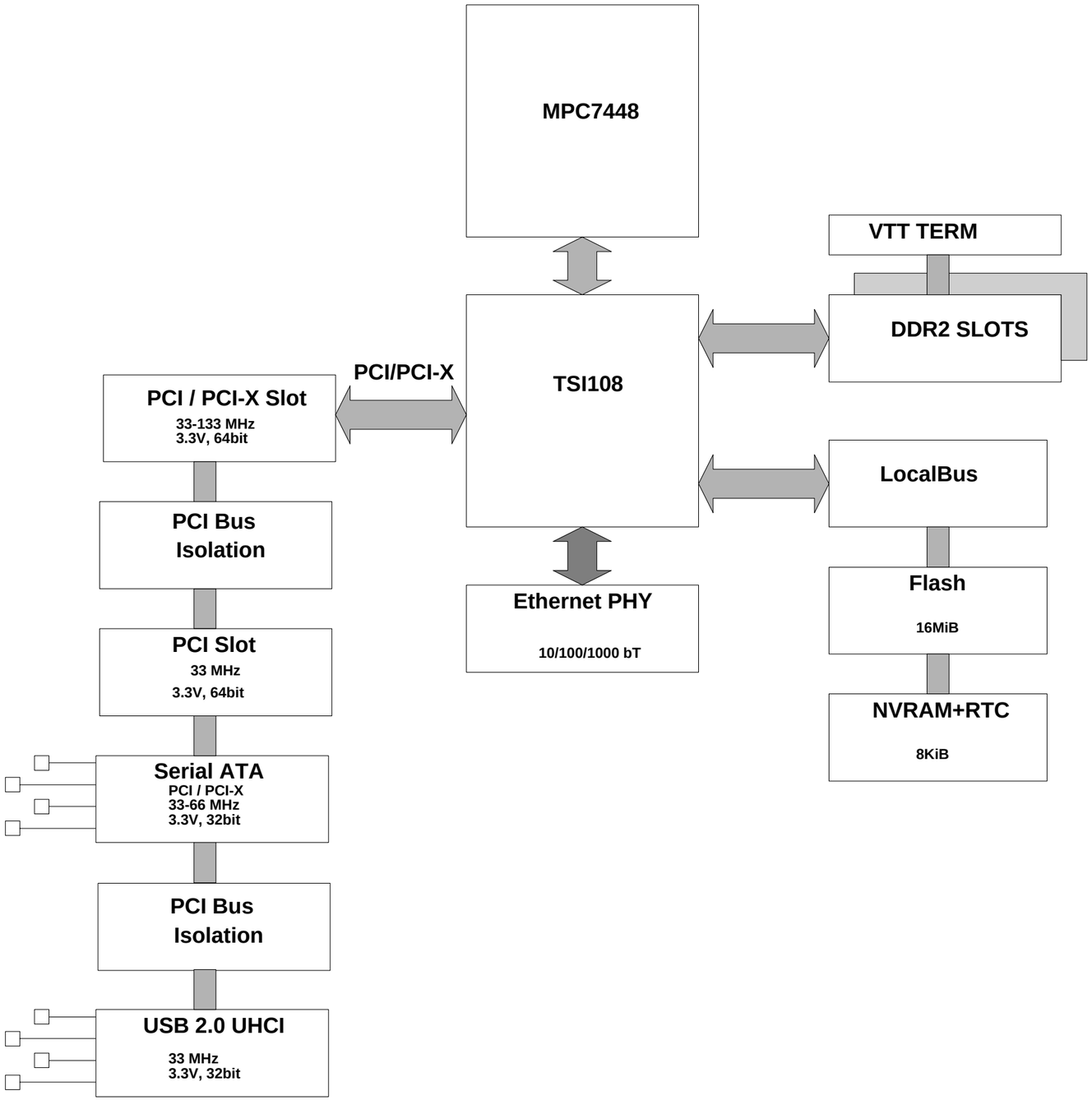
7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

This schematic is provided for reference purposes only. All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. Contact Freescale Sale/FAEs to obtain the latest information on this product.

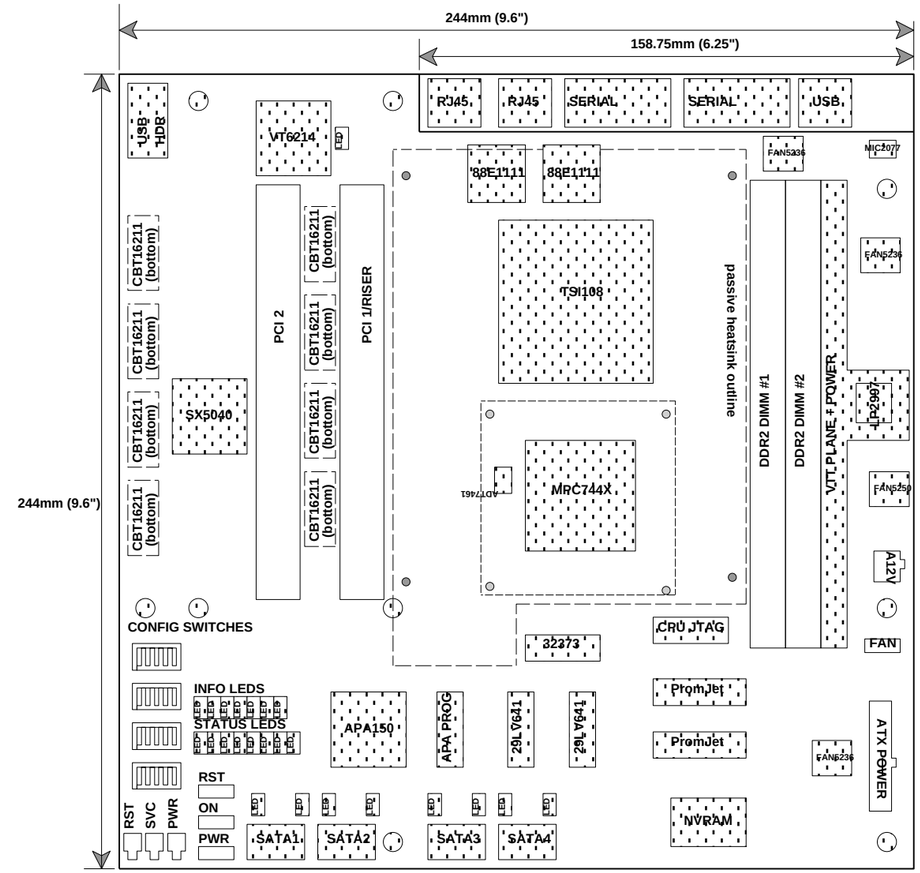
HPC II

SCH-20935

REV	DATE	DESCRIPTION / MAJOR CHANGES
V0	Nov2004	Initial version
V1	Jan2005	Prototype
V2	May2005	Added VCC_3.3_REG rail Deleted external clk generator Corrected local bus addressing Modified local bus placement

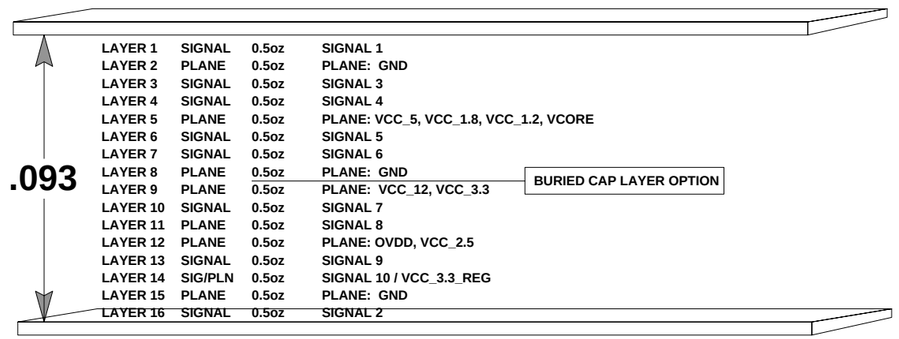


freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:15:45 am	Title: Block Diagram		Page: 03



- Mounting holes, positioned per microATX spec.
- Mounting holes for passive thermal cooling.
- Mounting holes for conventional fansink.

No components higher than 2.70 mm permitted inside passive heatsink outline



LAYER 1	SIGNAL	0.5oz	SIGNAL 1
LAYER 2	PLANE	0.5oz	PLANE: GND
LAYER 3	SIGNAL	0.5oz	SIGNAL 3
LAYER 4	SIGNAL	0.5oz	SIGNAL 4
LAYER 5	PLANE	0.5oz	PLANE: VCC_5, VCC_1.8, VCC_1.2, VCORE
LAYER 6	SIGNAL	0.5oz	SIGNAL 5
LAYER 7	SIGNAL	0.5oz	SIGNAL 6
LAYER 8	PLANE	0.5oz	PLANE: GND
LAYER 9	PLANE	0.5oz	PLANE: VCC_12, VCC_3.3
LAYER 10	SIGNAL	0.5oz	SIGNAL 7
LAYER 11	PLANE	0.5oz	SIGNAL 8
LAYER 12	PLANE	0.5oz	PLANE: OVDD, VCC_2.5
LAYER 13	SIGNAL	0.5oz	SIGNAL 9
LAYER 14	SIG/PLN	0.5oz	SIGNAL 10 / VCC_3.3_REG
LAYER 15	PLANE	0.5oz	PLANE: GND
LAYER 16	SIGNAL	0.5oz	SIGNAL 2

BURIED CAP LAYER OPTION

freescale™ semiconductor

Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729

Project: Taiga
Revision: 2.0

Engineer: Michael Everman

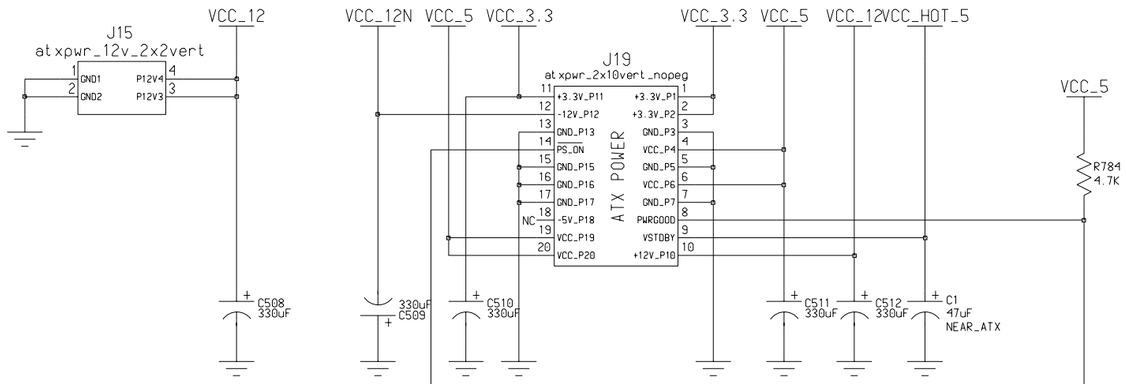
Date Changed: 11/11/2005
Time Changed: 11:15:54 am

Title: Placement (approximate) and PCB Stackup

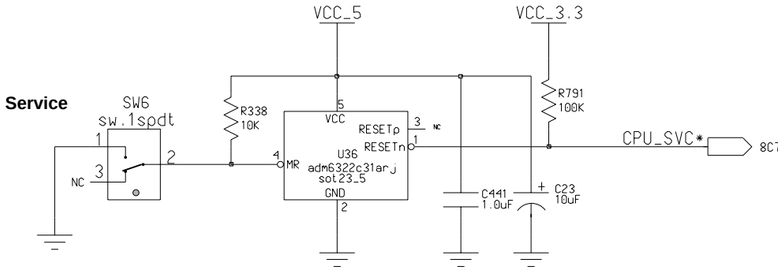
Page: 04

ATX CHASSIS POWER

VCC and VCC_3.3 on separate power planes.

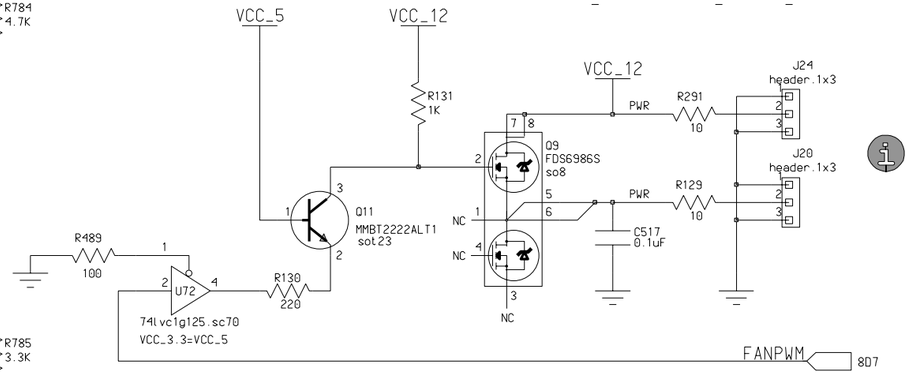


CPU0 Service

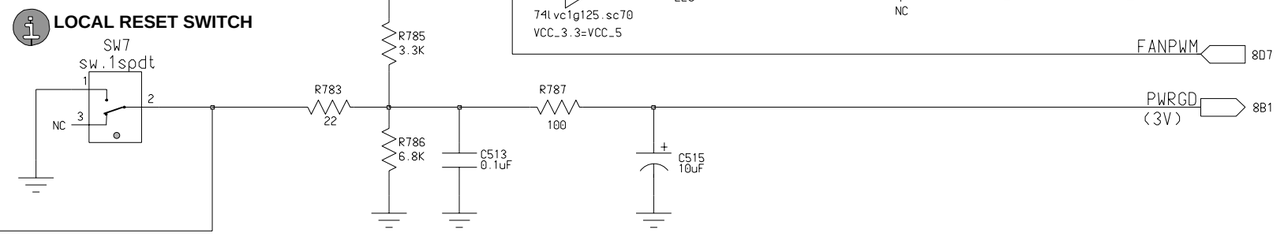


FANSINK HEADER

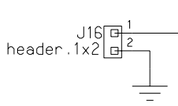
1A Maximum



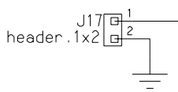
LOCAL RESET SWITCH



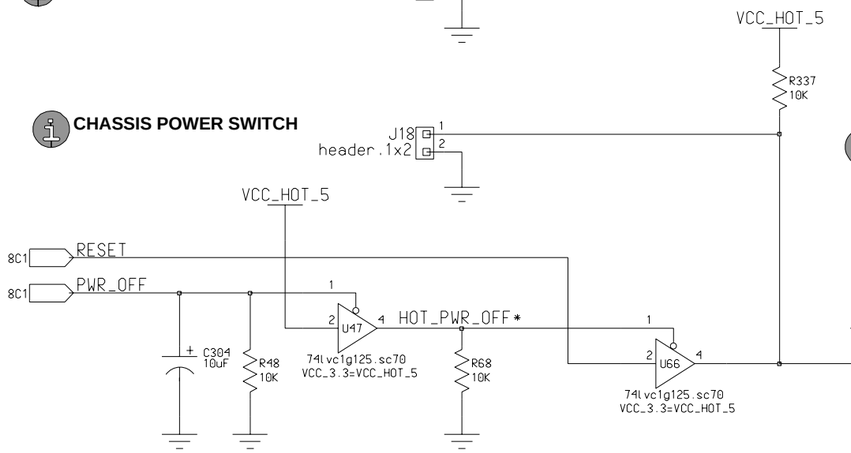
CHASSIS RESET SWITCH



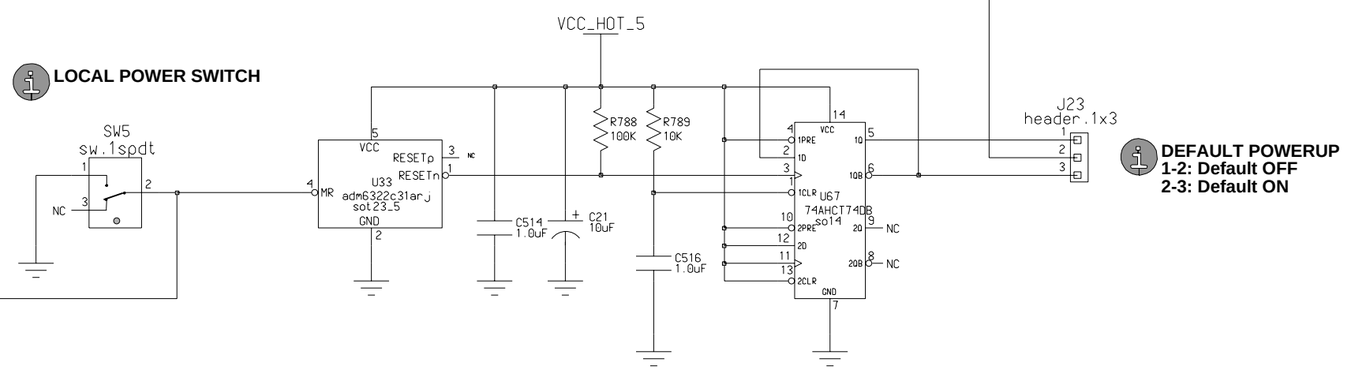
FORCE PSU ALWAYS ON



CHASSIS POWER SWITCH



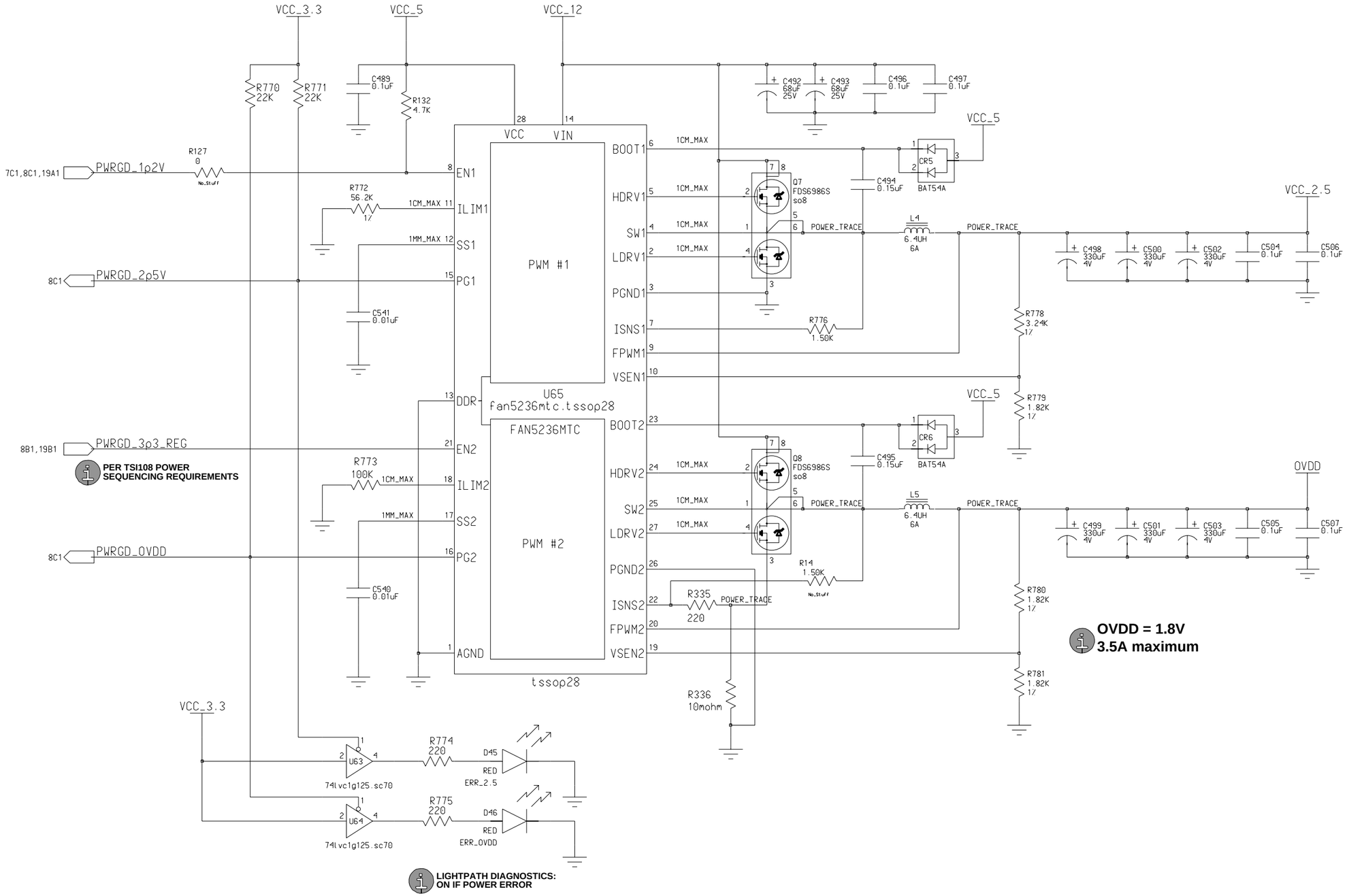
LOCAL POWER SWITCH



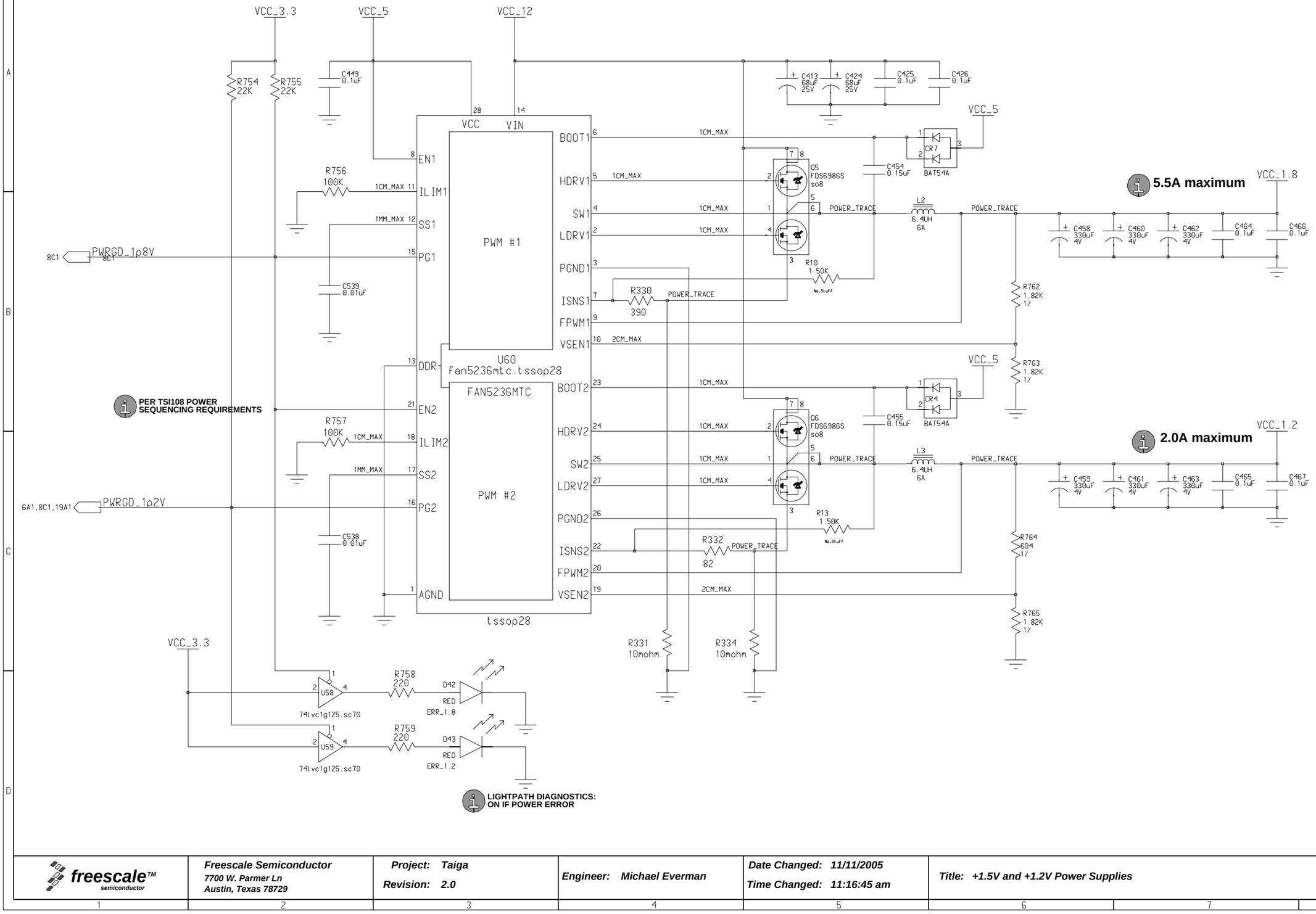
DEFAULT POWERUP

1-2: Default OFF
2-3: Default ON

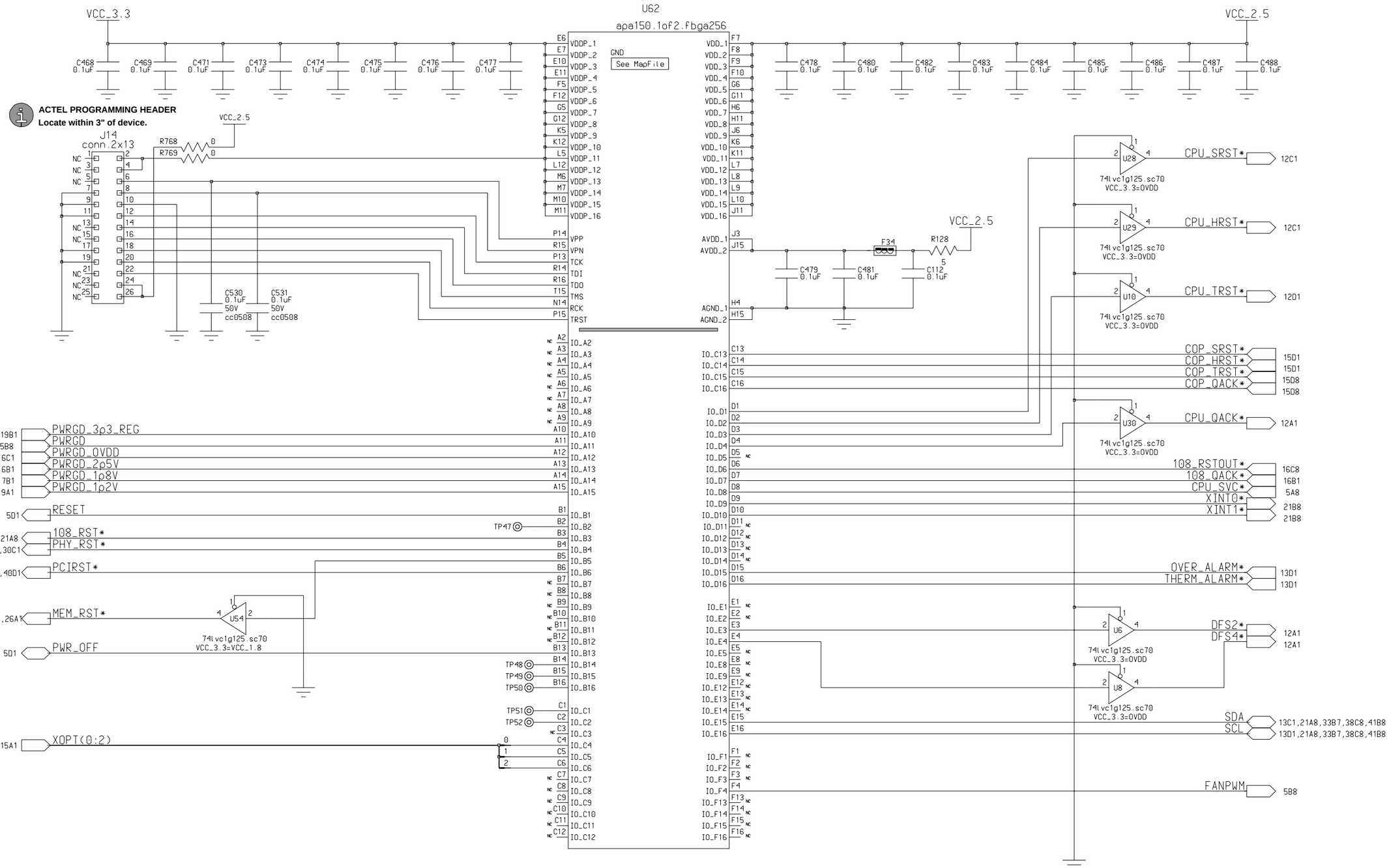
freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:16:05 am	Title: Chassis Connections / Power Control		Page: 05



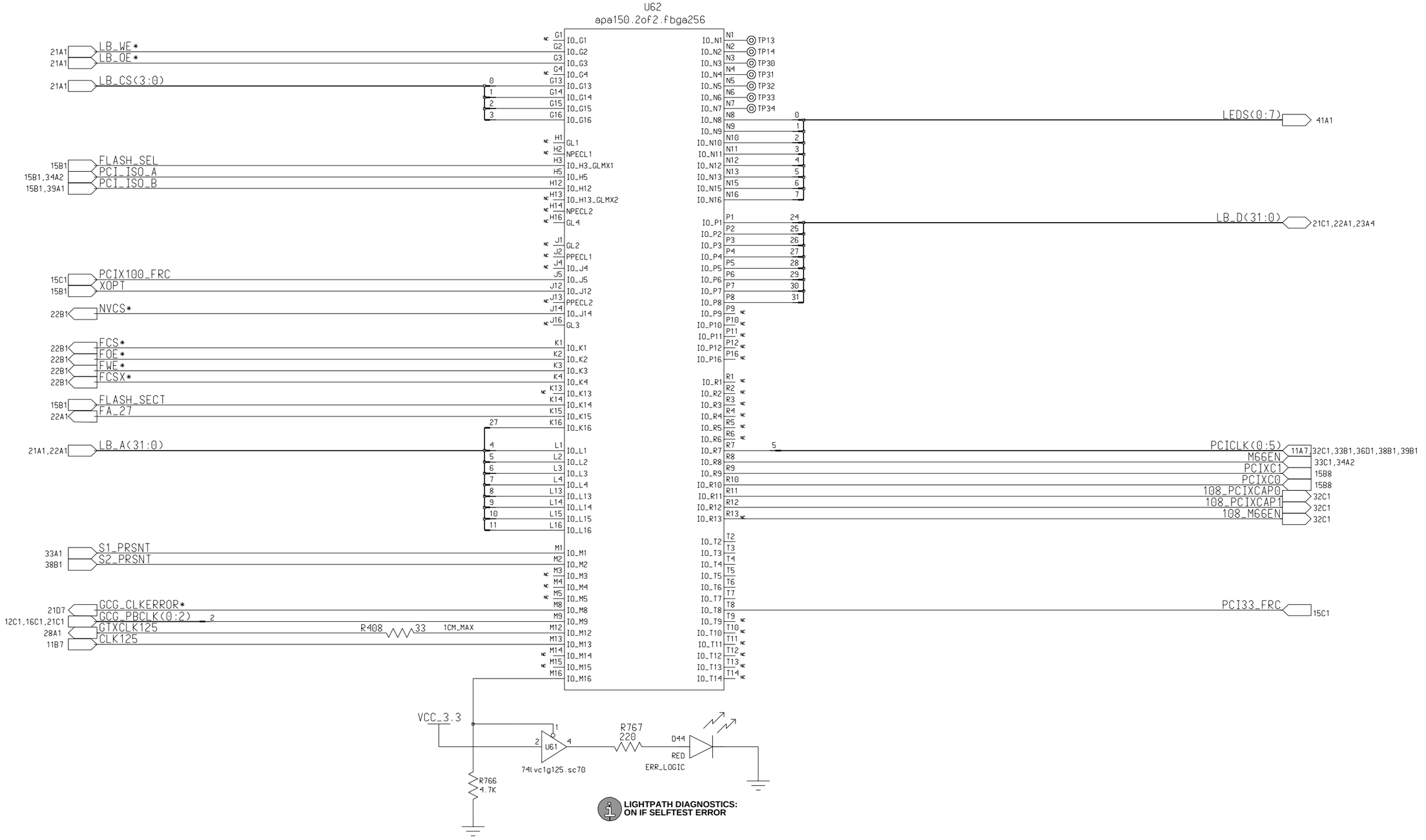
freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:16:15 am	Title: Power: +2.5V and OVDD (Nominally 1.8V)		Page: 06
1	2	3	4	5	6	7	8



freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:16:45 am	Title: +1.5V and +1.2V Power Supplies		Page: 07
1	2	3	4	5	6	7	8



freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:16:25 am	Title: System Control Logic (part I)		Page: 08
1	2	3	4	5	6	7	8



freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:16:35 am	Title: System Logic (part II)		Page: 09

1	2	3	4	5	6	7	8

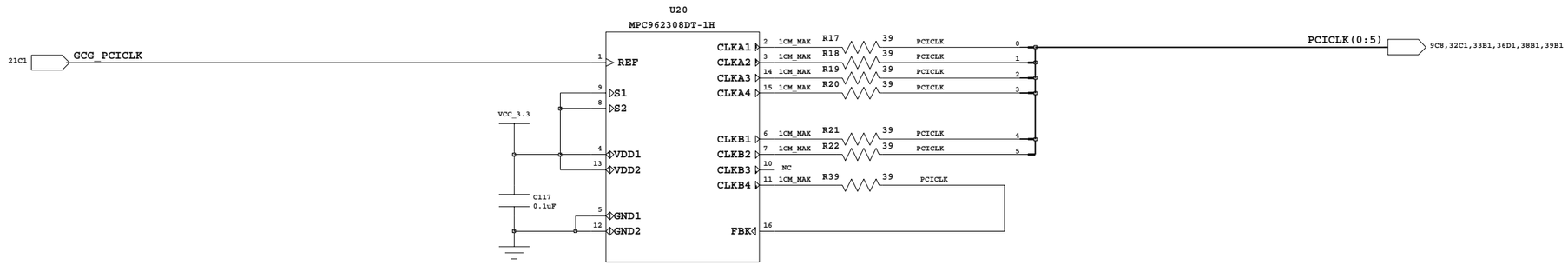
freescale semiconductor
Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729

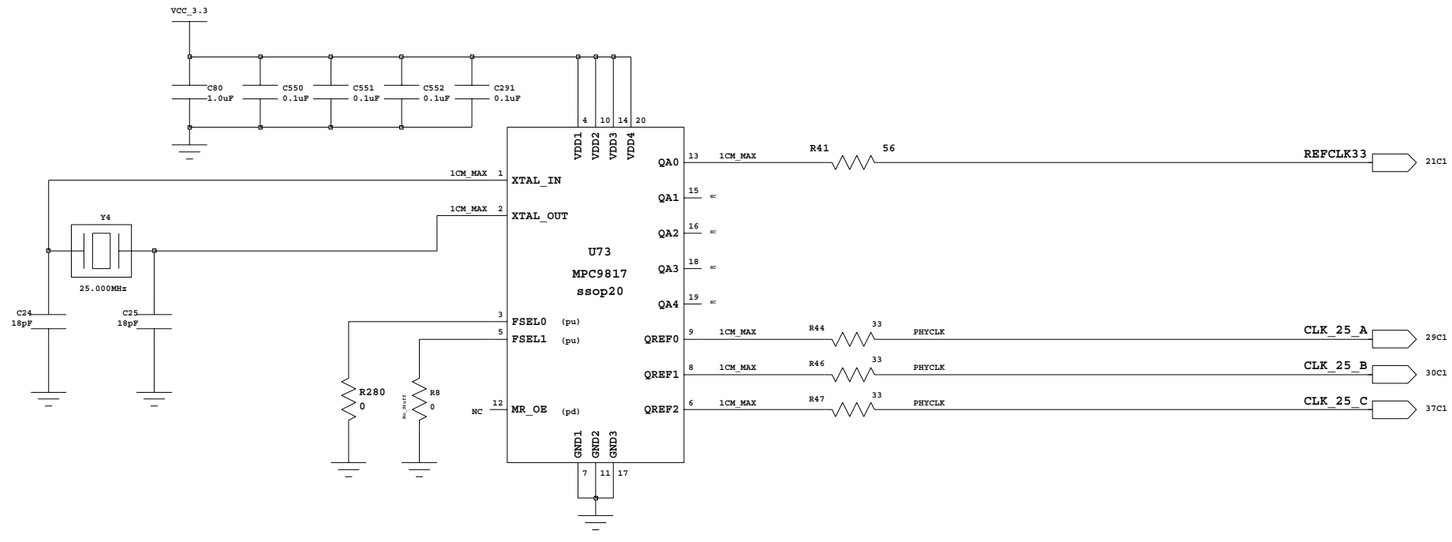
Project: Taiga
Revision: 2.0

Engineer: Michael Everman

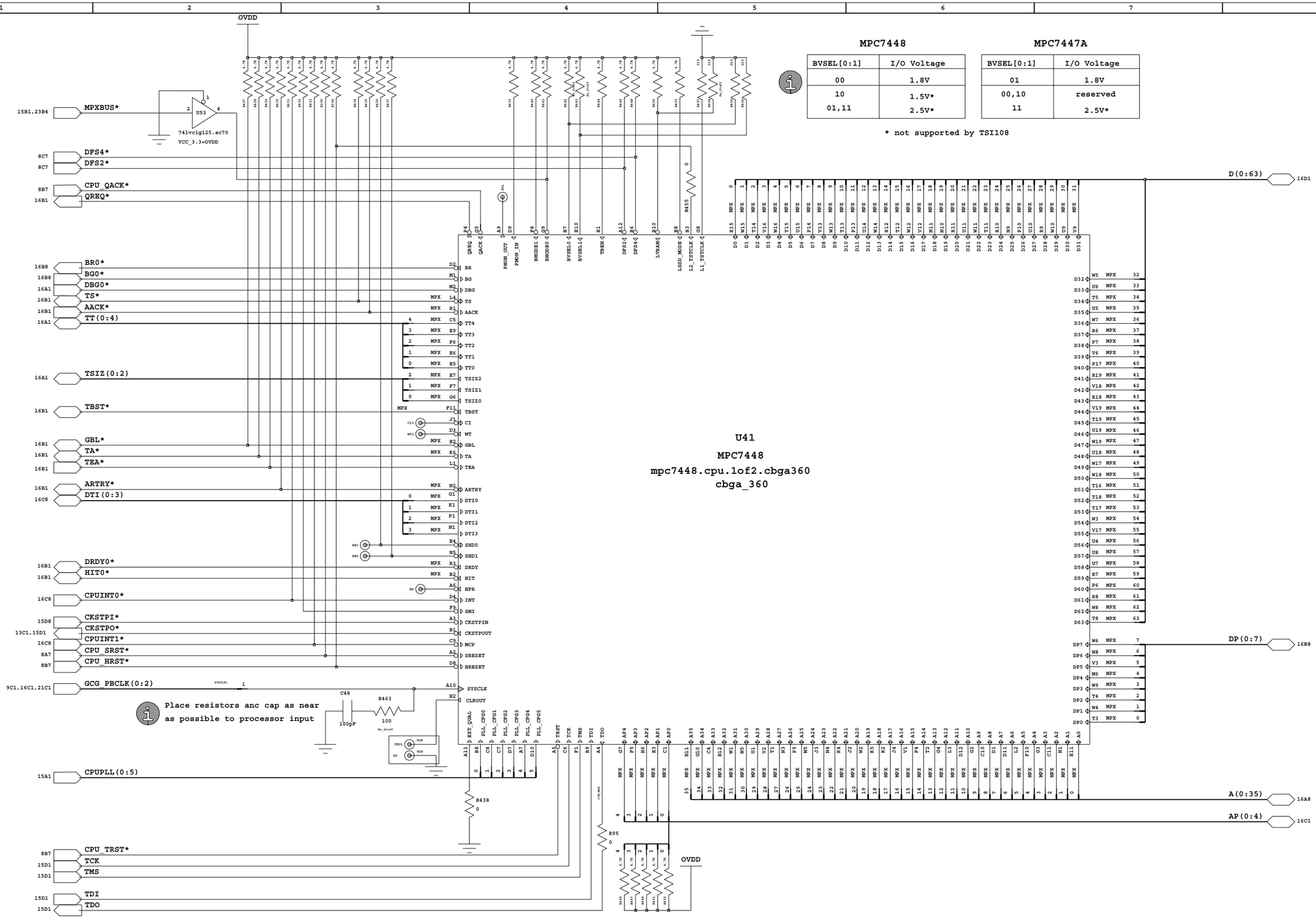
Date Changed: 11/11/2005
Time Changed: 11:22:20 am

Title: reserved





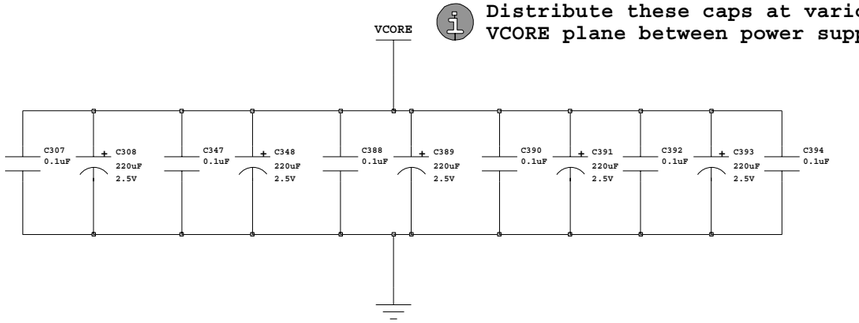
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:22:11 am	Title: PCI Clock Fanout and Other Clocks	Page: 11

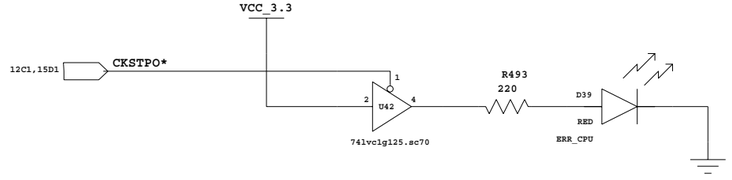


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:16:56 am	Title: Processor #0		Page: 12

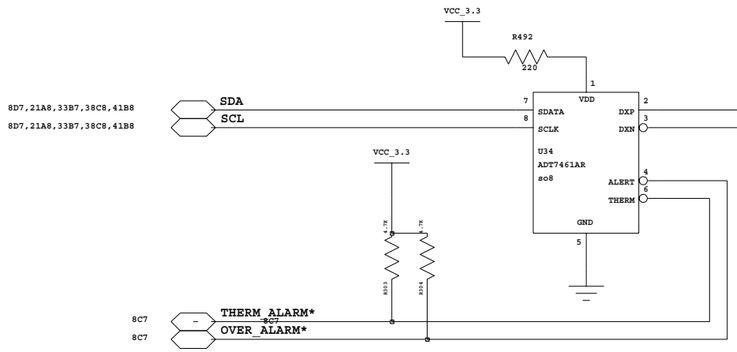
Place caps as close as possible to CPU power pins; see AN2747 for escape pattern and capacitor placement recommendations

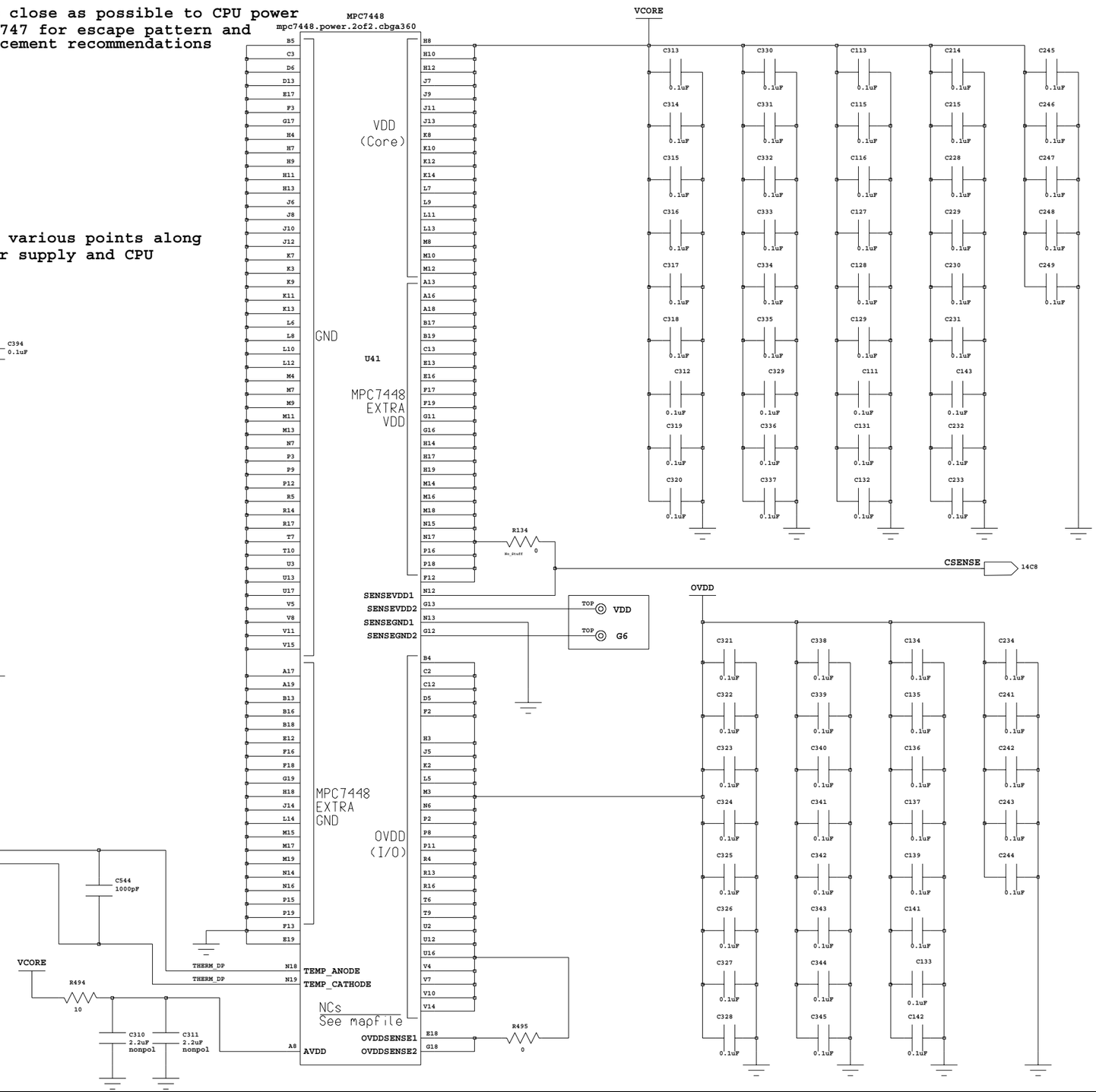
Distribute these caps at various points along VCORE plane between power supply and CPU



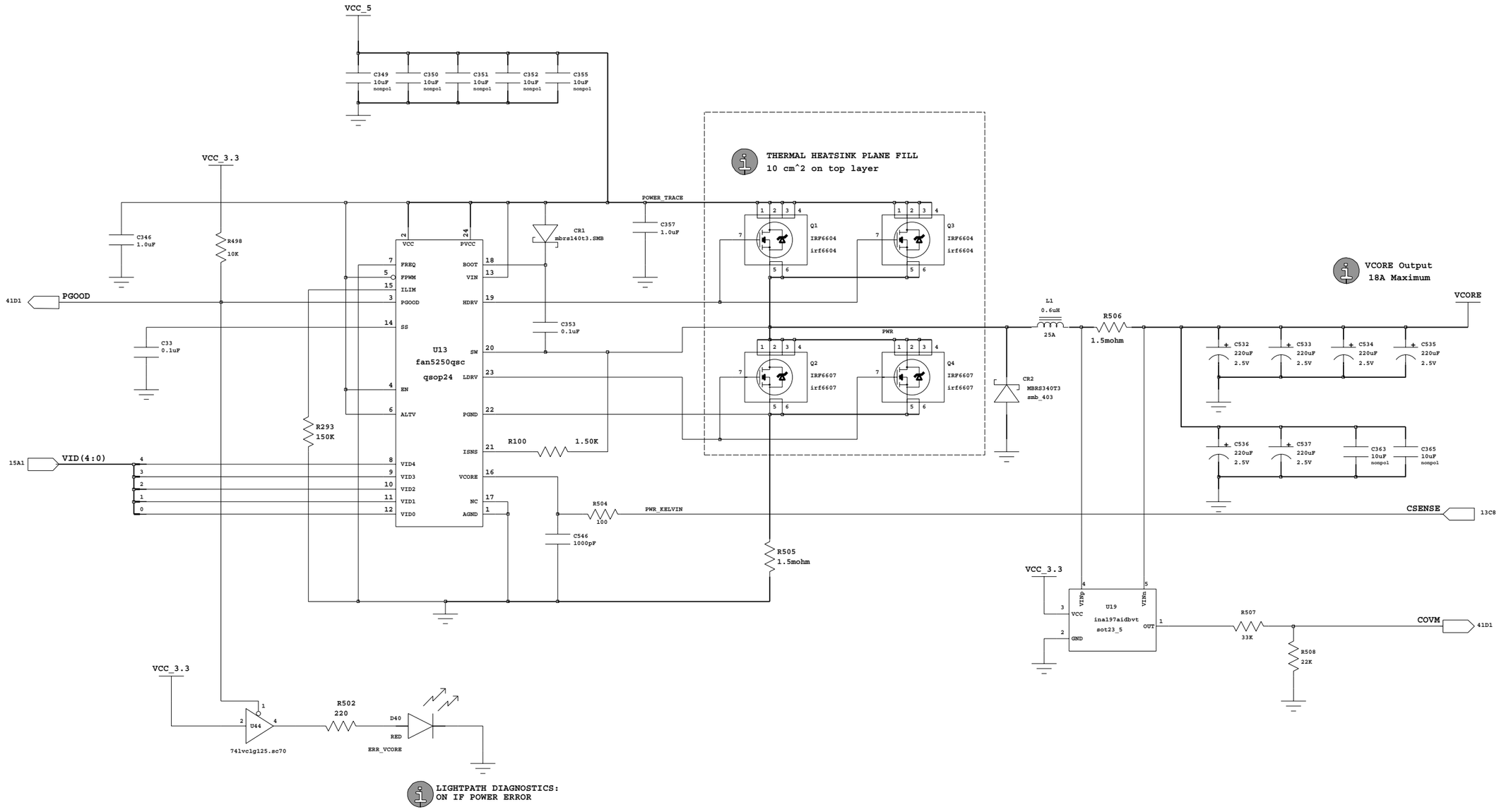


LIGHTPATH DIAGNOSTICS: ON IF POWER ERROR





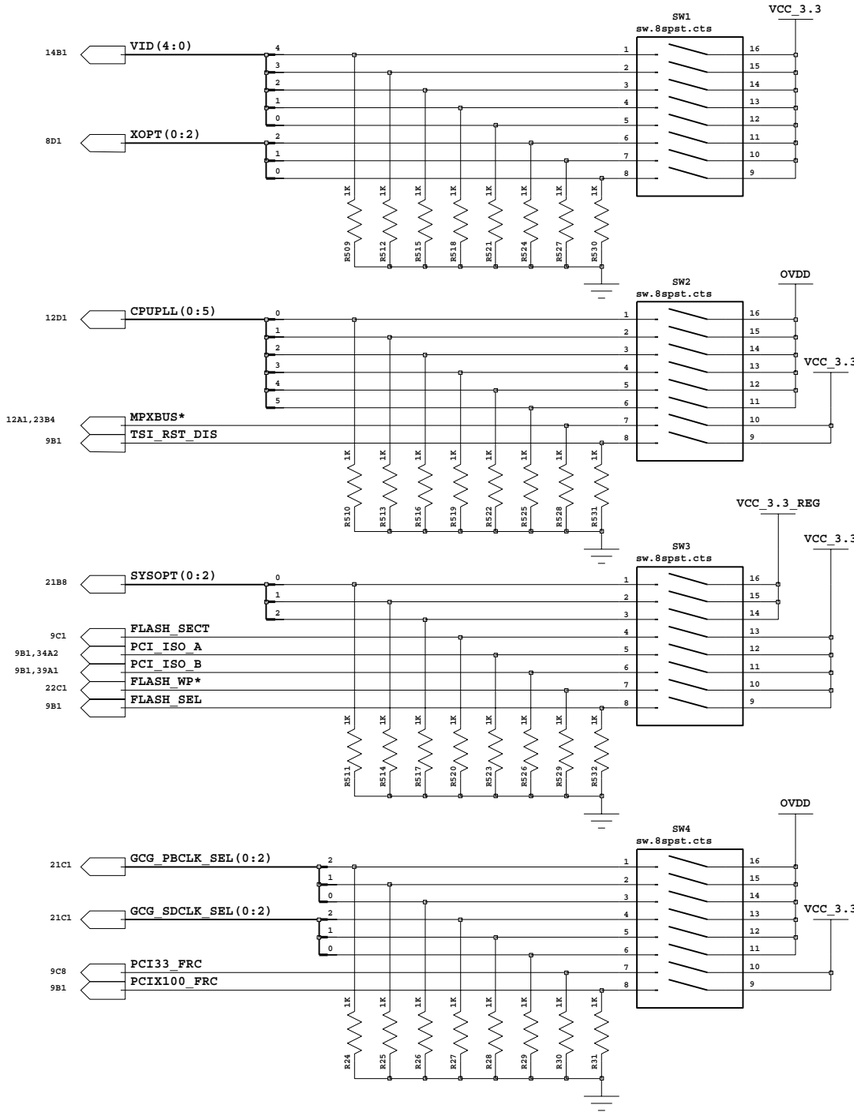
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:17:08 am	Title: MPC7447A Power Connections	Page: 13



POWER SUPPLY LAYOUT RULES

1. All components in the power path (large/red bus) should be on the same layer, with area filled connections.
2. No vias or thermal reliefs allowed on power path components.
3. Ground plane connections should be made with two vias close to the component.

freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:22:00 am	Title: Processor Power Supply	Page: 14



VCORE OUTPUT
VID[4:0] = 01111 = 1.0V
VID[4:0] = 01101 = 1.1V
VID[4:0] = 01011 = 1.2V
VID[4:0] = 01001 = 1.3V

XOPT
For optional configuration of FPGA

BUS PROTOCOL
0 = MPX; 1 = 60X

TSI_RST_DIS
0 = allow TSI108 to reset CPU (default)
1 = do not allow TSI108 to reset CPU

SOFTWARE OPTIONS
Software-dependant

FLASH SECTOR SELECT
0 = normal, 1 = invert LB_A[27] to boot from high half of flash

PCI BUS ISOLATION
PCI_SLOT0_ISO: 0 = Normal; 1= Isolated (Slot0 only)
PCI_SATA_ISO: 0 = Normal; 1= Isolated (Slot0 and SATA only)

FLASH WRITE PROTECT BOOTBLOCK
0 = Protected; 1 = Writable

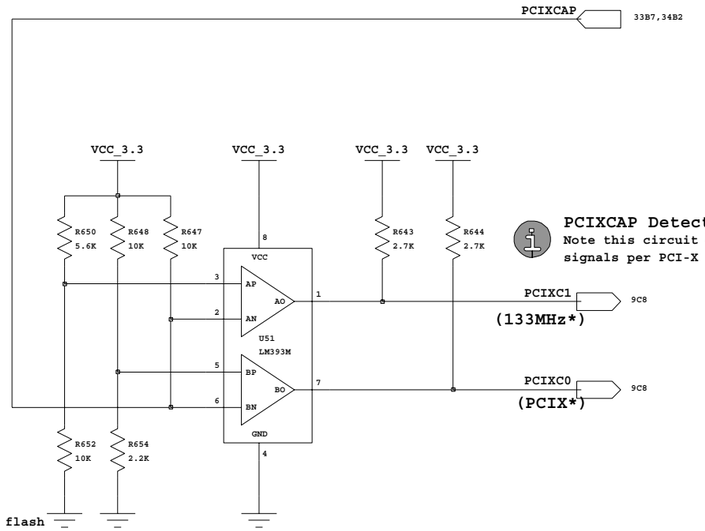
FLASH SELECT
0 = Normal; 1 = PromJet Flash Emulator

TSI108 CG SYSCLK FREQUENCY
See TSI08 datasheet

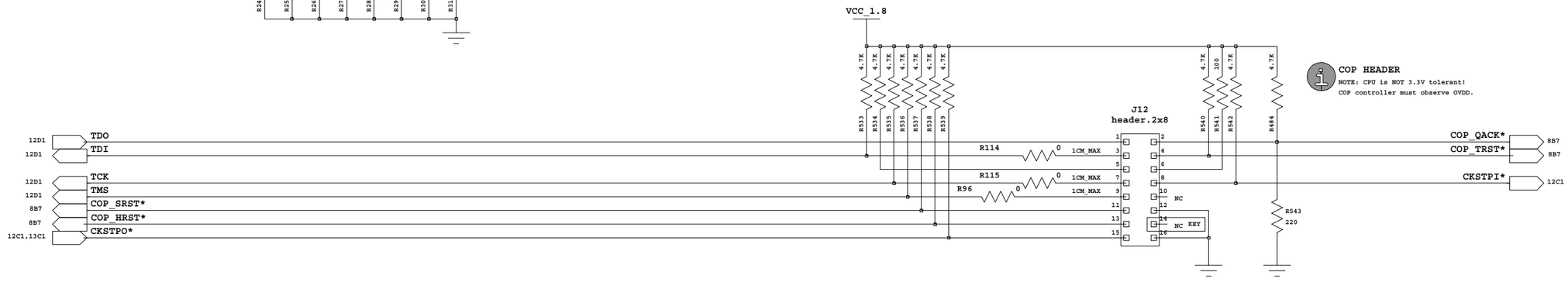
TSI108 CG DDR2 CLOCK FREQUENCY
See TSI108 datasheet

PCI33 FORCE
0 = Normal; 1 = Force 33 MHz PCI bus

PCI-X 100 FORCE
0 = Allow PCI-X 133 MHz; 1 = Limit PCI-X to 100 MHz

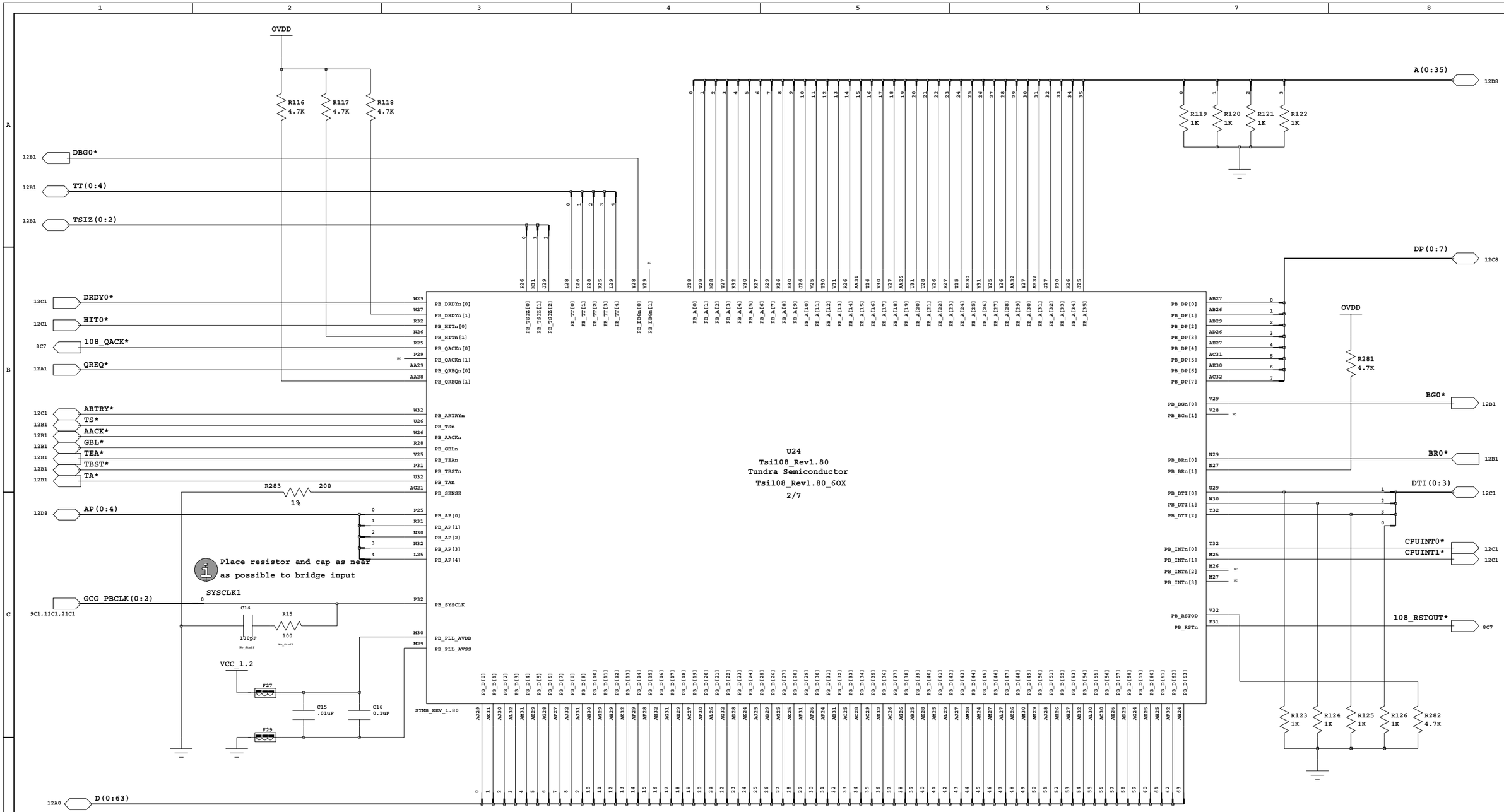


PCIXCAP Detect
Note this circuit generates active low signals per PCI-X spec example circuit



COP HEADER
NOTE: CPU is NOT 3.3V tolerant!
COP controller must observe OVDD.

freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:17:19 am	Title: COP, Configuration and PCIXCAP	Page: 15



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:17:30 am	Title: TSI108 MPX Bus Interface		Page: 16

1	2	3	4	5	6	7	8

freescale semiconductor

Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729

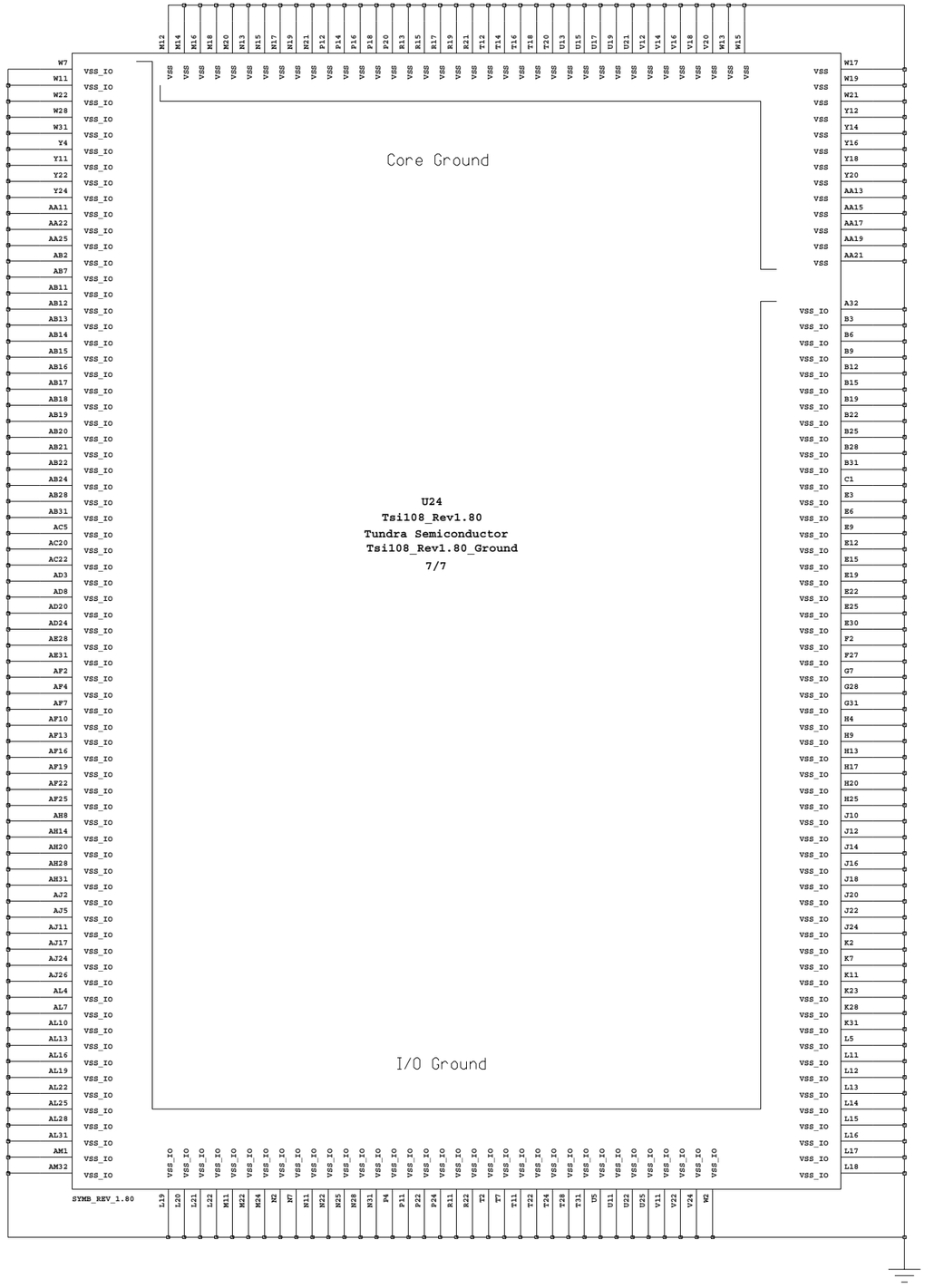
Project: Taiga
Revision: 2.0

Engineer: MIchael Everman

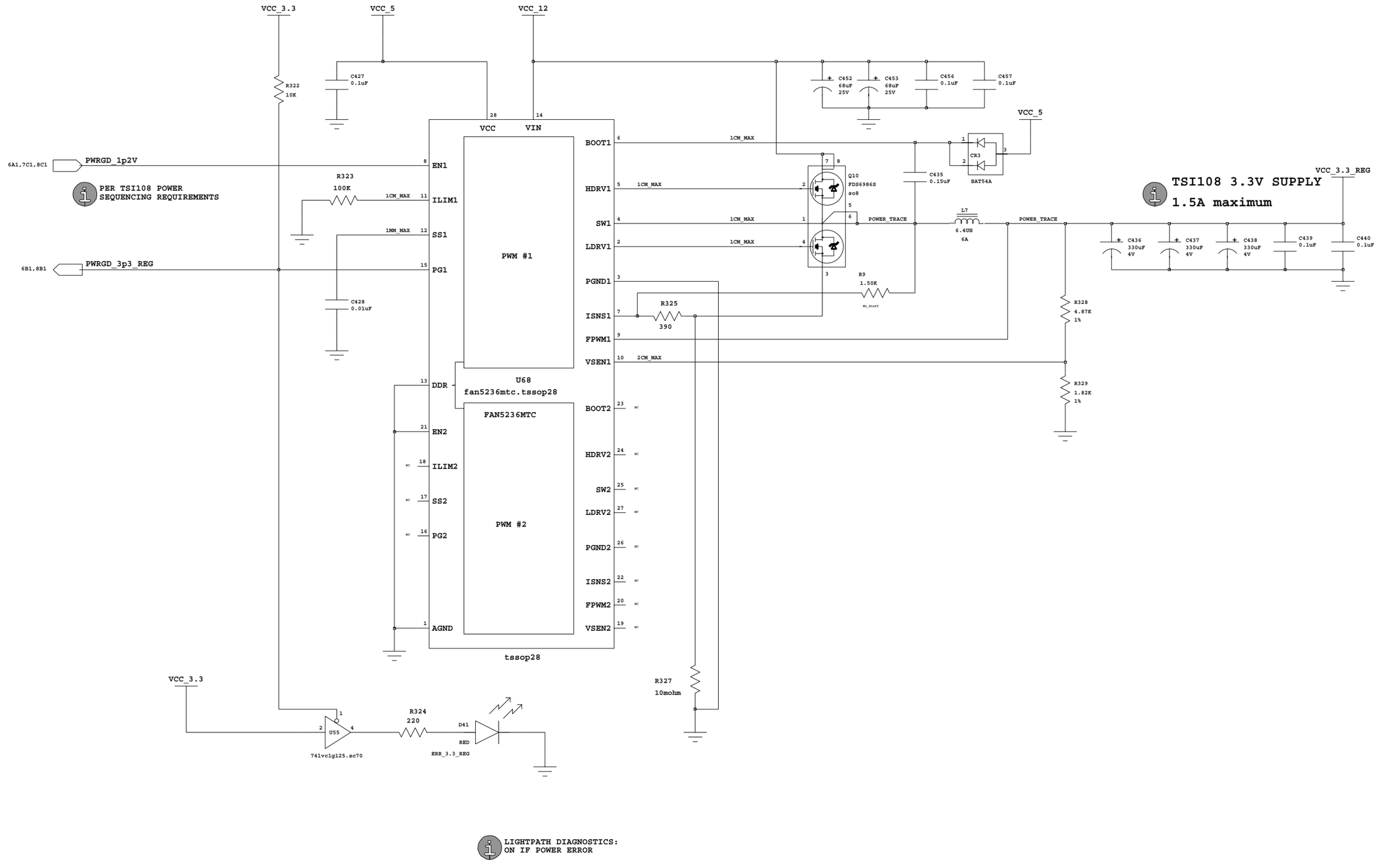
Date Changed: 11/11/2005
Time Changed: 11:17:41 am

Title: --reserved--

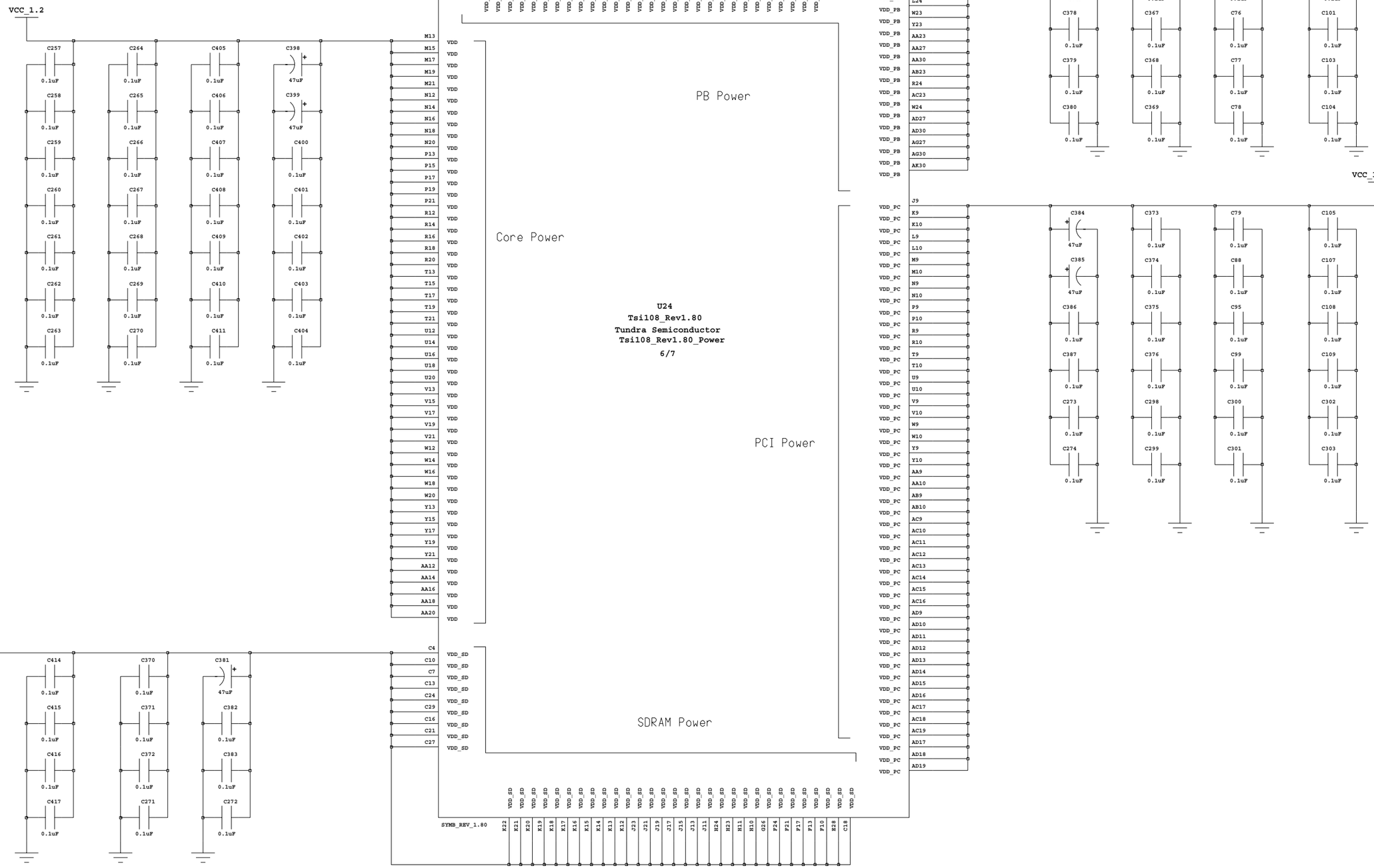
Page: 17



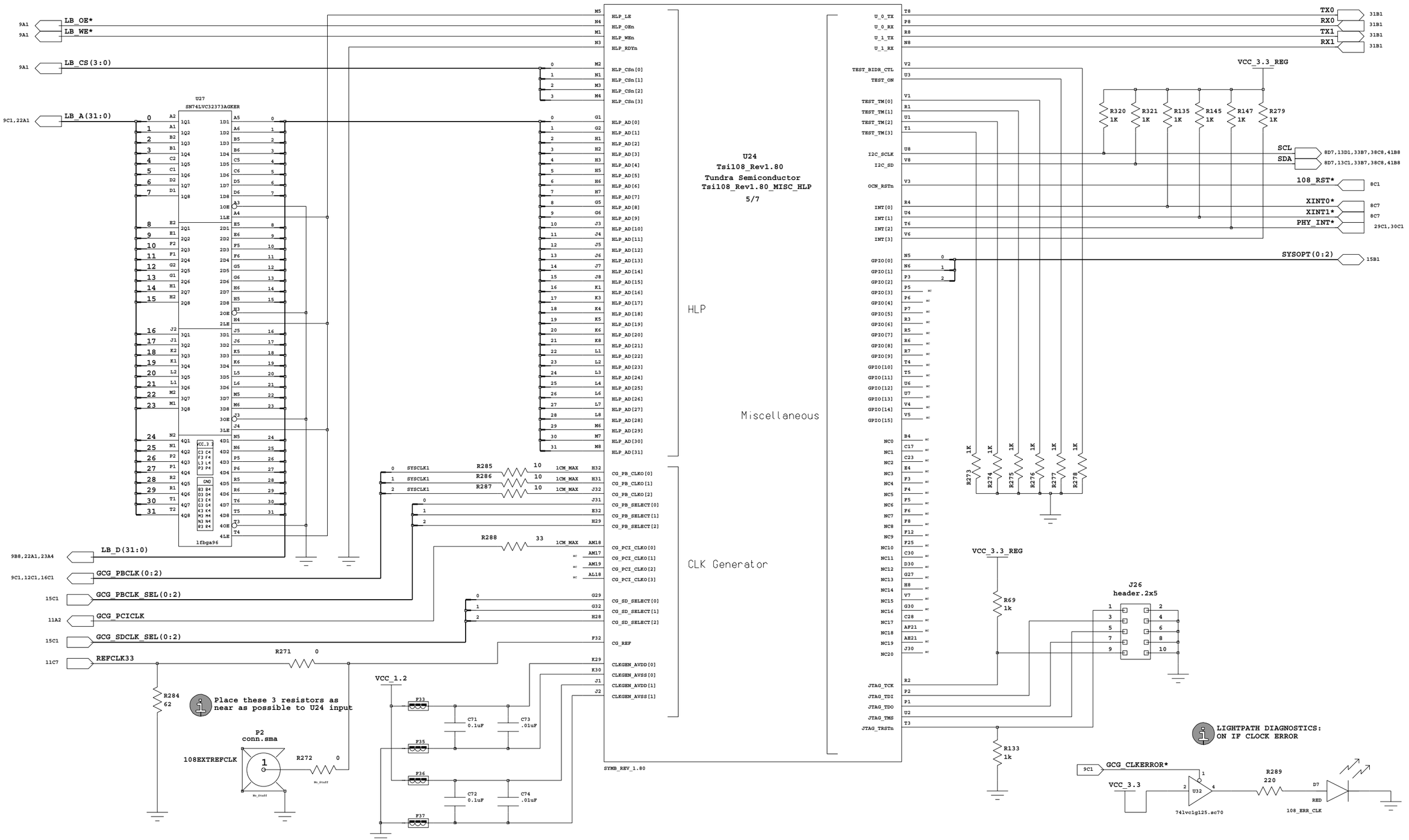
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:17:53 am	Title: TSI108 Ground		Page: 18
1	2	3	4	5	6	7	8



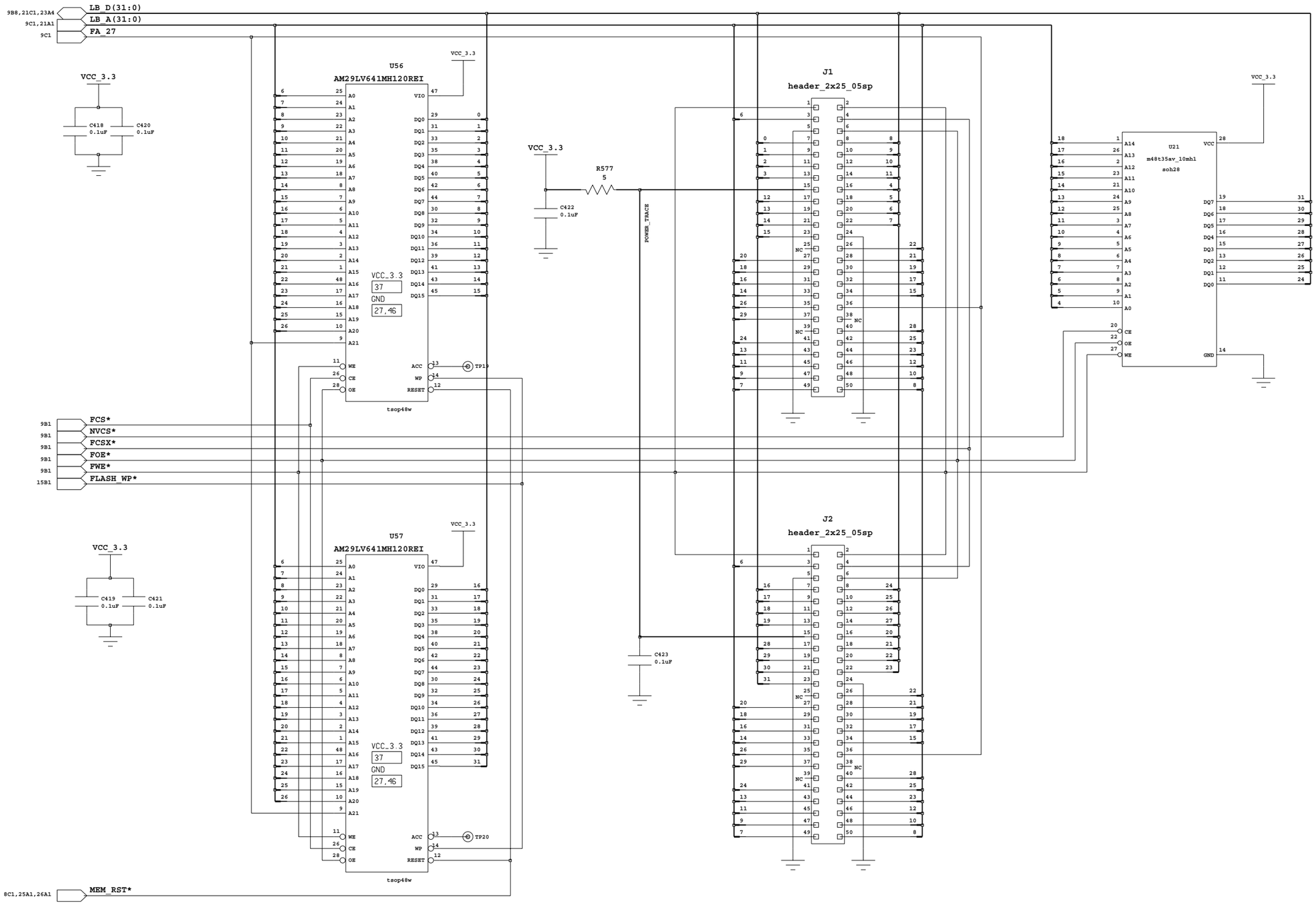
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:18:04 am	Title: TSI108 3.3V Regulator	Page: 19



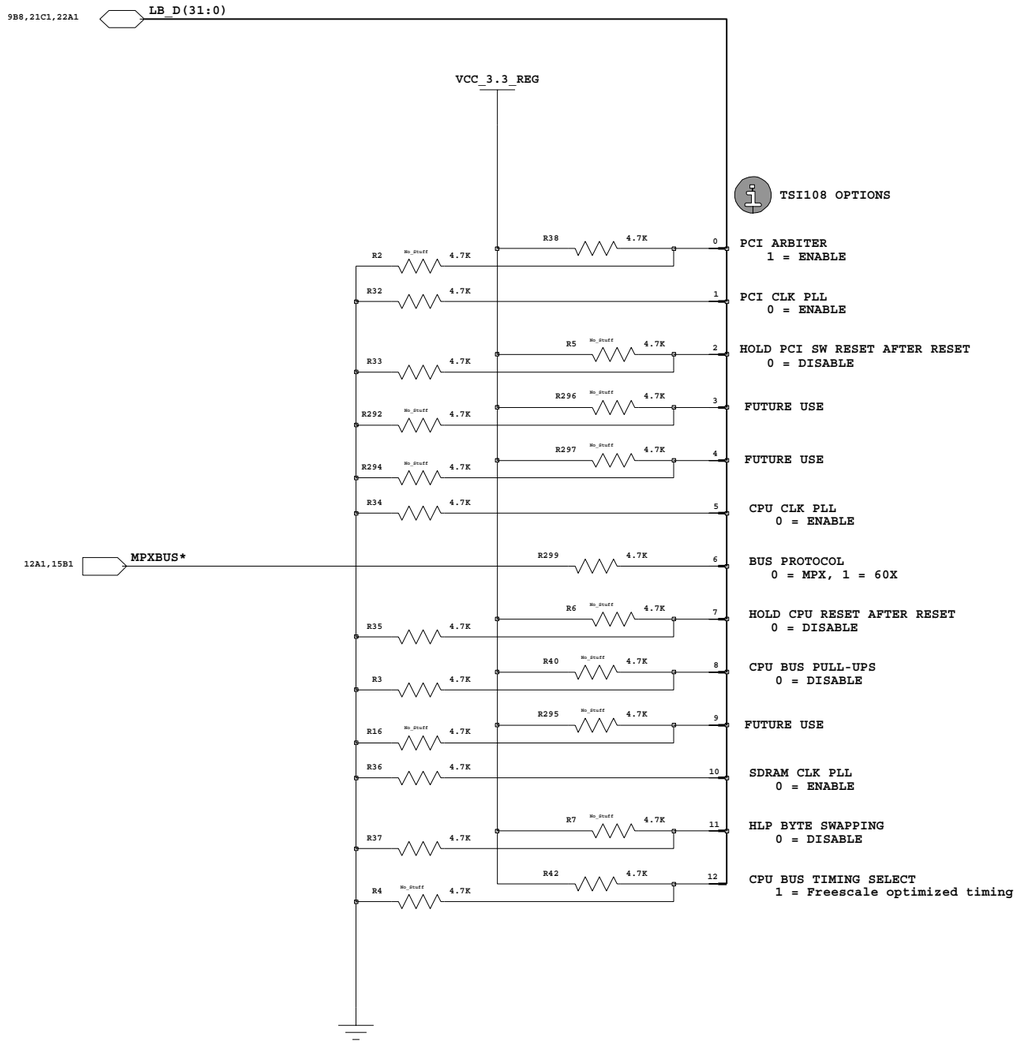
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:18:13 am	Title: TSI108 Power	Page: 20



freescale semiconductor Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:18:24 am	Title: TSI108 HLP Interface		Page: 21



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:18:35 am	Title: Flash (32-bit) and PromJet Headers	Page: 22



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:22:41 am	Title: TSI108 Configuration	Page: 23

TSI108 DDR2 feedback clock:
See board specification for
special layout requirements

P1
conn.sma
EXT_DDR2_CLK
108_EXTSDCLK
No_Stuff

VREF_DDR2

VCC_1.2
C397 0.1uF
C412 0.1uF
C69 0.1uF
C70 .01uF
F31
F32

R105 22
R106 22

MCB(7:0)
25A7,26A7

SD_CLKFBI_P
SD_CLKFBI_N
SD_SYSCLK
SD_VREF[0]
SD_VREF[1]
SD_PLL_AVDD
SD_PLL_AVSS
SD_DLL_TEST[0]
SD_DLL_TEST[1]

SD_CB[0]
SD_CB[1]
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SYMB_REV_1.80

U24
Tsi108_Rev1.80
Tundra Semiconductor
Tsi108_Rev1.80_DDR2
3/7

SD_CLKEN[0]
SD_CLKEN[1]
SD_CLKFBO_P
SD_CLKFBO_N
SD_RASn
SD_CASn
SD_WEn
SD_I2C_SD
SD_I2C_CLK
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SD_BA[1]
SD_BA[2]
SD_ODT[0]
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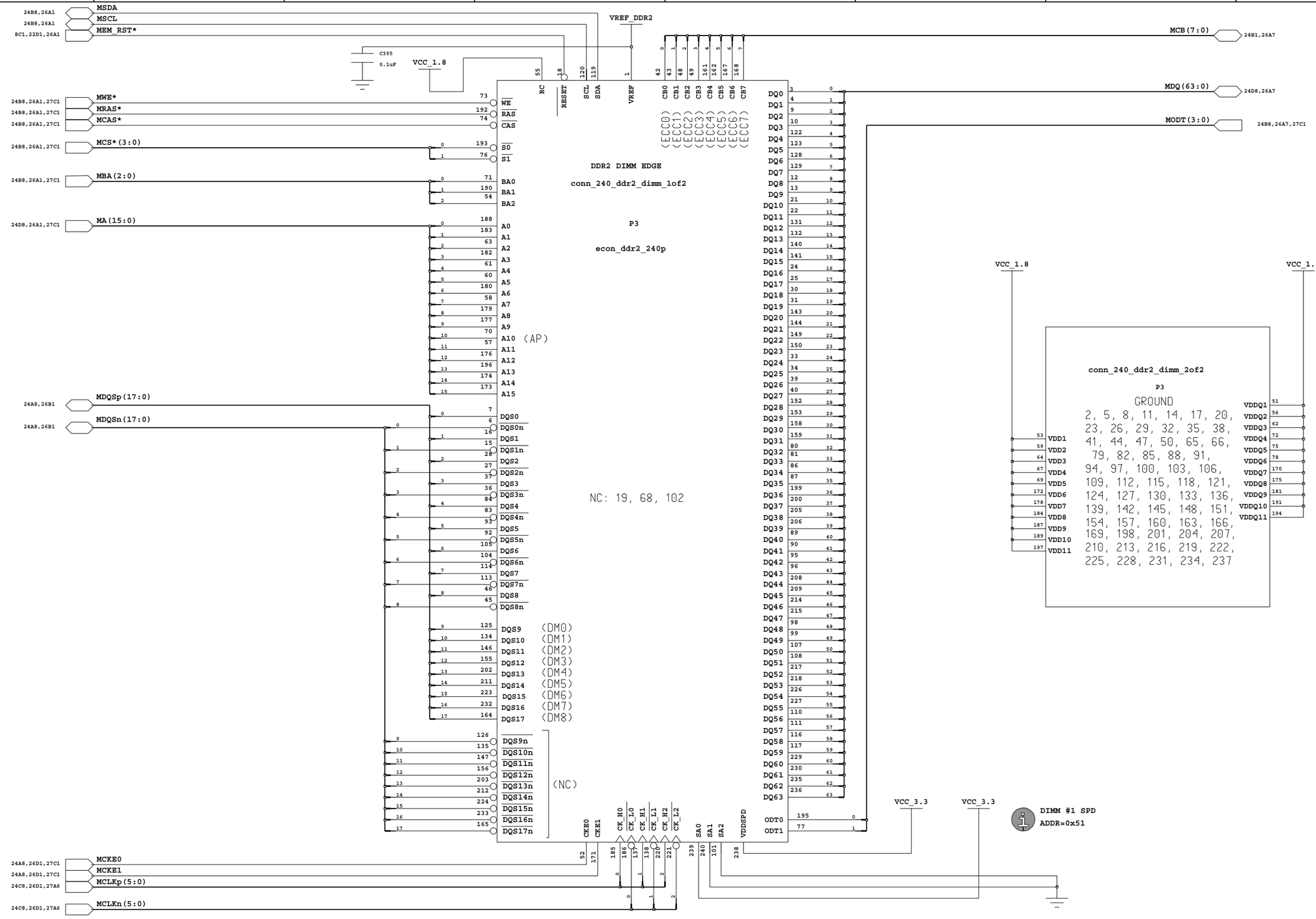
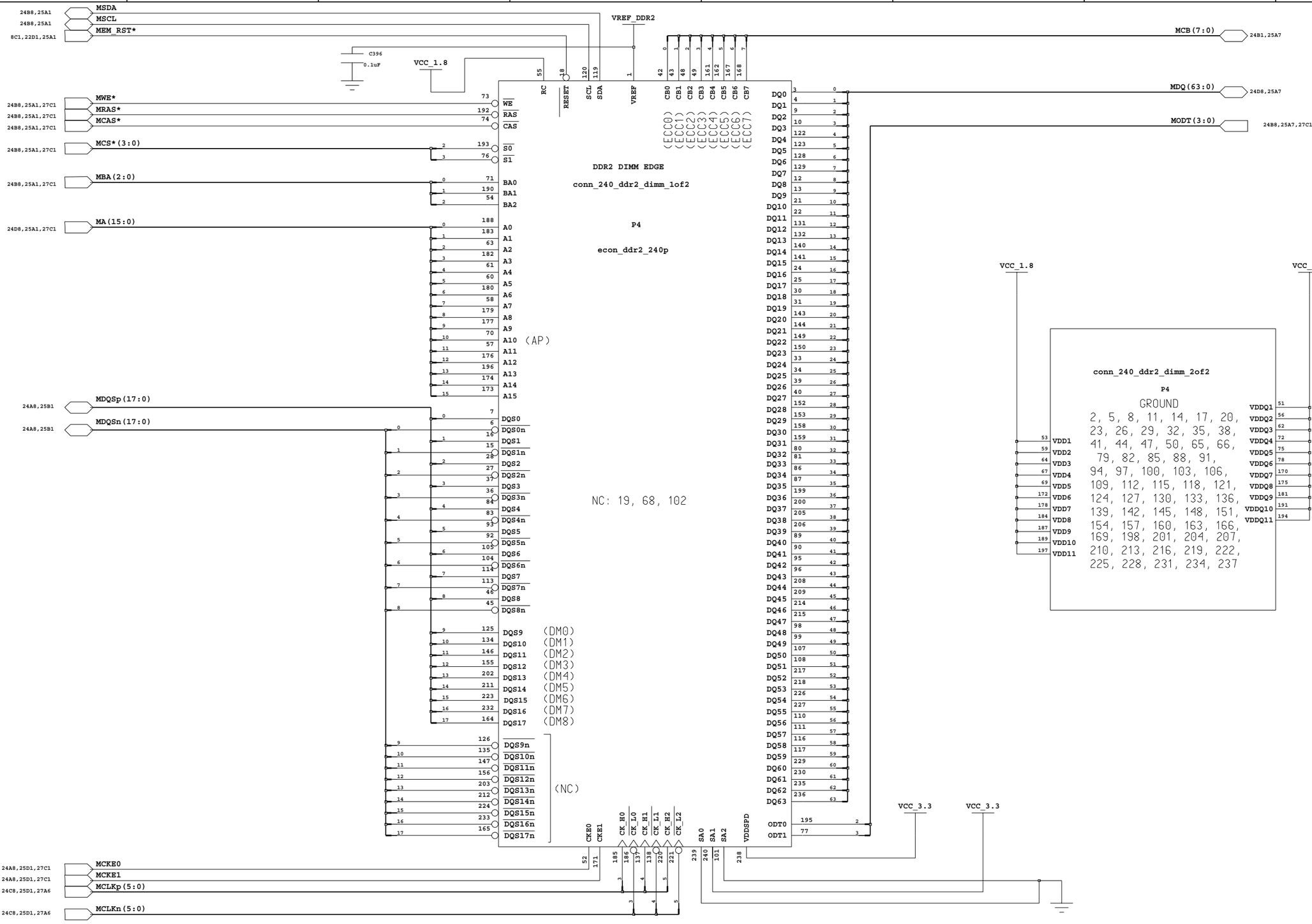
SD_A[12]
SD_A[13]
SD_A[14]
SD_A[15]

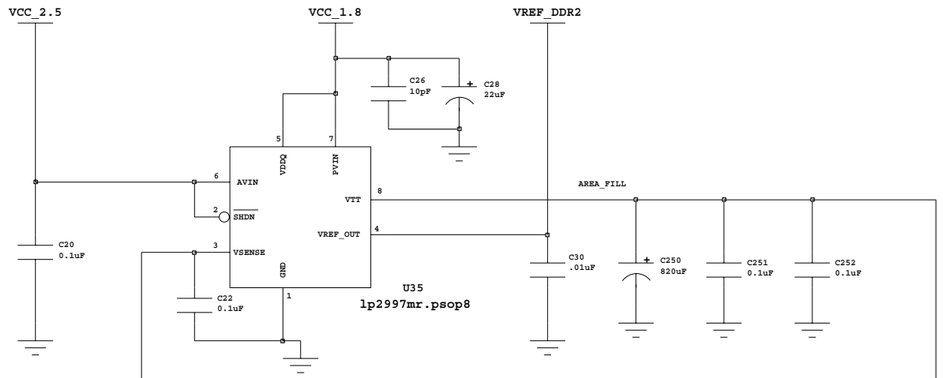
MDQSp(17:0) 25B1,26B1
MDQSn(17:0) 25B1,26B1
VCC_3.3_REG
R161 10K
R162 10K
R103 5
R104 5
MCKE0 25D1,26D1,27C1
MCKE1 25D1,26D1,27C1
MRAS* 25A1,26A1,27C1
MCAS* 25A1,26A1,27C1
MWE* 25A1,26A1,27C1
MSDA 25A1,26A1
MSCL 25A1,26A1
MBA(2:0) 25A1,26A1,27C1
R107 5
R108 5
R109 5
R110 5
MODT(3:0) 25A7,26A7,27C1
R111 5
R112 5
R113 5
R138 5
MCS*(3:0) 25A1,26A1,27C1
MCLKp(5:0) 25D1,26D1,27A6
MCLKn(5:0) 25D1,26D1,27A6
MA(15:0) 25A1,26A1,27C1
MDQ(63:0) 25A7,26A7

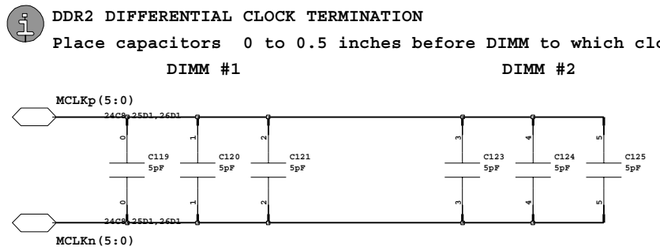


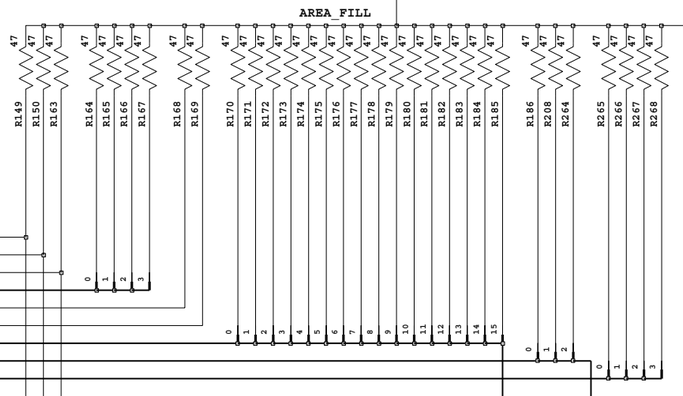
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:18:56 am Title: DDR2 DIMM #1 Page: 25

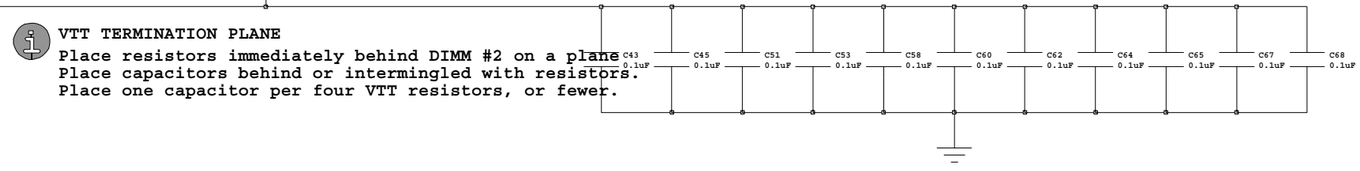


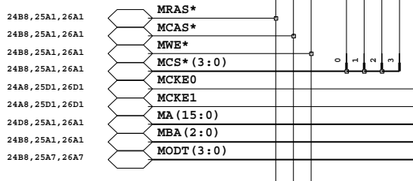
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:19:08 am	Title: DDR2 DIMM #2	Page: 26

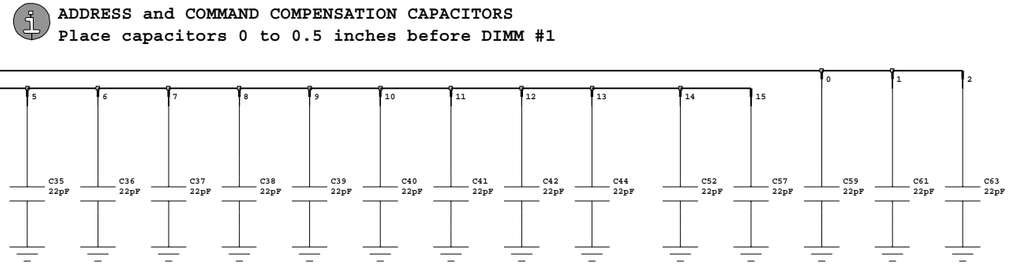




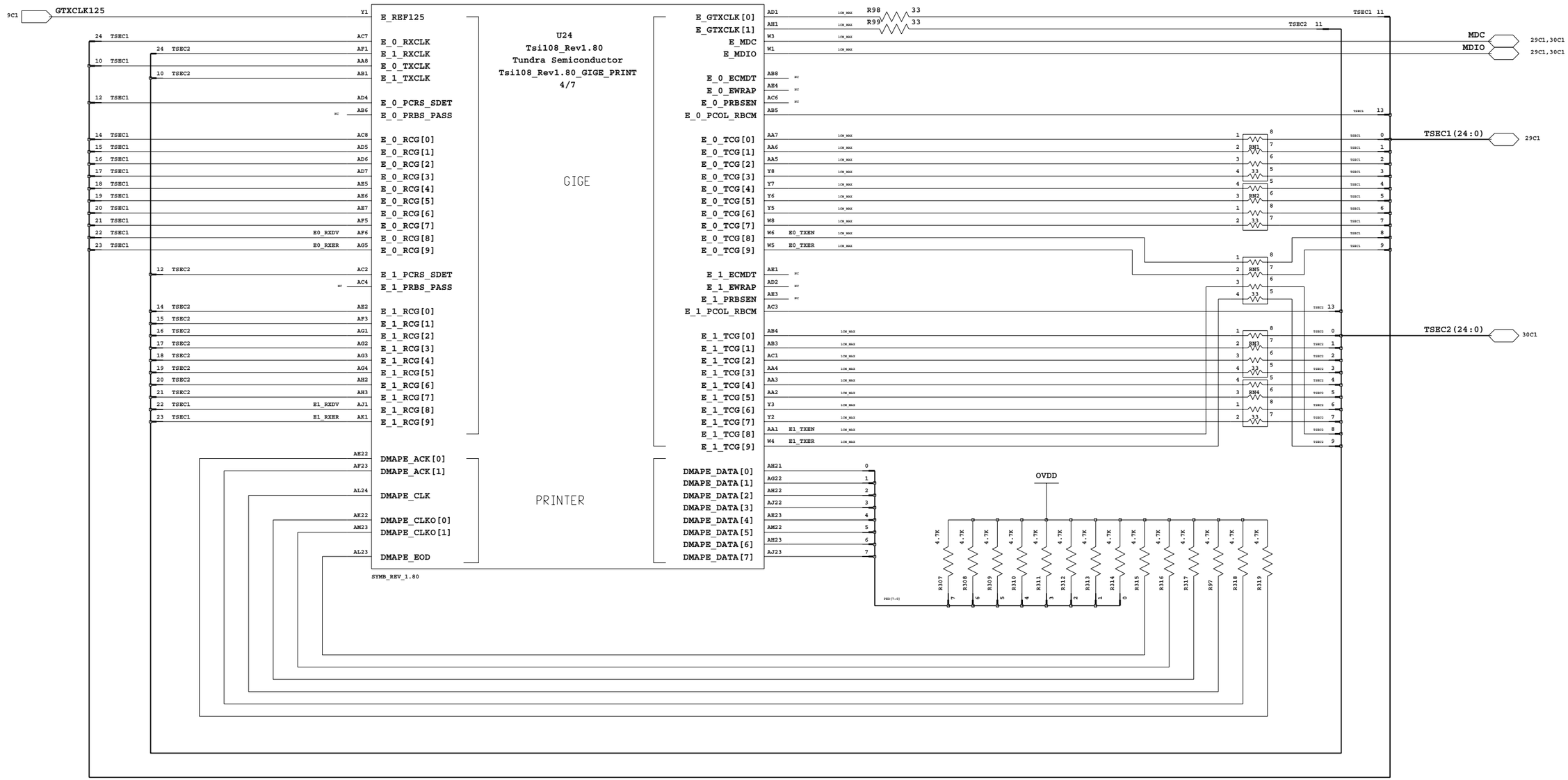




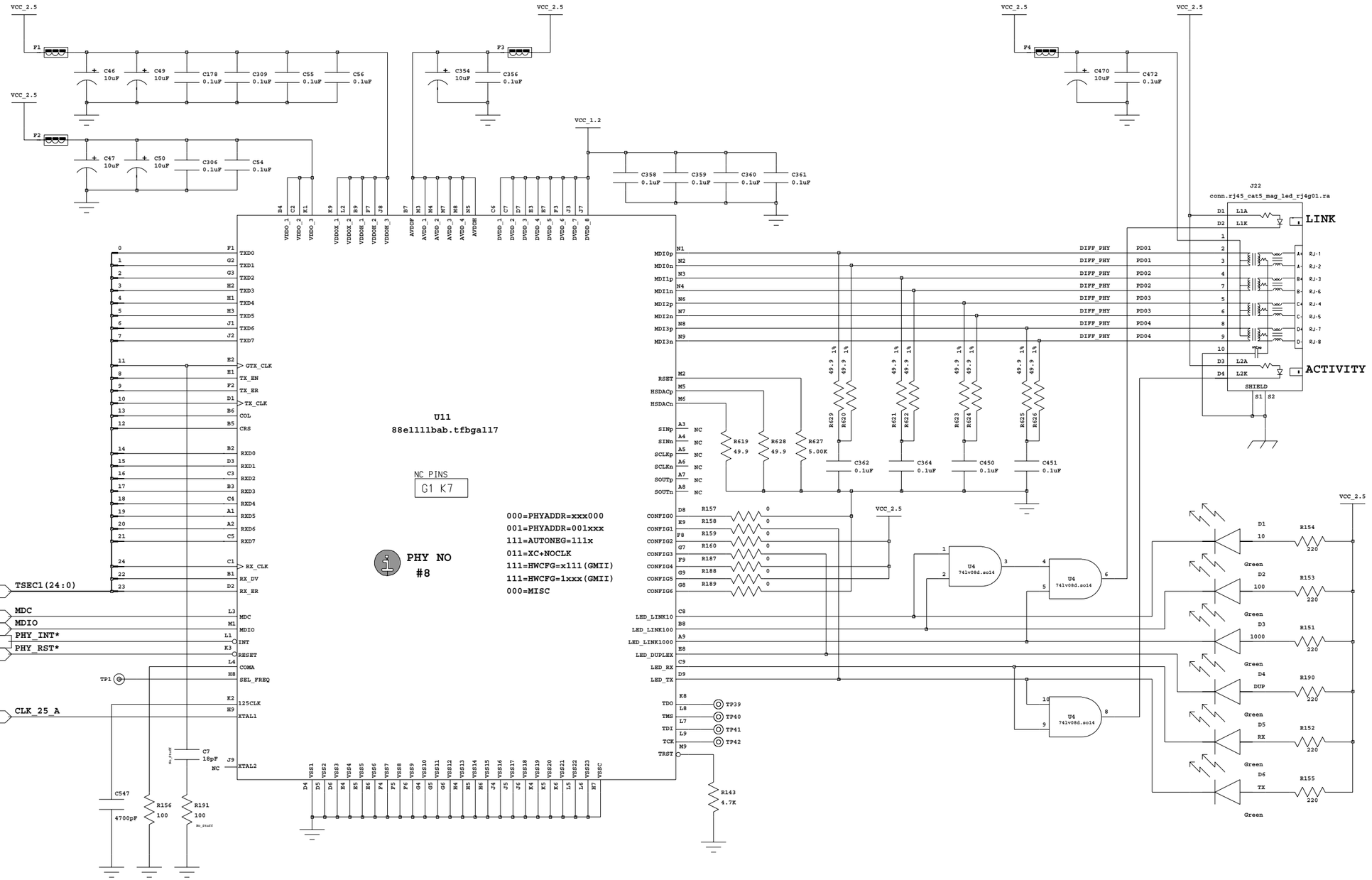




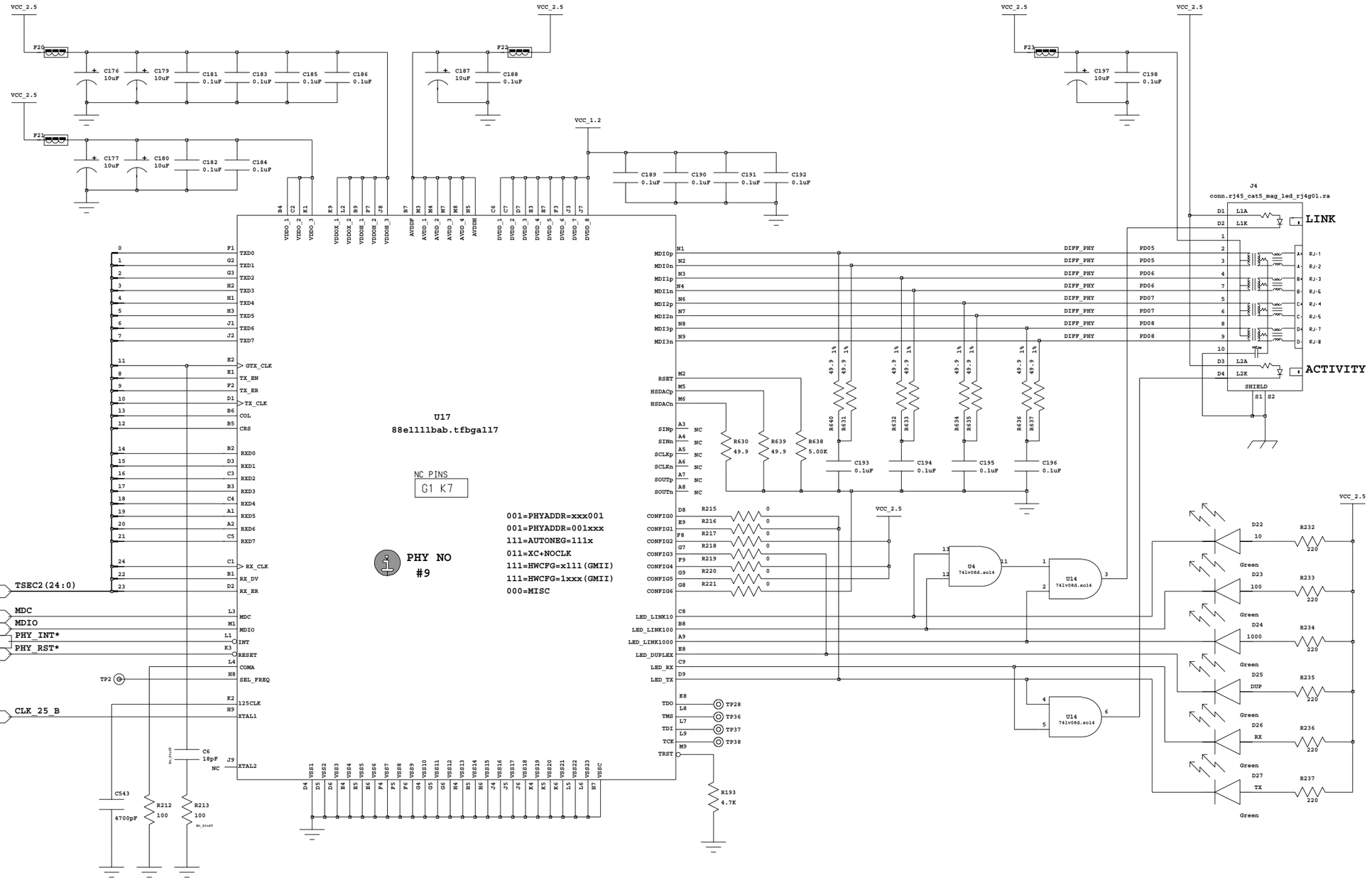
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael EVerman	Date Changed: 11/11/2005 Time Changed: 11:19:18 am	Title: DDR2 Termination and VTT/VREF Power		Page: 27



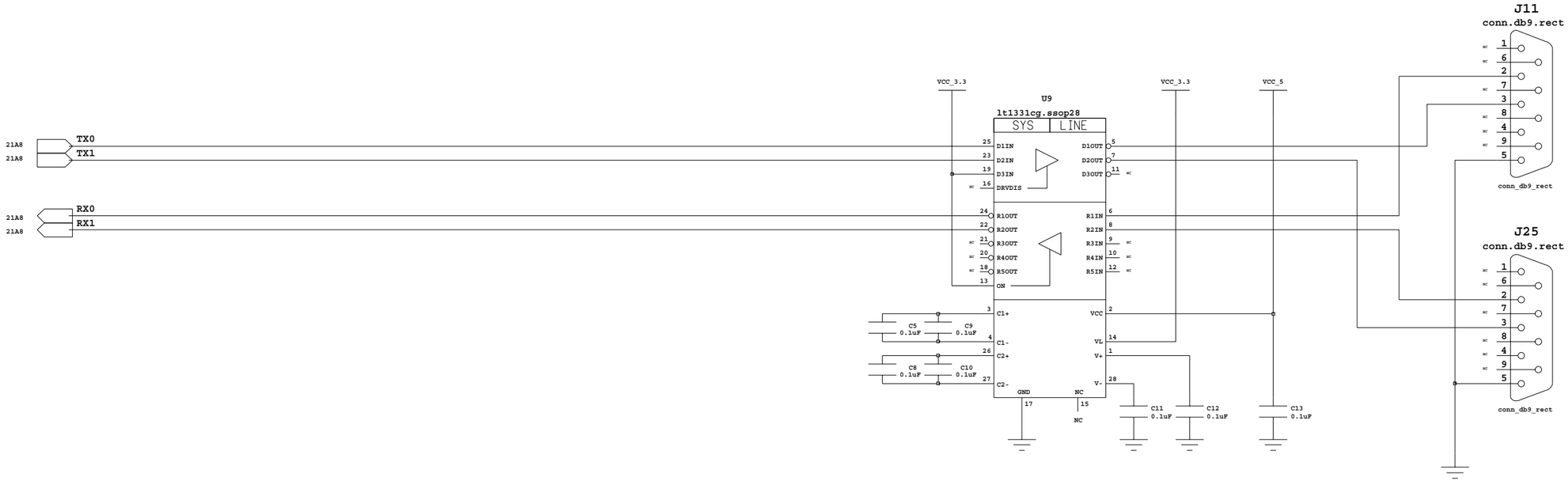
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:19:29 am	Title: TSI108 Ethernet Interface		Page: 28



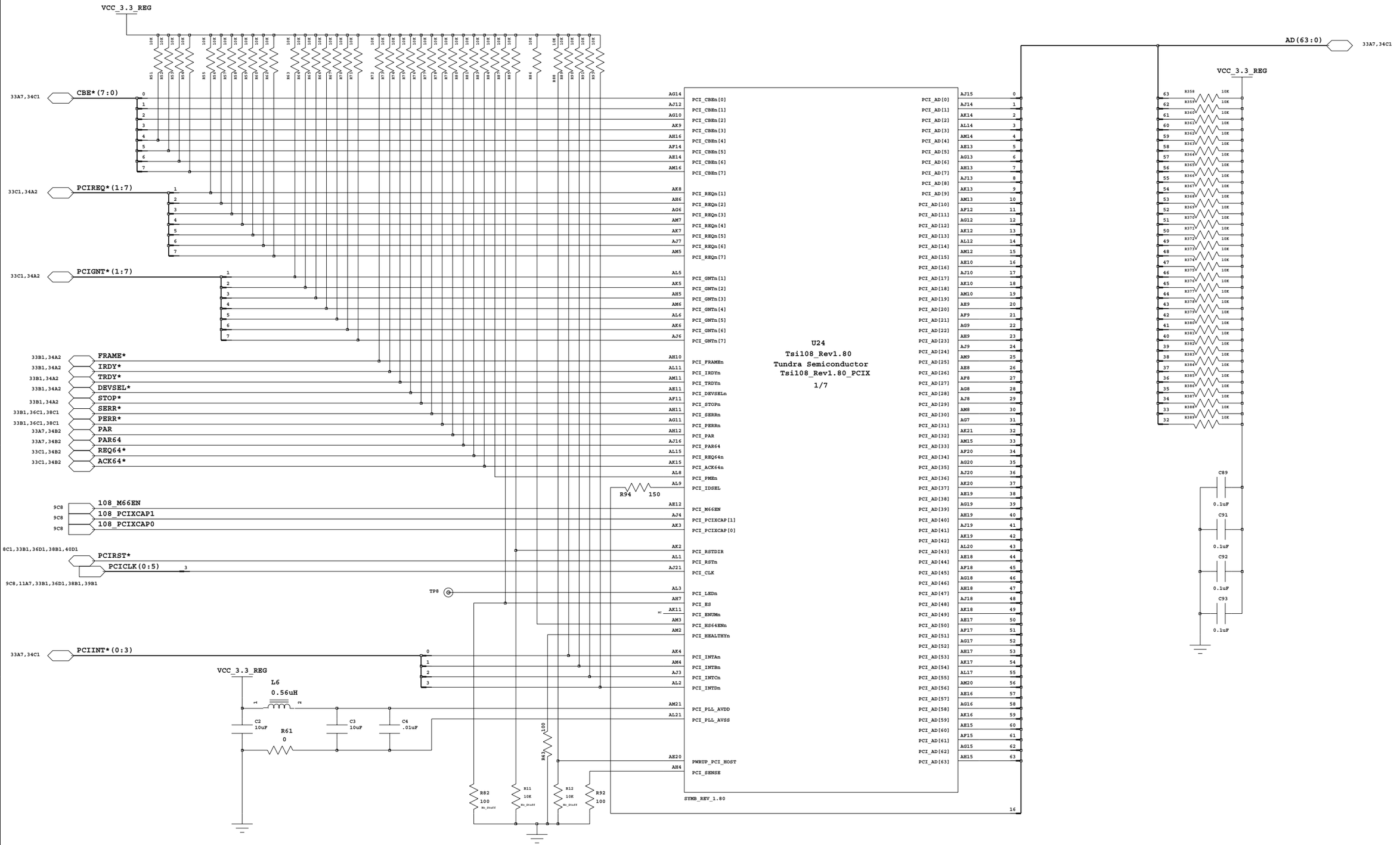
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:19:41 am	Title: Ethernet PHY #1		Page: 29



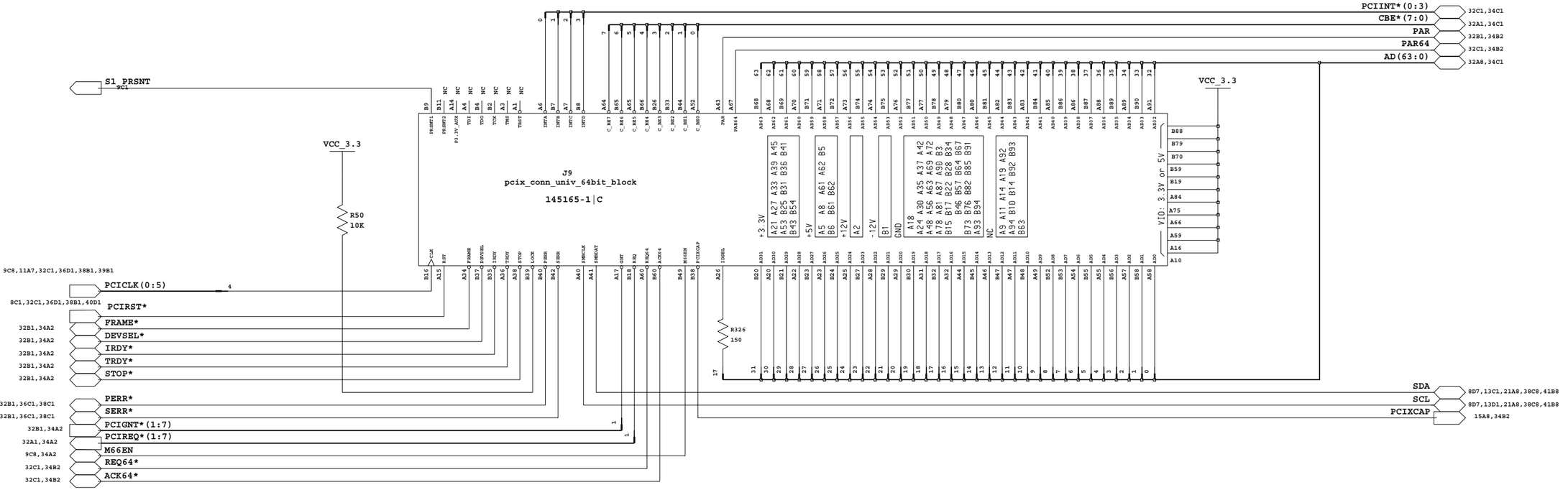
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: MIchael Everman	Date Changed: 11/11/2005 Time Changed: 11:19:52 am	Title: Ethernet PHY #2		Page: 30

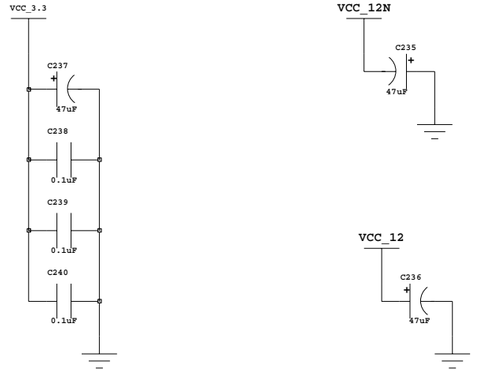


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:20:06 am	Title: Serial Ports		Page: 31

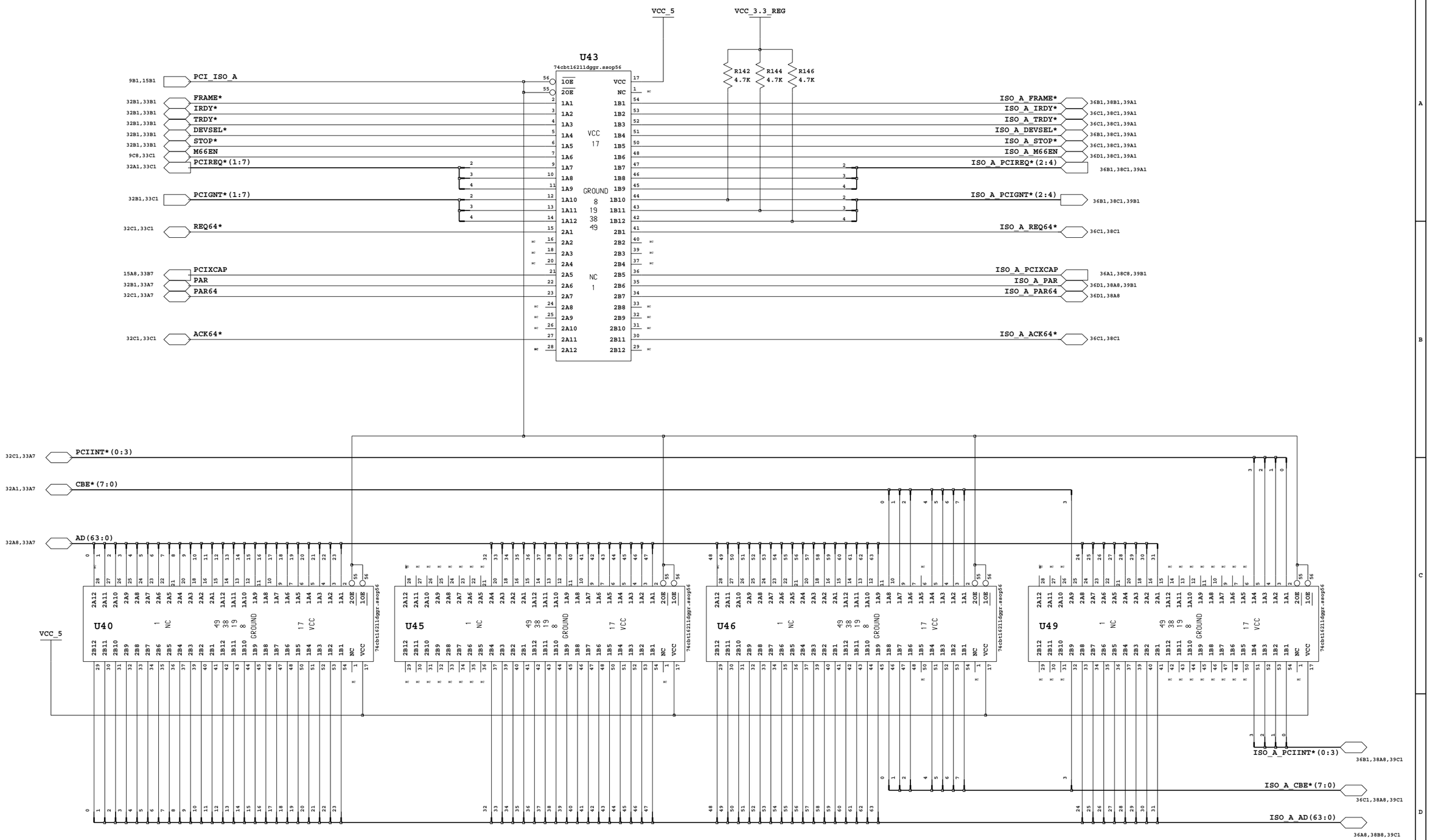


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:20:23 am	Title: TSI108 PCI / PCI-X Interface		Page: 32



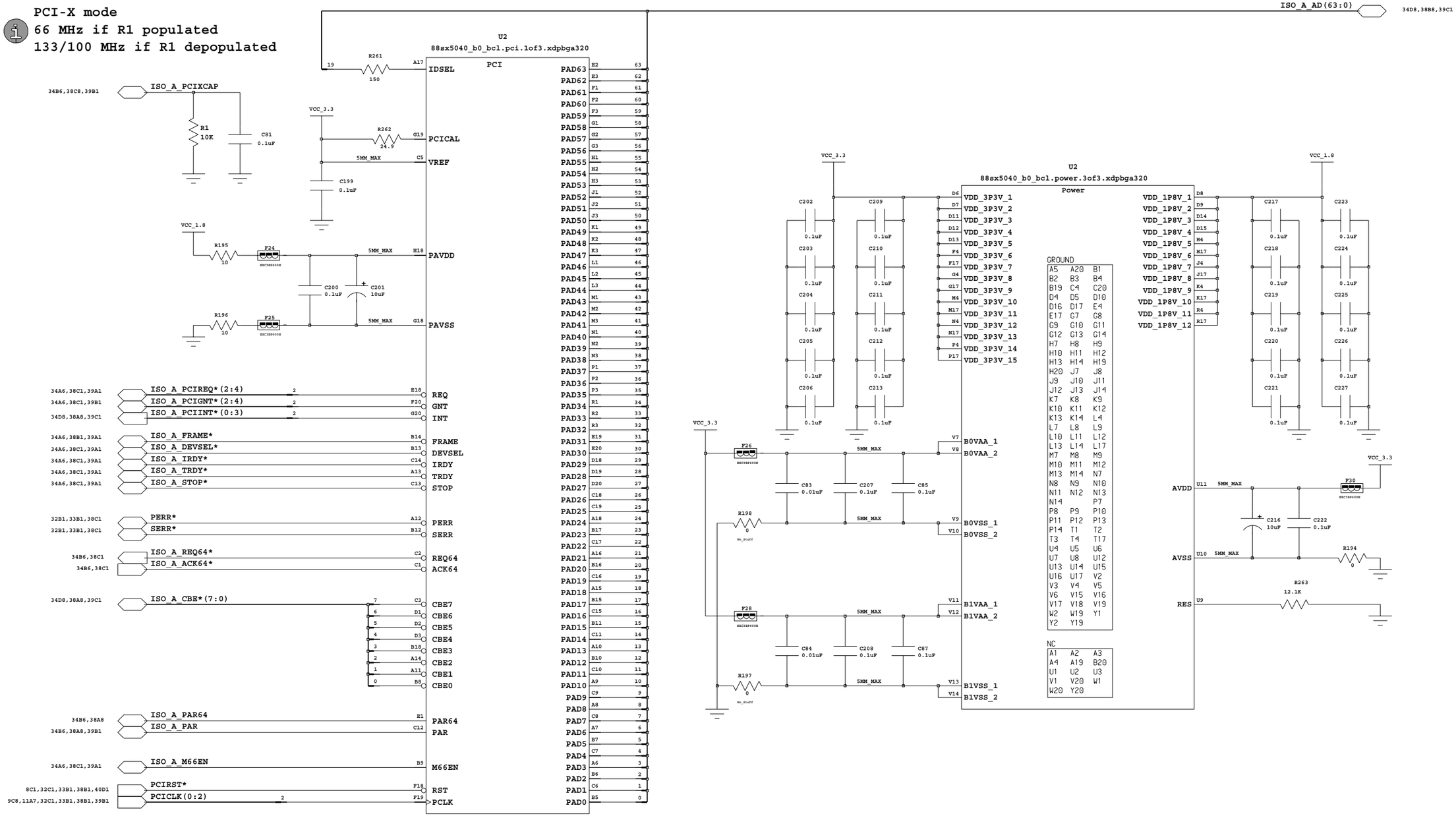


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:20:35 am	Title: PCI Bus Slot 1	Page: 33

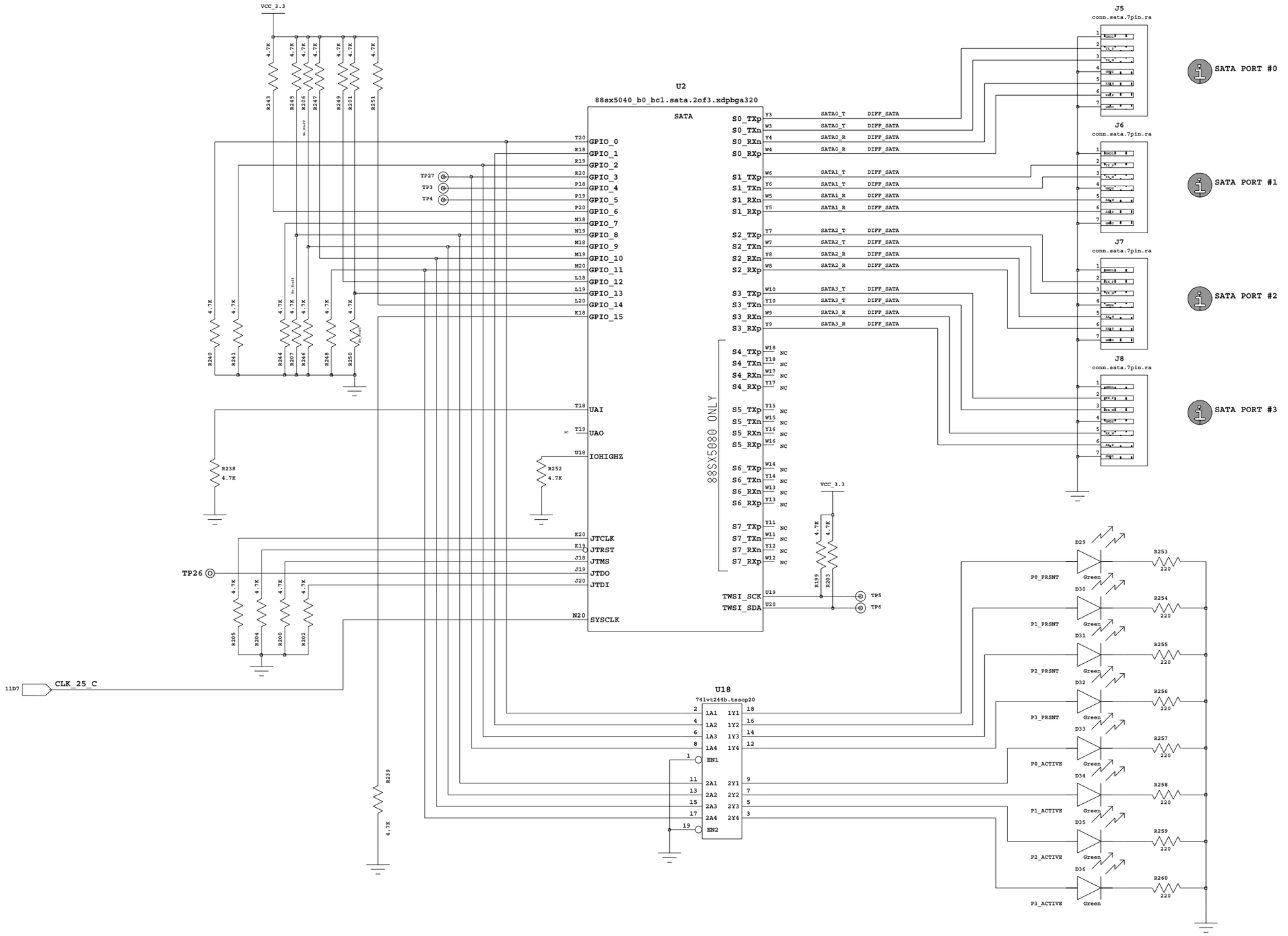


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:22:29 am	Title: PCI Bus Isolation A	Page: 34

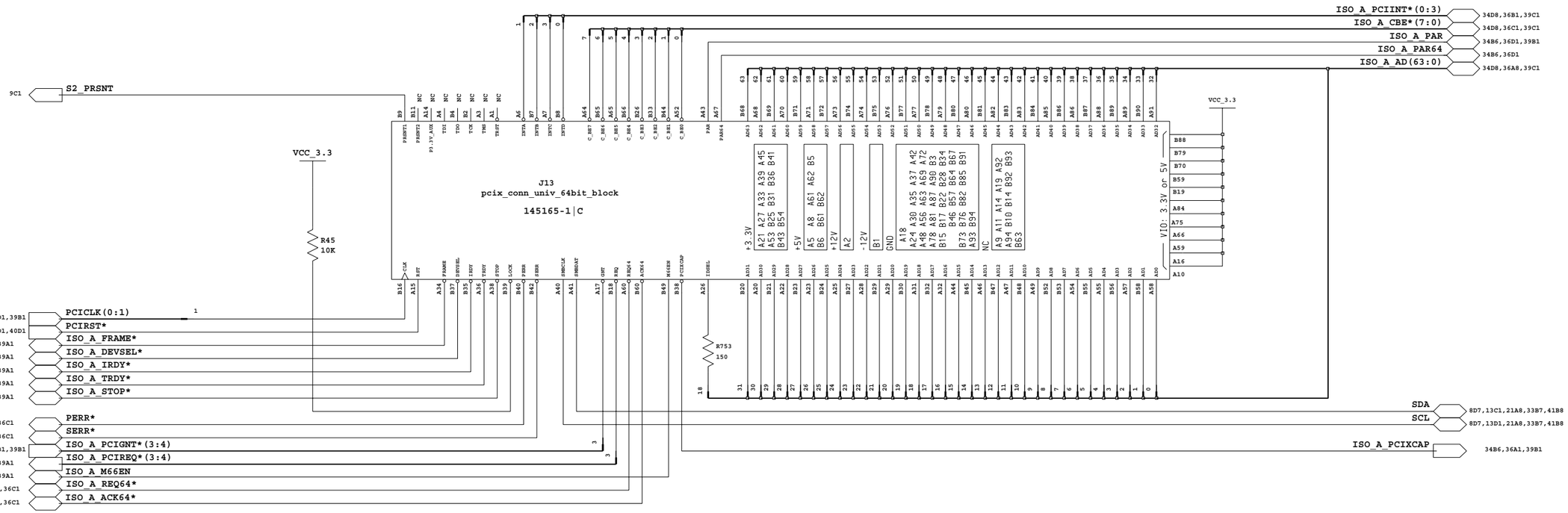
PCI-X mode
66 MHz if R1 populated
133/100 MHz if R1 depopulated

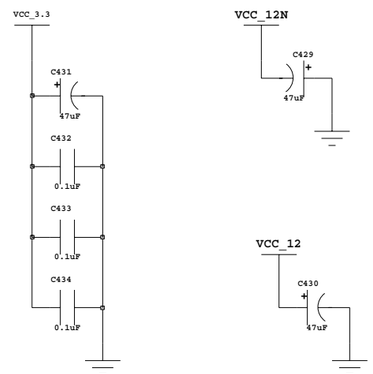


ISO_A_AD(63:0) — 34D8,38B8,39C1

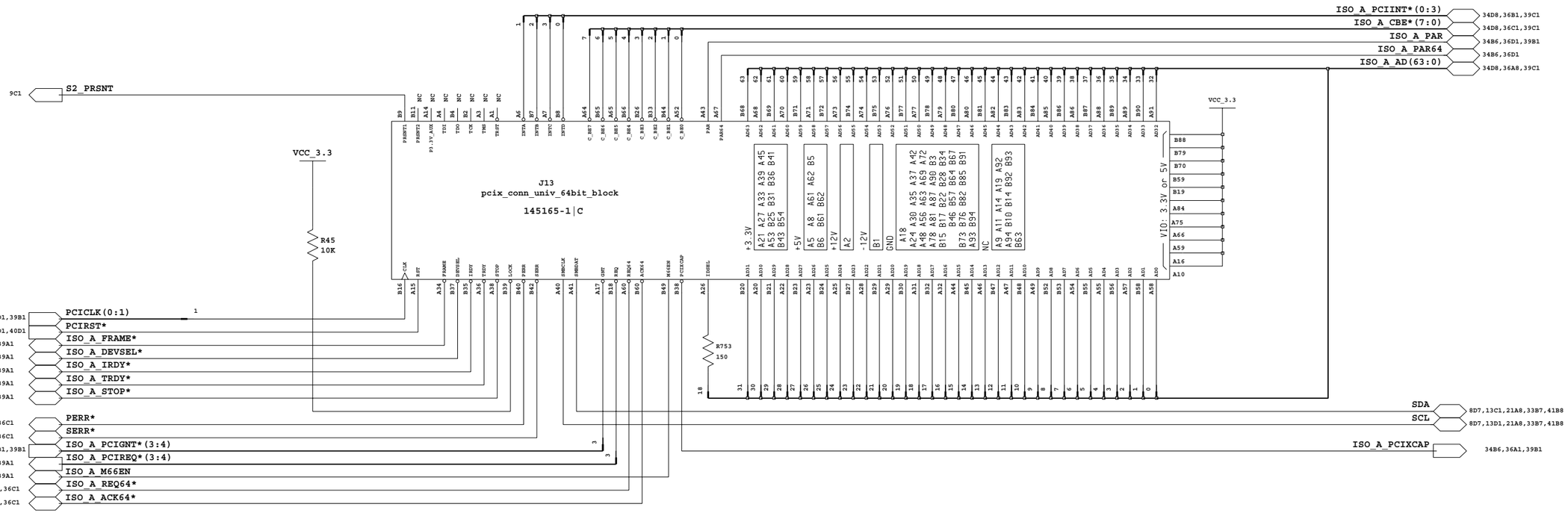


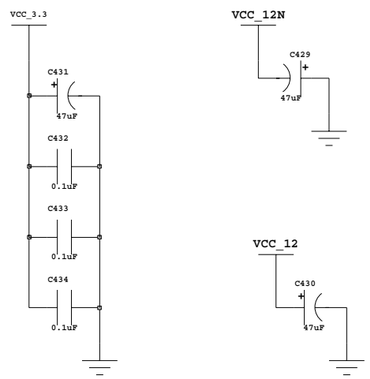
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:21:06 am	Title: Serial ATA Controller Interface	Page: 37



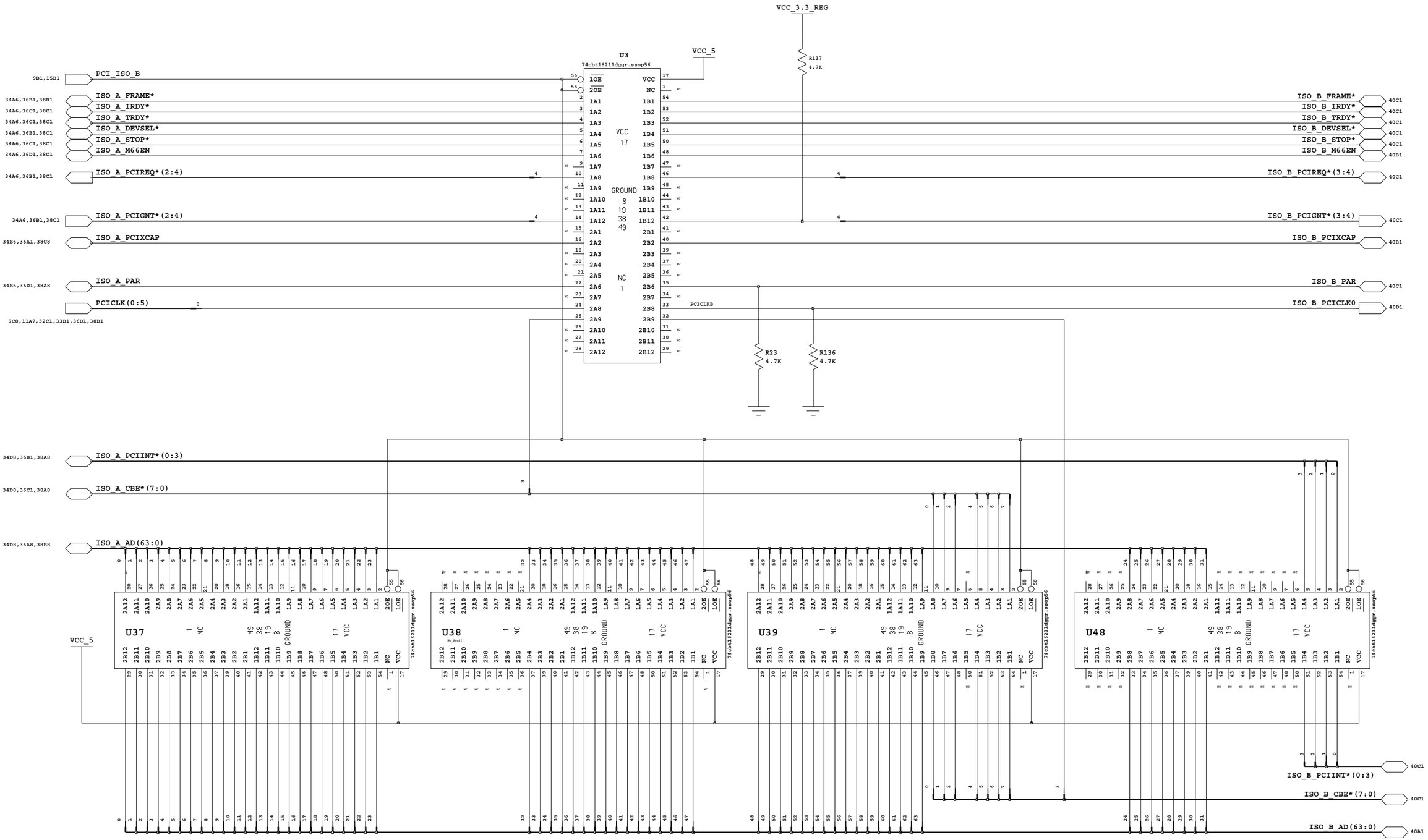


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:21:17 am	Title: PCI Bus Slot 2		Page: 38

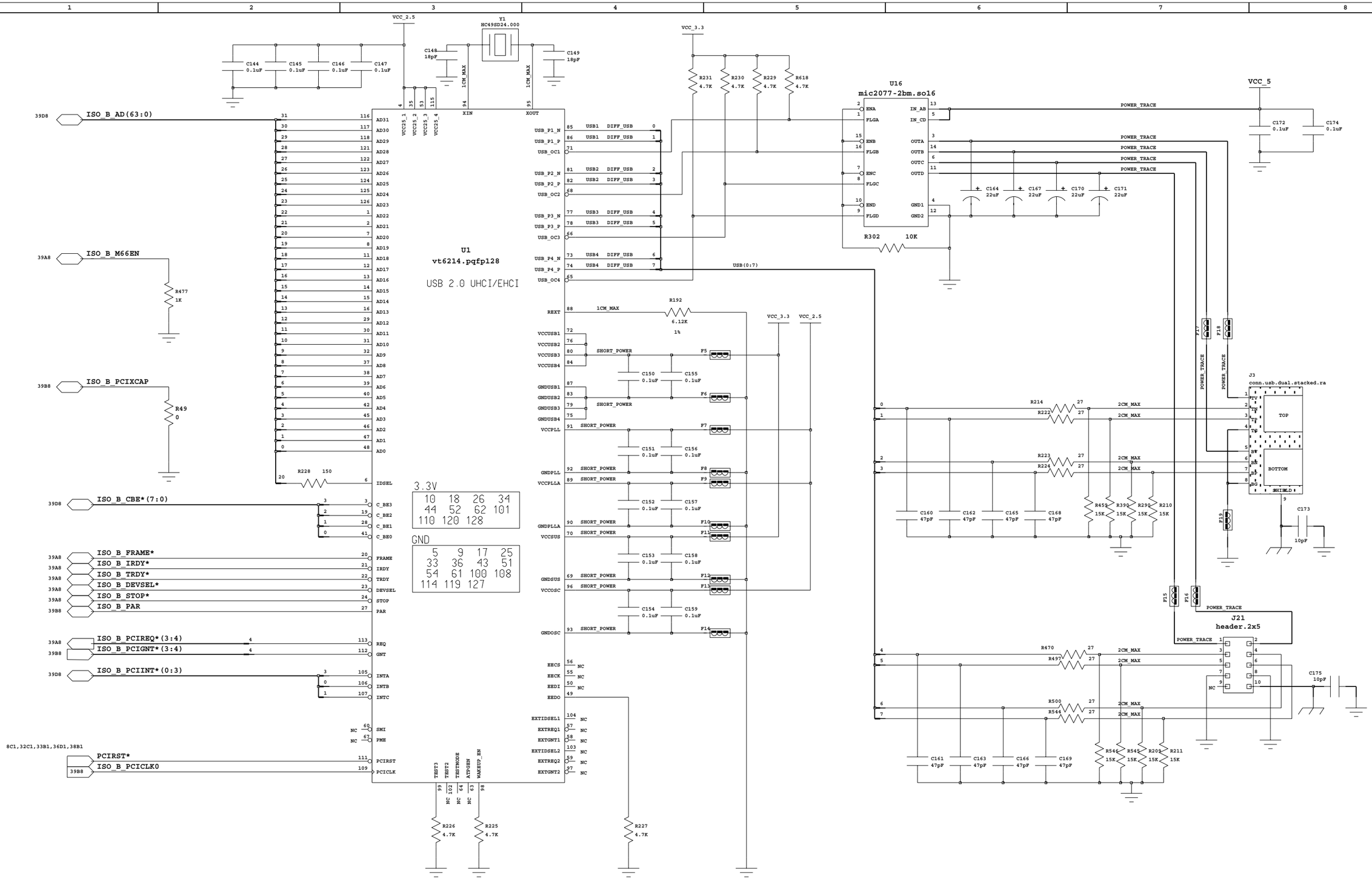




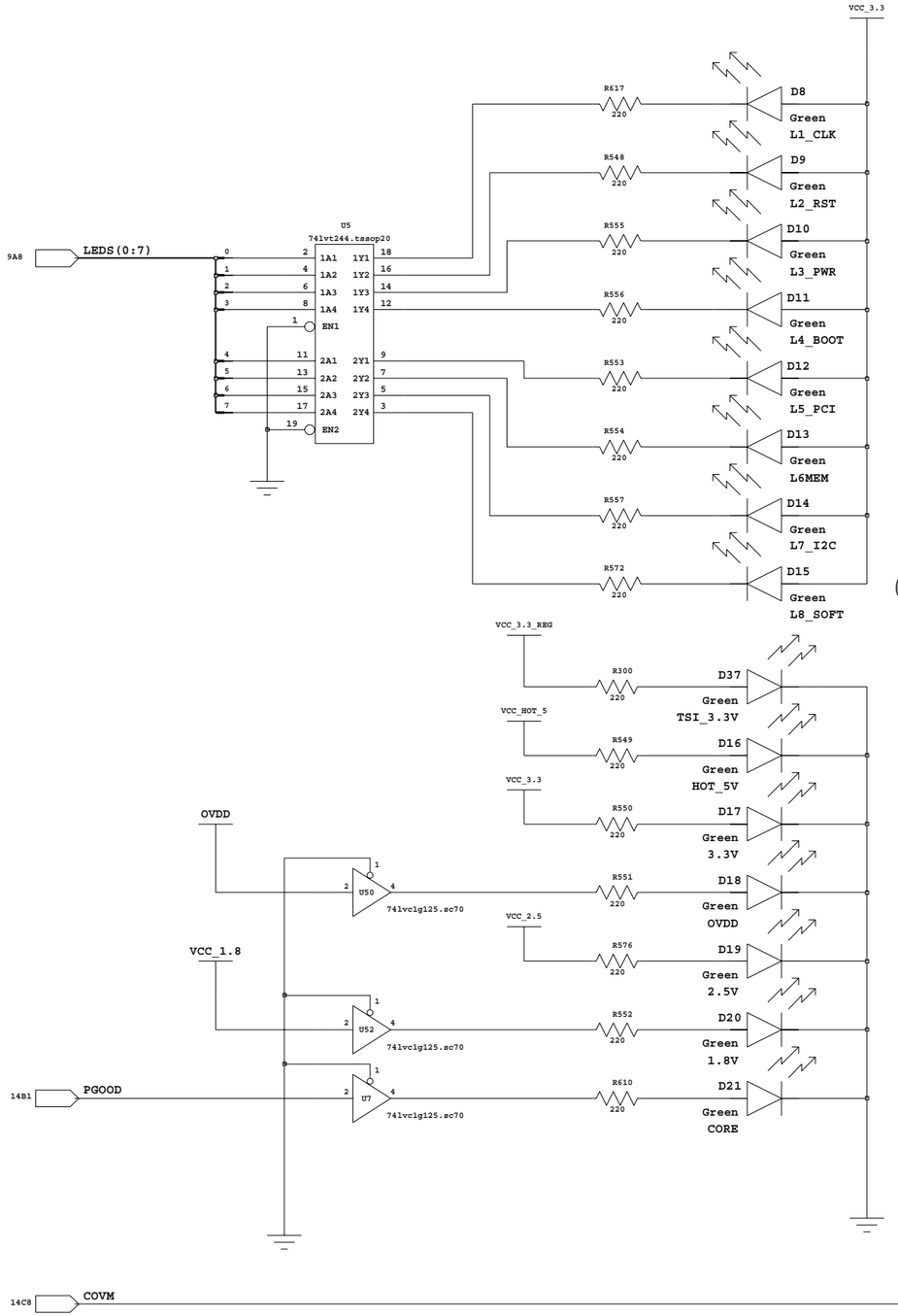
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 7/12/2005 Time Changed: 12:11:38 pm	Title: PCI Bus Slot 2		Page: 38



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:22:51 am	Title: USB Interface PCI Bus Isolation	Page: 39

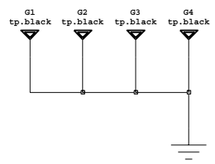


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:21:29 am	Title: USB Interface		Page: 40

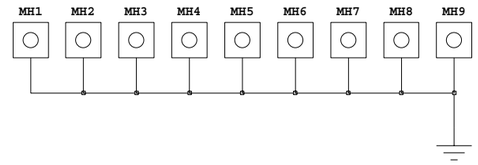


LED8 undefined; may be used by software for general purpose

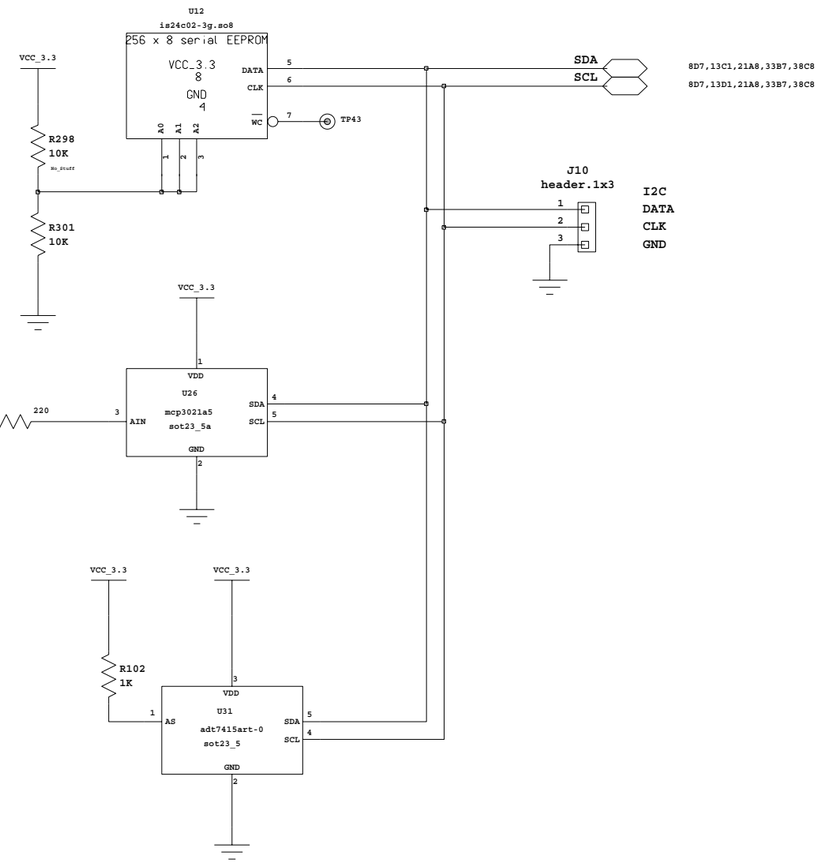
GROUND TEST POINTS
Optional



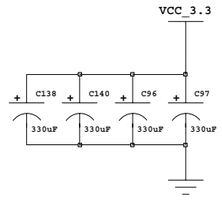
CHASSIS MOUNTING HOLES
ATX/Micro-ATX Chassis: 9 holes.



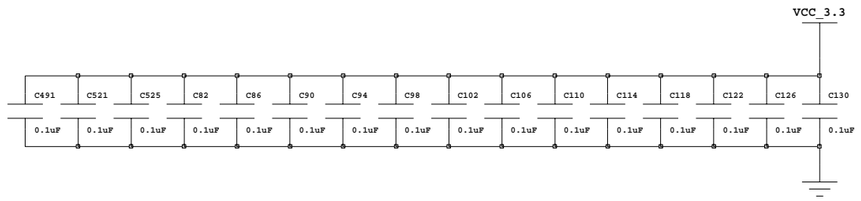
SYSTEM ID EEPROM
I2C ADDR=50 (enable 108 config) or 57 (disable 108 config ROM)



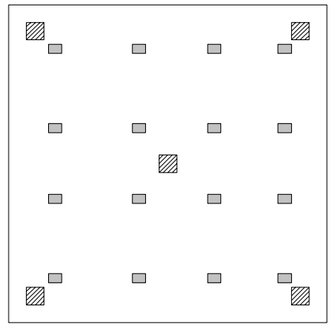
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:21:39 am	Title: Miscellaneous Functions		Page: 41



GLOBAL BULK CAPACITANCE
Place ~2cm from each corner and one in the center.



GLOBAL HF CAPACITANCE
Place in a grid ~5cm everywhere.



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Taiga Revision: 2.0	Engineer: Michael Everman	Date Changed: 11/11/2005 Time Changed: 11:21:49 am	Title: Global Bypass Capacitors		Page: 42