USB Compliance Checklist
Peripherals (Excluding Hubs)

For the 2.0 USB Specification
Checklist Version 1.09
January 16, 2012

USB Device Product Information

field	**—all fields must be filled in—**
Date	01/23/2014
Vendor Name	NXP Semiconductors
Vendor Street Address	411 E Plumeria Dr.,
Vendor City, State, Postal Code	San Jose, CA 95134
Vendor Country	USA
Vendor Phone Number	+1-408-518-5521
Vendor Contact, Title	Durgesh Pattamatta
Vendor Contact Email Address	Durgesh.pattamatta@nxp.com
Product Name	Keil MCB1800 Board
Product Model Number	MCB1850
Product Revision Level	v1.3
Test ID Number	
Captive Cable Used (Yes/No)	No
Manufacture, Model, & TID of Receptacles used	Hirose ZX62D-AB-5P8, TID 60001401
Manufacture, Model, & TID of Connectors and/or Cable Assemblies used	JEM, RD-090001, TID60001488
Manufacture & Model Identifier of the USB Silicon used in this peripheral	NXP, LPC1850 USB0
Signature of Preparer	durgesh.pattamatta@nxp.com Digitally signed by durgesh.pattamatta@nxp.com DN: cn=durgesh.pattamatta@nxp.com Date: 2014.01.23 10:32:51 -08'00'

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Revision History

version	changes	Date
1.07	Minor modifications for 2.0 spec	2001.11.28
1.07	Changes for 2.0	2001.10.5
1.06	added test ID field	1999.8.16
1.05	added D3, revised D2, D4	1999.7.15
1.04	typo fixes	1999.5.18
1.03	added D25, test description pointers	1999.4.9
1.02	revised introduction and clarified bus current draw ownership revised D11, D12, LP9, HP12, fixed μ, Ω, typos	1999.2.5
1.01	added preparer's signature and changed checklist contact info	1999.1.4
1.00	initial release: added contact info and some minor clarifications	1998.11.20
.95	first public review draft, released for Taipei USB Plugfest	1998.10.26

1 Introduction

This checklist helps designers of USB peripherals to assess their products' compliance with the Universal Serial Bus Specification, Revision 2.0. Unless explicitly stated otherwise, all references to the USB Specification refer to Revision 2.0.

This checklist is also used, in part, to qualify a USB peripheral for the USB-IF Integrators List. This document and other USB compliance tools, including USB Check, are available in the developers section of the USB-IF's website, http://www.usb.org/developers/. The compliance checklists are updated periodically, so developers should check for updates when starting new projects.

Section 5, Recommended Questions, contains questions covering areas not required by the USB Specification. Answering these questions is not a requirement for compliance with the Specification or acceptance to the Integrators List. However, vendors are strongly encouraged to take these questions into consideration when designing their products.

Questions or comments regarding the Integrators List, Compliance Workshop testing results, or checklist submissions should be sent to admin@usb.org. If you have questions regarding the checklist itself, feel it fails to adequately cover an aspect of the USB specification, have found an error, or would like to propose a question, please contact the USB-IF at checklists@usb.org.

1.1 General Notes

- All voltages are referenced to the device's USB ground.

2 Mechanical Design and Layout

ID	question
M1	What is the manufacture and model identifier of the connectors or cables used with this peripheral? Manufacturer: Hirose Model: ZX62D-AB-5P8 .
M2	What is the manufacture and model identifier of the USB silicon used in this peripheral? Manufacturer: NXP Semiconductors Model: LPC1850 If the silicon used in this peripheral is **NOT** listed on the USB Integrators List attach a Peripheral Silicon checklist covering this peripheral's USB silicon.

Device vendors are strongly encouraged to review the Connector and Cable Assembly and Peripheral Silicon checklists regardless of whether or not their device's cabling, connectors, and silicon appear on the Integrators List.

ID	question	response	sections in spec

M3	Can the device's data lines withstand voltages between –1.0 and 4.6V applied with a source impedance of 39Ω ±2% for up to 100ns?	yes ☑ no ☐	7.1.1
M4	When tri-stated, can either data line be continuously shorted to V_{BUS}, GND, the other data line, or the connector's shield without damage occurring?	yes ☑ no ☐	7.1.1
M5	When driving 50% of the time, can either data line be shorted to V_{BUS}, GND, the other data line, or the connector's shield without damage occurring?	yes ☑ no ☐	7.1.1
M6	Do the D+ and D- traces present a characteristic impedance of 45Ω ±15% to GND and a differential impedance of 90Ω ±15%, between the device's cable connection and termination resistors?	yes ☑ no ☐	7.1.6
M7	If edge rate control capacitors are used: Are they located between the transciever pins and the device's termination resistors? Is their capacitance less than 75pF and balanced within 10%?	 yes ☐ no ☐ yes ☐ no ☐	7.1.6
M8	Are the device's receivers and transmitters within 1ns of its cable connection?	yes ☑ no ☐	7.1.16
M9	Does the device present sufficient capacitance between V_{BUS} and GND to prevent adverse effects from flyback voltages when its cable is disconnected? (A minimum of 1.0µF is recommended.)	yes ☑ no ☐	7.2.4.2
M10	Are you using the USB pins on any of the USB connectors on your device for any other purposes except for USB?	yes ☐ no ☑	

2.1 Low-Speed Devices

(not applicable to full-speed devices)

MLS1	Does the device have a captive cable?	yes ☐ no ☐	7.1.1.2
MLS2	Does the device pull up D-?	yes ☐ no ☐	7.1.5
MLS3	Does the device, with its captive cable, present a single-ended capacitance between 200 and 450pF on the D+ and D- lines?	yes ☐ no ☐	7.1.1.2
MLS4	Is the device's signaling rate 1.50Mb/s ±1.5%, even if the device uses spread spectrum clocking?	yes ☐ no ☐	7.1.11

2.2 Full-Speed Devices

(not applicable to low-speed devices)

MFS1	Does the device's source impedance remain in the shaded areas of Figure 7-4?	yes ☑ no ☐	7.1.1.1
MFS2	Does the device pull up D+?	yes ☑ no ☐	7.1.5
MFS3	Is the device's signaling rate 12.000Mb/s ±.25%, even if the device uses spread spectrum clocking?	yes ☑ no ☐	7.1.11

2.3 Tethered Devices

(not applicable to untethered devices)

Tethered devices are devices with a captive cable.

MT1	Does the captive cable have a series A plug?	yes ☐ no ☐	6.2
MT2	Does the device pull up the appropriate data line with a 1.5kΩ ±5% resistor attached to a voltage source between 3.0 and 3.6V or with a Thevénin	yes ☐ no ☐	7.1.5

	source of at least 900Ω?		

2.4 Untethered Devices

(not applicable to tethered devices)

Untethered devices are devices with a detachable cable.

MUT1	Does the device have a series B receptacle?	yes ☑ no☐	6.2
MUT2	Does the device pull up D+ with a 1.5kΩ ±5% resistor attached to a voltage source between 3.0 and 3.6V?	yes ✔ no ☐	7.1.5
MUT3	Does the device's upstream port present 100pF or less on D+ and D-?	yes ☑ no☐	7.1.6

3 Device States and Signals

D1	Can the device pull up the appropriate data line to at least 2.0V within 2.5µs?	yes ✔ no ☐	7.1.5
D2	Is the device's pullup active only when V_{BUS} is high?	yes ☑ no☐	7.1.5
D3	Is the V_{BUS} switching threshold for the device's pullup control between 1.0V and 4.0V?	yes ✔ no ☐	7.1.5
D4	If the device is bus powered, or uses bus power to run any of its components, does it pull up the appropriate data line within 100ms of V_{BUS} exceeding 4.01V?	yes ✔ no ☐	7.1.5
D5	Does the device meet all power-on and connection timing requirements, as illustrated in Figure 7-29?	yes ✔ no ☐	7.1.7.3 7.3.2
D6	Does the device respond to a reset no sooner than 2.5µs and no later than 10ms after the SE0 begins?	yes ✔ no ☐	7.1.7.5
D7	Is the device's reset recovery time less than 10ms?	yes ☑ no☐	7.1.7.5
D8	At the end of reset is the device in the default state?	yes ☑ no☐	7.1.7.3 9.1.1
D9	Can the device correctly handle more than one USB RESET with no intervening packets?	yes ✔ no ☐	7.1.7.3
D10	Does the device begin the transition to its suspend state after its bus segment has been idle for 3ms, regardless of the device's state?	yes ✔ no ☐	7.1.7.4
D11	Has the device's power consumption dropped to its suspended value after the hub's upstream bus segment has been idle for 10ms?	yes ✔ no ☐	7.1.7.4
D12	When suspended, does the device recognize any non-idle state on the bus, excluding a reset, as a resume signal?	yes ✔ no ☐	7.1.7.5
D13	When suspended, does the device recognize a reset and act on the signal so that it enters the default state?	yes ✔ no ☐	7.1.7.5 7.1.7.3 9.1
D14	Does the device recognize a K→low-speed EOP→J transition on its upstream port as the end of resume signaling?	yes ✔ no ☐	7.1.7.7
D15	Is the device able to accept a SetAddress() request 10ms after resume is signaled?	yes ✔ no ☐	7.1.7.5
D16	Does the device complete its wakeup within 20ms?	yes ☑ no☐	7.1.7.5
D17	Can the device function correctly with frame lengths between 995 and 1005µs?	yes ✔ no ☐	7.1.12
D18	Does the device function correctly on tier 6, when subjected to worst-case	yes ☑ no☐	7.1.14

	hub bit skews and delay times?		7.1.19
D19	Does the device drive no signals upstream on power up?	yes ☑ no ☐	7.2.1
D20	Does the combination of the device's pullup and the 15kΩ ±5% pulldown resistor at the upstream port yield a voltage between 2.7 and 3.6V when the bus is idle?	yes ✔ no ☐	7.3.2
D21	Does the device complete SetAddress() or a standard request with no data in less than 50ms?	yes ✔ no ☐	7.3.2 9.2.6.3
D22	Does the device deliver the first and all subsequent data packets, except for the last data packet, for a standard request within 500ms?	yes ✔ no ☐	7.3.2 9.2.6.4
D23	Does the device deliver the last data packet for a standard request within 50ms?	yes ✔ no ☐	7.3.2 9.2.6.4
D24	Does the device pass a full Chapter 9 test, as performed by USB Check?	yes ✔ no ☐	Chapters 8 and 9
D25	Does the device implement a default control endpoint 0 for all addresses?	yes ☑ no ☐	9.1.1.4
D26	Are the device's differential *and* single-ended USB signals within spec? Note: This test is especially important if ferrite beads or a common mode choke is used on the USB data lines, as these components often pose a significant signal integrity hazard.	yes ✔ no ☐	7.1.6

Device vendors are strongly encouraged to complete all bus transactions as quickly as is practical. See section 9.2.6.1 for details.

For details on testing USB signals, consult the USB-IF's signal quality test description, which can be downloaded from the USB-IF Compliance Program webpage.

3.1 Low-Speed Devices

(not applicable to full-speed devices)

LS1	Does a low-speed device implement the default control pipe and, at most, two interrupt endpoints?	yes ☐ no ☐	5.3.1.1
LS2	Does the device allow an interpacket delay of at least two low-speed bit times?	yes ☐ no ☐	7.1.18
LS3	Is the device's transaction timeout 16–18 low-speed bit times?	yes ☐ no ☐	7.1.19
LS4	Does the device recognize keep alive strobes and remain awake?	yes ☐ no ☐	11.8.4.1

3.2 Full-Speed Devices

(not applicable to low-speed devices)

FS1	Does the device allow an interpacket delay of at least two full-speed bit times?	yes ✔ no ☐	7.1.18
FS2	Is the device's transaction timeout 16–18 full-speed bit times?	yes ☑ no ☐	7.1.19
FS3	Does the device ignore low-speed packets?	yes ☑ no ☐	8.6.5

3.3 Remote Wakeup

(not applicable to devices which do not support remote wakeup)

W1	Does the device wait at least 5.0ms after its bus segment enters the idle state before sending a remote wakeup?	yes ☐ no ☐	7.1.7.5
W2	Does the device signal remote wakeup by driving K upstream for at least 1ms, but not more than 15m?	yes ☐ no ☐	7.1.7.5

W3	After driving K, does the device immediately tri-state its buffers without driving the bus to any non-K state?	yes ☐ no ☐	7.1.7.5
W4	Does the device send remote wakeups only when configured to do so?	yes ☐ no ☐	9.6.2

4 Operating Voltages and Power Consumption

P1	Does the device source no current to V_{BUS} under any circumstance?	yes ☑ no ☐	7.2.1

4.1 Bus Power Consumption

(applicable to **all** devices, **including self powered devices**)

Note: the current allotted for a device consuming bus power encompasses all current drawn from V_{BUS}, including the power required to drive the device's upstream USB port. For details on testing USB device current consumption, please consult the USB-IF current test description, which can be downloaded from the USB-IF Compliance Program webpage.

4.1.1 Low-Power and Self Powered Devices

(not applicable to high power devices)

LP1	Is the MaxPower field in the device's configuration descriptor 100mA or less?	yes ☑ no ☐	7.2.1.3 9.6.2
LP2	Can the device operate in all states with a steady-state V_{BUS} of 4.35–5.25V?	yes ☑ no ☐	7.2.2
LP3	Can the device operate in all states with a transient V_{BUS} as low as 4.02V?	yes ☑ no ☐	7.2.2
LP4	Does the device draw the amount of current specified in its MaxPower field or less at all times, provided its V_{BUS} is between 4.02 and 5.25V?	yes ☑ no ☐	7.2.1.3
LP5	When the device is suspended, is its average current draw less than 500µA?	yes ☑ no ☐	7.2.3
LP6	If the device's current draw spikes during suspend, is the maximum spike height less than 100mA and is the spike's edge rate less than 100mA/µs for V_{BUS} between 4.02 and 5.25V?	yes ☑ no ☐	7.2.3
LP7	When the device wakes up from suspend, does it limit any inrush currents to 100mA or less?	yes ☑ no ☐	7.2.3
LP8	Does the device limit its inrush current, either by using capacitors smaller than 10µF or by using soft-start circuits, such that no more than 10µF of capacitance is charged by currents higher than 100mA when the device is hot plugged?	yes ☑ no ☐	7.2.4.1 7.2.3
LP9	Does the device draw no inrush current at configuration or when it transitions to its operating mode?	yes ☑ no ☐	7.2.4.1

4.1.2 High Power Devices

(not applicable to low-power and self powered devices)

HP1	Is the MaxPower field in the device's configuration descriptor 500mA or less?	yes ☐ no ☐	7.2.2
HP2	Can the device operate in its unconfigured state with a steady-state V_{BUS} of 4.35–5.25V?	yes ☐ no ☐	7.2.2

HP3	Can the device operate in its unconfigured state with a transient V_{BUS} as low as 4.02V?	yes ☐ no ☐	7.2.2
HP4	While unconfigured, does the device draw 100mA or less at all times, provided its V_{BUS} is between 4.02 and 5.25V?	yes ☐ no ☐	7.2.1.3
HP5	Can the device operate in its configured state with a steady-state V_{BUS} of 4.50–5.25V?	yes ☐ no ☐	7.2.2
HP6	Can the device operate in its configured state with a transient V_{BUS} as low as 4.17V?	yes ☐ no ☐	7.2.2
HP7	While configured, does the device draw the amount of current specified in its MaxPower field or less at all times, provided its V_{BUS} is between 4.02 and 5.25V?	yes ☐ no ☐	7.2.1.3
HP8	If the device does not support remote wakeup, the device is not configured, or remote wakeup is disabled, is the device's average suspend current draw less than 500µA?	yes ☐ no ☐	7.2.3
HP9	If the device supports remote wakeup, remote wakeup is enabled, and the device is configured, is the device's average suspend current draw less than 2.5mA?	yes ☐ no ☐	7.2.3
HP10	If the device's current draw spikes during suspend, is the maximum spike height less than 500mA and the spike's leading edge rate less than 100mA/µs for V_{BUS} between 4.02 and 5.25V?	yes ☐ no ☐	7.2.3
HP11	When the device wakes up from suspend, does it limit any inrush currents to 500mA or less?	yes ☐ no ☐	7.2.3
HP12	Does the device limit its inrush current, either by using capacitors smaller than 10µF or by using soft-start circuits, such that no more than 10µF of capacitance is charged: By currents higher than 100mA when the device is hot plugged? By currents higher than the device's MaxPower at configuration or when the device transitions to its operating mode?	 yes ☐ no ☐ yes ☐ no ☐	7.2.4.1 7.2.3

5 Recommended Questions

R1	Are the device's signal swings matched as closely as possible?	yes ☑ no ☐	7.1.2
R2	If ferrite beads are used in the device's USB connection, are they present on only the V_{BUS} and GND lines?	yes ☐ no ☐	7.1.6
R3	Does the device complete all commands as quickly as is practical?	yes ☑ no ☐	9.2.6.1
R4	If the device is self-powered and does not operate any of its components from bus power, does it only signal an attach when both bus power and external power are available?	yes ✔ no ☐	

6 Explanations

This section should be used to explain any “no” answers or clarify answers on checklist items above. Please key entries to the appropriate checklist question.