Freescale Semiconductor
White Paper

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i.MX31 and i.MX31L Power Management

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1 Executive Brief

Microprocessors have long been classified, rated, differentiated and marketed on their clock speed, measured in kilohertz, megahertz, and now even gigahertz. When processors were still fairly simple machines, this measure was sufficient. In today's mobile global society, using the clock speed as a measurement is inadequate and outdated. Current microprocessors designed with the clock speed accelerated consume power rapidly, compromising battery life. The complexity of today's microprocessor architectures mandates a new metric.

Freescale's engineers believe the capabilities of processor architectures, not the speed of their clocks, is the key to increased functionality and the performance mobile device manufacturers and consumers demand. So, from the transistor level to memory accesses, and from software builds to power saving modes, innovative thinking and engineering at Freescale Semiconductor has resulted in the i.MX family of applications processors with Smart Speed Technology. The i.MX processors enable wireless mobile devices to deliver

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longer performance times with plenty of energy available to drive power-hungry applications, such as video conferencing and 3-D gaming.

The primary target of the i.MX31 and i.MX31L processors is the mobile device market; thus, a lot of thought and effort has been invested to optimize performance and provide longer performance time for mobile systems based on the i.MX31 and i.MX31L. In this white paper, we describe some non-application-specific techniques and mechanisms deployed in these processors that significantly prolong the battery life of the device.

Here is a brief look at the i.MX31 and i.MX31L Advanced Power Management features:

- Dynamic Process Temperature Compensation (DPTC)—dynamic adjustment of the supply voltage relative to the current temperature and the manufacturing process used.
- Dynamic Voltage Frequency Scaling (DVFS)—reduction of operating voltage to the *minimum* level needed to support only the *minimum* operating *frequency* required by running applications at the given moment. The i.MX31 and i.MX31L bring the concept to new heights by introducing an automatic hardware mechanism for DFVS control that requires minimum CPU resources and software (OS and drivers') complexity.
- Three separate Power Domains—CPU (ARM), peripherals, and the PLLs, provide the ability to save power in one domain while the others remain functional.
- Power Gating— the ability to shut down the entire IC (hibernate) or only the most power-hungry ARM® Platform power domain in standby mode.
- Independent low-power modes for different power domains, including the following modes:
  - Stop—Clocks off
  - Doze—Turn off the clocks/PLL
  - Hibernate—Power down
  - State Retention—Retain ultra-low voltage
- Active Well Biasing—Reduces standby leakage by up to 15 times by lowering the well voltage of the transistor. Standby leakage is a great concern in sub-micron manufacturing processes' IC designs in the semiconductor industry.
- Careful and power-friendly IC design with 3 levels of clock hierarchy, enabling shutting down clocks to the parts of logic that are not used by the running application.
- Technology choice for optimum trade-off between speed and low-power, high-performance, yet with leaky transistors (*low-Vt*) versus ultra-low power semiconductor circuits (*high-Vt*) for functional modules with modest performance requirements.

2 Power Consumption Model

Power consumed by a semiconductor device has two components—dynamic and static:

$P_{total} = P_{dynamic} + P_{static}$

The dynamic power should be considered in only the active mode, when signal values are switching, and when analog circuits change their state, in other words, when operations occur because of the device performing its function. The dynamic power is defined by:

$P_{dynamic} = C_{apacitance} \times V_{oltage}^2 \times F_{requency}$

In the formula, the voltage is squared, and so has had a great effect on the consumed power and, thus, on the battery life.

On the other hand, the static power which is significantly smaller than the dynamic power when the device is in its active mode, plays the main role in the Standby Mode (a cellular phone in its inactive state, a PDA that is switched off, etc.) which is the dominant mode in the lifetime of the device. In typical usage Standby time is longer than active time by a factor of ten.

P_{static}= f(leakage current)

Static Power is a function of leakage, which, on its own, is dependent mostly on the manufacturing process used, the size of the die, and the voltage in the transistor well as shown in Figure 1. While the DPTC and DVFS techniques reduce dynamic power consumption, all other techniques primarily address the Static Power in standby.

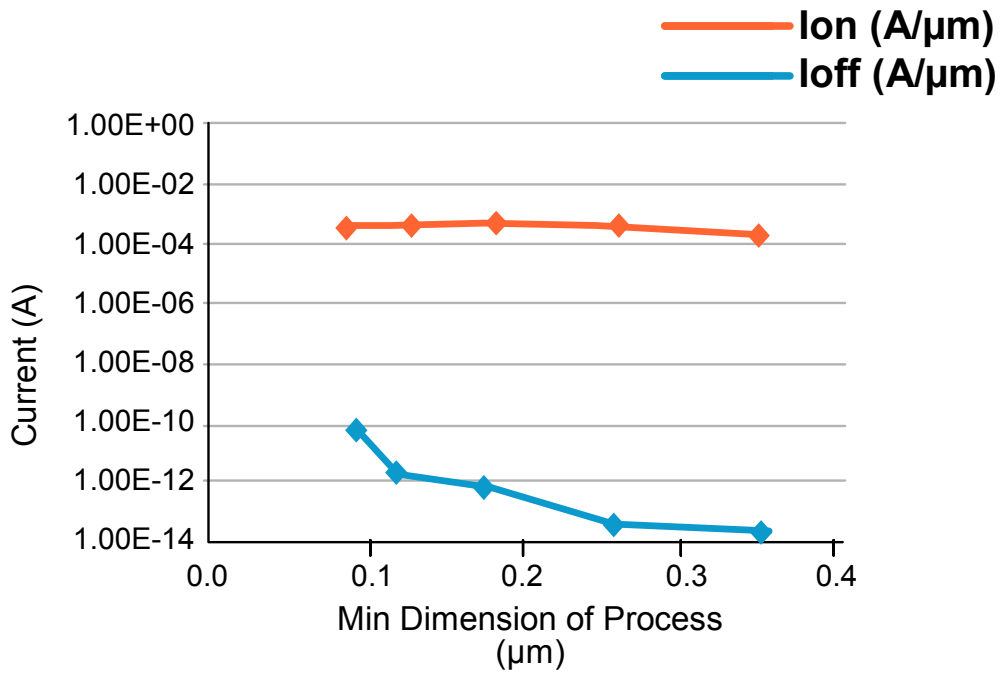

Figure 1. Leakage Current vs. Manufacturing Process

3 Dynamic Process Temperature Compensation

A key engineering philosophy at Freescale designing processors that perform under “worst case” conditions. Worst case in the semiconductor industry applies to very high temperatures and variations in the manufacturing process; transistor performance varies in a predefined range of parameters. Thus, some IC parts in the same lot come out capable of supporting higher operating frequencies (fast process), or lower frequencies at the bottom of the pre-defined performance window (slow process) at the given voltage. The Dynamic Process Temperature Compensation (DPTC) mechanism (Figure 2) measures delays of reference circuits that are dependent on the process speed and temperature, then lowers the voltage to the minimum level needed to support the current operating frequency.

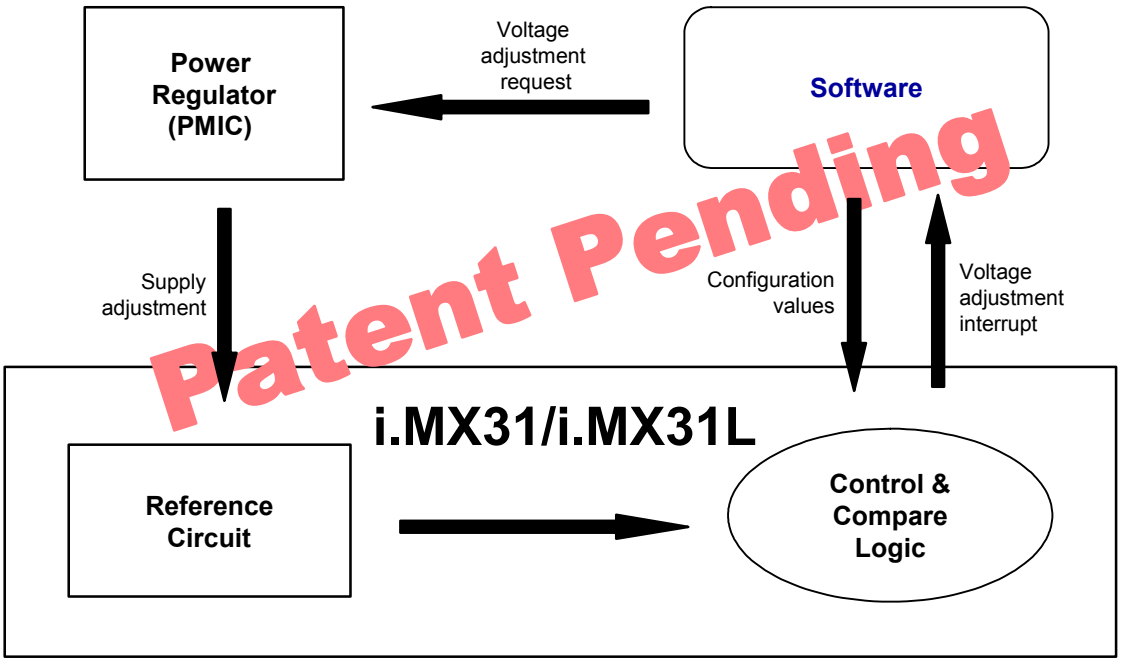

Figure 2. Dynamic Process Temperature Compensation (DPTC) Mechanism

So, a device containing a fast-process IC operating in a moderate climate condition can be expected to work at the worst-case calculated voltage to support the required frequency. In room temperature conditions, a typical process case 1.2 V is enough for DPTC-enabled 90 nm i.MX31 and i.MX31L processors, while a conventional 90 nm design will require 1.6 V. This may result in a power savings approaching 40%, thereby nearly doubling the battery life.

The inputs from reference “sense” circuits are processed by internal control and compare logic and written to software-readable registers. If there is a significant (pre-defined) change in the reference circuit delay values, an interrupt is triggered, then the relevant software interrupt routine calculates the new required voltage and re-programs the Power Management IC (PMIC) to supply the new voltage to the i.MX31 and i.MX31L processors. After the new voltage is applied the reference circuit delay, values change, providing feedback and closing the loop of the DPTC mechanism, making sure the system stabilizes at the proper voltage level.

4 Dynamic Voltage Frequency Scaling

Dynamic Voltage Frequency Scaling (DVFS) is an advanced technique that allows on-the-fly frequency adjustment according to the current performance requirements of the system. By lowering the frequency, it is possible to lower the operating voltage (on-the-fly as well), thereby dramatically reducing the power consumption.The concept is not new, but the major innovation introduced in the i.MX31 and i.MX31L processors is an autonomous hardware mechanism that controls the frequency and voltage with minimal software involvement. Also, the performance requirements (system load) are monitored by dedicated hardware sampling the internal signals of the i.MX31 and i.MX31L processors, such as CPU execution status, data bus requests, and signals.

DVFS works in conjunction with DPTC making sure the minimal voltage is applied, taking into account both the performance and process-temperature conditions.

Figure 3 shows two approaches to DVFS that the i.MX31 and i.MX31L processors support.

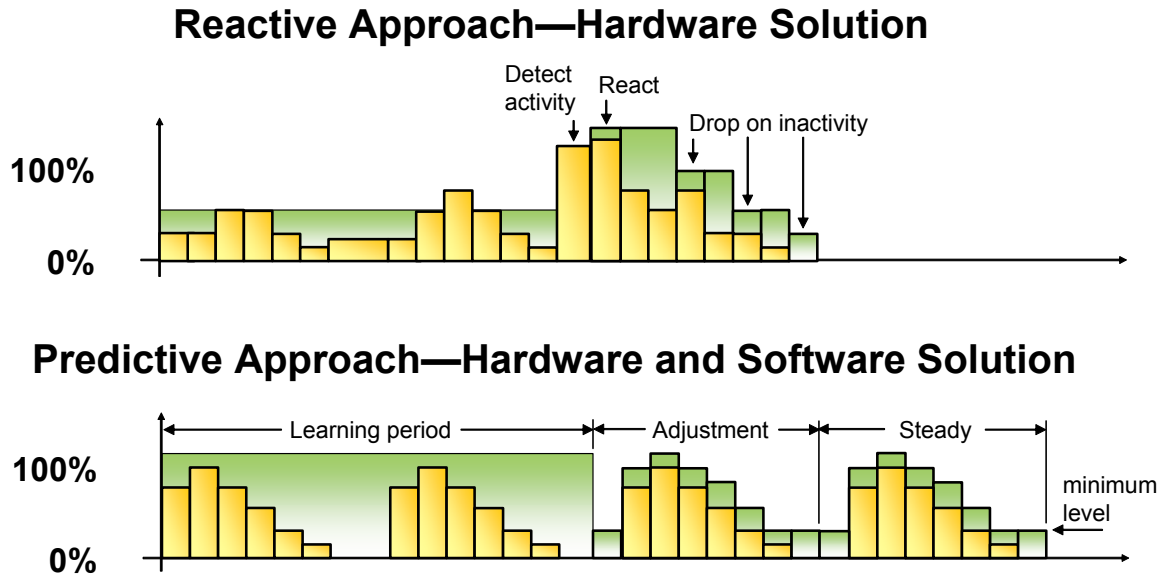

Figure 3. DFVS Approaches

The reactive approach is a hardware-driven mechanism with a minimal software interference (some initialization and occasional tracking required). In reactive mode the DFVS hardware measures system load. When it detects changes in performance requirements, it adjusts automatically the voltage and frequency.

The predictive approach is a software-driven mechanism, where the i.MX31 and i.MX31L DVFS hardware writes the system load measurements to the dedicated software-readable registers. The hardware also provides the interface for the software to program a pre-defined pattern for voltage and frequency. The example shown in Figure 3 describes a case where the software analyzes the system load pattern and tries to predict the future load. After it generates a prediction, it programs the DVFS hardware with a voltage-frequency pattern. In the case of an inaccurate prediction, an adjustment can be easily made.

For extreme cases when there is a sudden surge in the system load, requiring maximum performance from the system, the panic mode of the DVFS activates, switching to the maximum frequency and voltage.

Figure 4 on page 6 shows the DVFS hardware details.

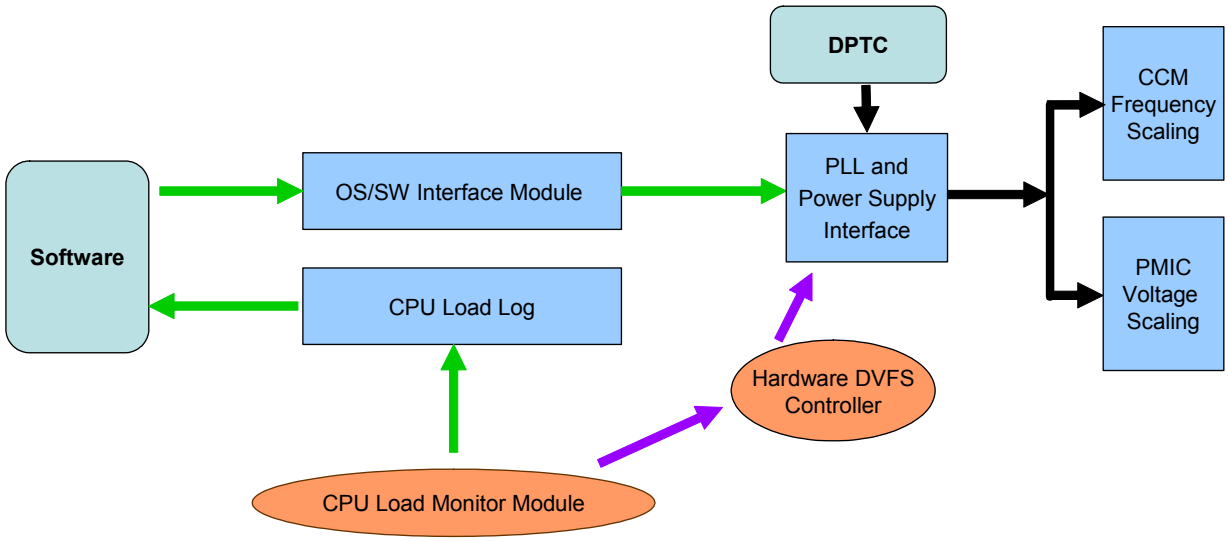

Figure 4. DVFS Hardware Mechanism

The hardware signals from different i.MX31 and i.MX31L functional units are sampled by the system load monitor logic. Pre-defined programmable weights can be assigned to different signals providing all the necessary input for the software to adjust the DVFS hardware behavior. The weighted and processed system load value is written to the system load register. This register value is sampled to the system load log so that the software DVFS algorithm can analyze system behavior and provide necessary adjustments by programming the frequency-voltage pattern register.

The system load register also outputs its value to the reactive logic. The reactive logic includes software-pre-programmed threshold system load levels. Once the system load changes by crossing a threshold boundary, the reactive logic sends a command to the DVFS interface to switch voltage and frequency. If the system load suddenly jumps to a pre-defined maximum performance threshold value, the system triggers the panic mode, switching as soon as possible to the highest voltage and frequency level. The system response time in this case is negligible, since everything is done automatically, independent of the CPU state and the software (OS) event latency policy.

Software complexity involved in the reactive mode is negligible—primarily involving initial system setup and occasional adjustments during runtime. For the predictive mode, the software developer can implement as complex algorithm as desired, as the i.MX31 and i.MX31L processors provide all the hardware tools for that.

5 Power Saving Modes

The i.MX31 and i.MX31L processors offer many different power saving modes, giving the system developer the ability to trade off between power consumption in stand-by and recovery times as shown in Figure 5 on page 7. One of the important features is the hardware handshake of the i.MX31 and i.MX31L clock controller with peripherals before entering a low-power mode. This allows the relatively power-hungry ARM core to enter a low-power mode immediately without waiting for the peripherals to complete their tasks.

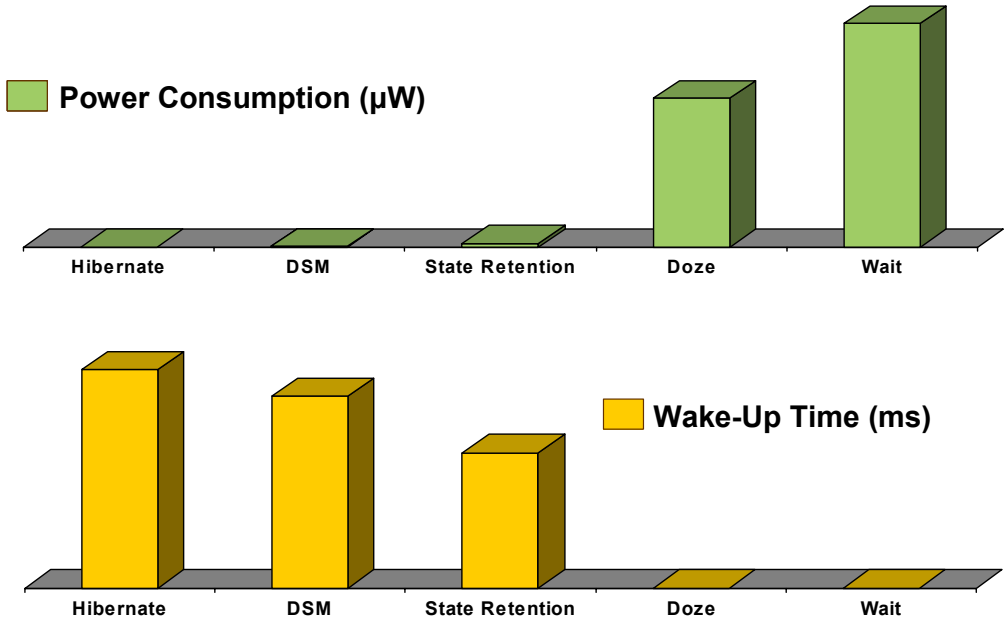

Figure 5. Power-Saving Modes vs. Wake-Up Time

5.1 Run

This is the normal, functional operating mode of the i.MX31 and i.MX31L processors. Frequency and voltage may vary according to DVFS and DPTC standards.

5.2 Wait

In this mode, the ARM11^{TM} MCU clock is stopped, but the i.MX31 and i.MX31L bus switch (MAX) and all peripherals' clocks remain active. This mode is useful for running low MIPS applications that primarily involve peripheral activity, such as a viewfinder that can be run with minimal ARM11 MCU involvement in i.MX31 and i.MX31L processors.

5.3 Doze

In this mode, both the ARM11 and MAX clocks are stopped. Clocks for specific peripherals can be switched off automatically in Doze mode by pre-programming the Clock Controller module. This mode is useful for processes that require quick reactivation.

5.4 State Retention

In this mode, all clocks are switched off and the PLL is disabled. External memory is put in low-power (self-refresh) mode. State retention uses less power and has a longer wake-up time than Doze mode, but there is no need to recover any data after the wake-up.

5.5 Deep Sleep

In this mode, the power supply of the ARM Platform—the biggest consumer of power in i.MX31 and i.MX31L processors—is shut down. Any relevant register data should be saved before entering Deep Sleep mode (WFI, otherwise known as Wait-For-Instruction).

5.6 Hibernate

The power supply of the entire i.MX31 and i.MX31L IC is shut down. All internal data should be saved to external memory prior to Hibernate.

6 Power Domains

Another important feature of the i.MX31 and i.MX31L processors is the division of the IC into power domains—providing the flexibility of clocking-off/powering-off different parts of the IC. The domains are as follows:

- MCU—Includes the ARM11 Core, the MMU, and the L1 Caches.
- L2 cache—Includes L2 cache data array.
- Peripheral—Includes all peripherals.
- PLL—Includes PLLs and the FPM (Frequency Pre-Multiplier).

7 Active Well-Bias (AWB)

Active Well-Bias battles the high-performance transistor current leakage of the advanced submicron manufacturing process technology of the i.MX31 and i.MX31L processors. By controlling the transistor well supply, the threshold voltage of leaky high performance transistors is reduced resulting in an increase of standby current by a factor of 10. Traditionally, the only shortcoming of the well-bias technique is the necessity to add an AWB Charge Pump to support the separate well supply. The i.MX31 and i.MX31L processors solve this problem by integrating their own AWB Charge Pump on-chip. Figure 6 on page 9 shows a contrast of well-biased gate versus conventional design.

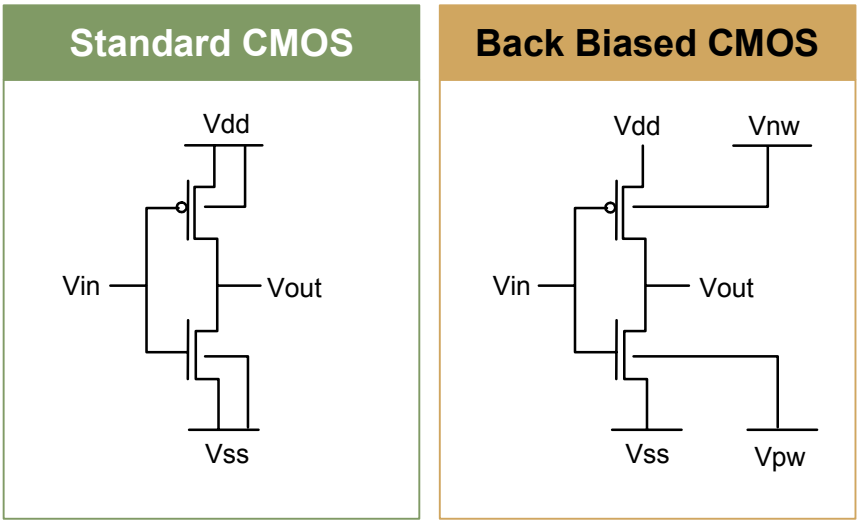

Figure 6. Well-Biased Gate vs. Conventional Design

8 State-of-the-Art Clock Tree Design

The clock tree is an important contributor to total power consumption, the clocks themselves being constantly switching signals when enabled and causing many other portions of logic to change value, drawing dynamic current. Balancing the clock tree is also very important not only to prevent functional failures, but to avoid unnecessary switching of logic values back and forth between different clock domains, until all clocks propagate. Figure 7 on page 10 shows the clock tree diagram.

Three main methods were applied to the design as follows:

- Custom design of the clock controller—manual balancing of the clocks
- Clock gating in RTL of modules when they are functionally disabled
- Automatic design tools' clock gating

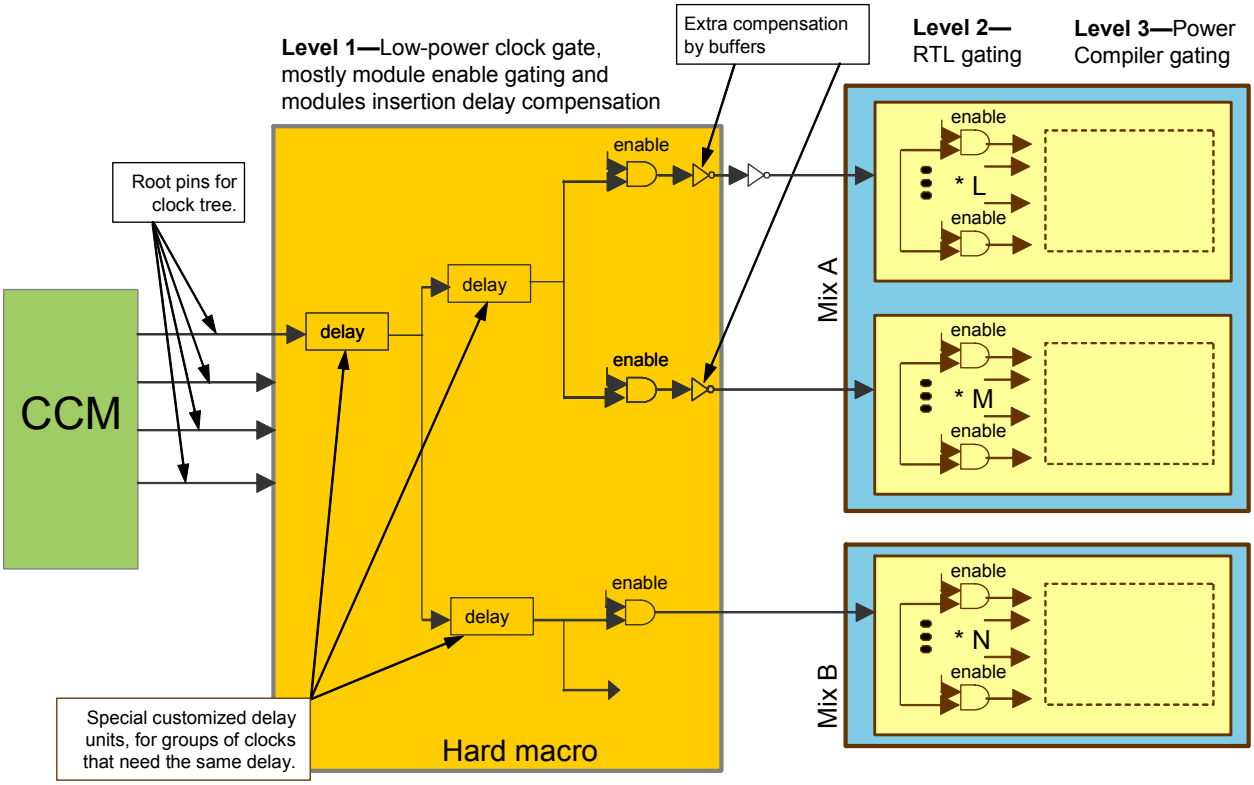

Figure 7. i.MX31 and i.MX31L Clock Tree Simplified Diagram

9 Conclusion

The i.MX31 and i.MX31L processors address all aspects of power management. They save dynamic power using the DPTC and DVFS, they reduce leakage with AWB, and they also offer multiple power saving modes. Devices having an i.MX31 or i.MX31L processor on-board will have all the means to multiply its operating time using the same battery versus using other conventional designs. All of the power saving is achieved using minimum additional software complexity and CPU load. The i.MX31 and i.MX31L processors open many new possibilities for the power aware system developer, as no other chip has done before.

10 Revision History

Rev. 1 changes the sentence in Section 7, Active Well Bias from:

By controlling the transistor well supply, the threshold voltage of leaky high performance transistors is reduced resulting in **a reduction** of standby current by a factor of 10.

To: By controlling the transistor well supply, the threshold voltage of leaky high performance transistors is reduced resulting in **an increase** of standby current by a factor of 10.

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