i.MX35 PDK Hardware

User's Guide

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About This Book

This document explains how to connect and operate the i.MX35 3-Stack Platform System.

Audience

This document is intended for software, hardware, and system engineers who are planning to use the product and for anyone who wants to understand more about the product.

Organization

This document contains the following chapters.

Chapter 1	Introduces the features and functionality of the 3-Stack board.
Chapter 2	Provides configuration and setup information.
Chapter 3	Provides block diagrams and memory mapping.
Chapter 4	Provides functional operation information.
Chapter 5	Describes the multiplexing pin signals.

Conventions

This document uses the following conventions:

`Courier`	Is used to identify commands, explicit command parameters, code examples, expressions, data types, and directives.
Italic	Is used for emphasis, to identify new terms, and for replaceable command parameters.

Definitions, Acronyms, and Abbreviations

The following list defines the abbreviations used in this document.

APMS	Atlas Power Management System
ATA	Hard drive interface spec
CD	Compact Disk
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Custom Programmed Logic Devices
CPU	Central Processing Unit
CSI	Camera Sensor Imaging
CSPI	Serial Peripheral Interface
DCE	Data Communications Equipment
DDR	Double Data Rate
DIP	Dual In-line Package
DMA	Direct Memory Access

DTE	Data Terminal Equipment
DUART	Dual Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
FIR	Infra Red
GPIO	General Purpose Input/Output
GPO	General Purpose Output
I^2C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
I/O	Input/Output
IrDA	Infrared Data Association
ISA	Instrumentation, System, and Automation Society
JTAG	Joint Test Access Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MB	Megabyte
MCU	Microcontroller Unit
MMC	Multi-media Card
MCP	Multi-chip product
MS	Memory Stick
NVRAM	Non-volatile Random Access Memory
OTG	On the Go
PC	Personal Computer
PCMCIA	Personal Computer Memory Card International Association
PCB	Printed Circuit Board
PHY	Physical interface
POR	Power on Reset
PSRAM	Pseudo Random Access Memory
PWM	Pulse Width Modulation
QVGA	Graphics Adapter
RAM	Random Access Memory
SD	SanDisk (Smart Media)
SDRAM	Synchronous Dynamic Random Access Memory
SI	System International (international system of units and measures)
SIMM	Single In-Line Memory Module
SPST	Single Pole Single Throw
SSI2	Synchronous Serial Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Chapter 1
Introduction

The i.MX35 3-Stack Platform System helps you develop automobile infotainment applications using the i.MX35 ARM-11 MCU . That represents the next step in low-power, high-performance application processors.

The 3-Stack platform consists of the CPU Engine board, Personality board, and Debug board. The system supports application software development, target board debugging, and optional circuit cards. The CPU board can be run in stand-alone mode for code development. An LCD display panel is supplied with the 3-Stack system.

Figure 1-1 shows the major components of the 3-Stack system.

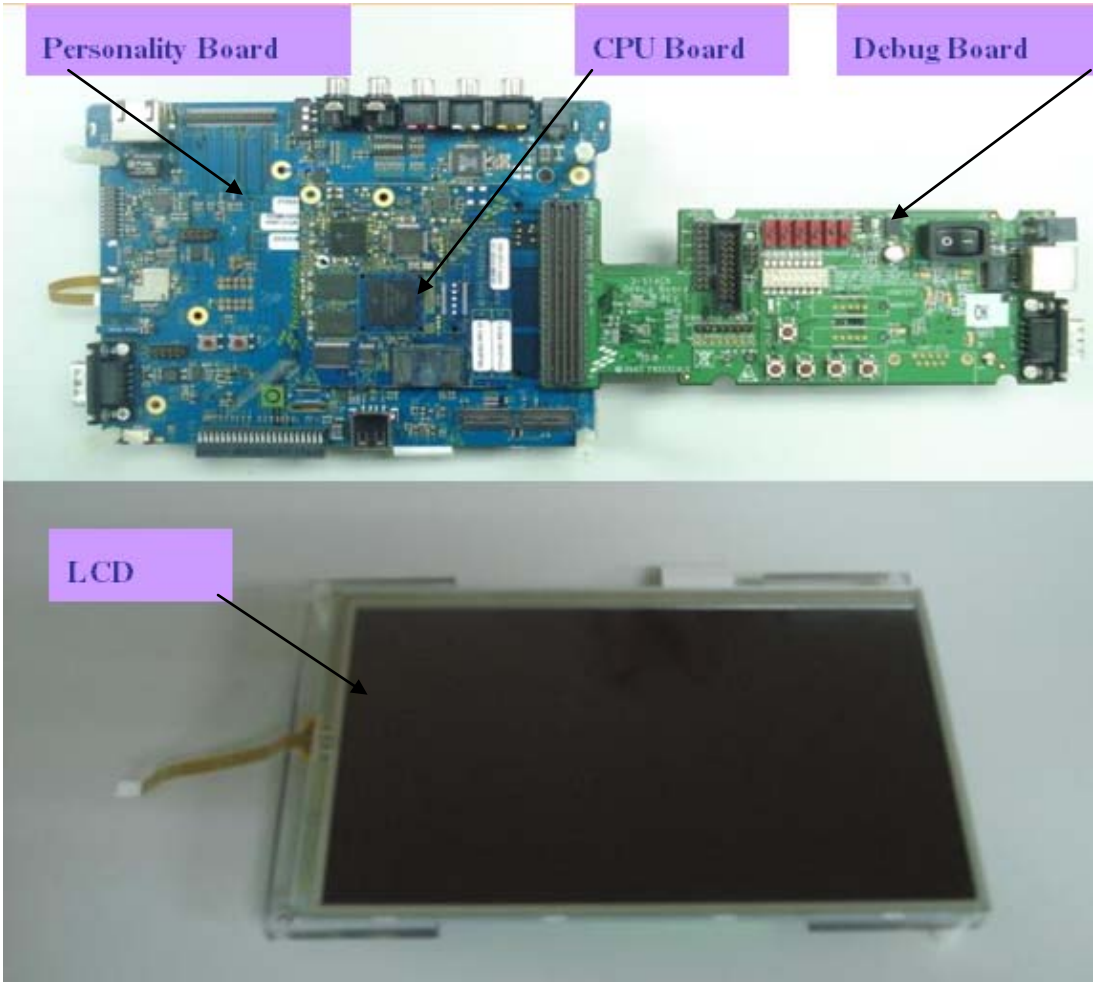

Figure 1-1 Major Components of the 3-Stack System

1.1 Features

The 3-Stack system can be used in two ways: the development mode requires a three-board assembly; the demonstration mode requires only a two-board assembly (without the Debug board).

The system includes the following features.

- Near form-factor demonstration modules and working platforms.
- Solid reference schematics that closely resemble final products to aid customers' designs.
- Three-board system, which includes:
  - CPU board with i.MX35 ARM11 MCU
  - Personality board with peripheral components and interface connectors
  - Debug board with two RS-232 interfaces, 10/100 Base-T Ethernet connector, and current measurement connectors.
- Utilizes reliable high-density connector to interface between boards.

Figure 1-2 illustrates the three-board assembly, which can be set up for software development (three boards) or demonstration (two boards).

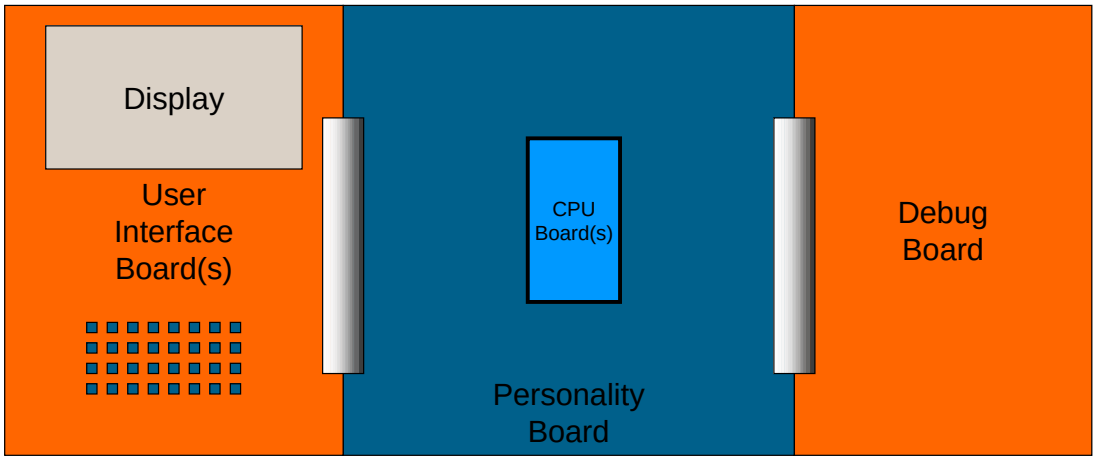

Figure 1-2 3-Stack Primary Boards

1.2 Components

Table 1.1 describes the i.MX35 board components.

Table 1.1 Board Components

Item	Description
ATA5-compliant controller	One 44-position dual row, 2mm header for small form-factor disk drivers and two CE-ATA connector
Audio codec header	Audio codec header for the connect audio feature card
Camera connector	Image sensor camera connector
CAN bus connectors	One DB9 connector for the CAN bus, and one 10-pin connector for the CAN bus
Clocks	System clock sources: 24MHz and audio clock source 24.567MHz
DDR2 memory	256MB of 32 bit DDR2 memory
Debug support	RealView-ICE® debug support
Flash memory, NAND	2 GB of MLC NAND Flash Memory
Flash memory, NOR	64MB of NOR Flash Memory
FM Receiver	
GPS connector	One connector to out board GPS module
Jacks and speaker terminals	Microphone jack, headphone and video jack, stereo and mono (ear piece) speaker terminals
LCD	7 inch LCD display panel with touch panel and LED backlight
MLB signal connector	One 2mm connector for the MLB signal
Power management	Configurable intelligent management of system power through power management chip ATLAS AP LITE
Power supply	+5.0 VDC, 2.4 A universal power supply
Reset	Reset control from ATLAS AP LITE
RS-232	One RS-232 interface with DB-9 connector, which is driven by the UART channel internal to the i.MX35
SD card connectors	Card sense functionality; also supports MMC and MS cards
TV IN decoder	Supports Y.Pr .Pb input
USB host transceiver	One USB fast-speed host transceiver, with standard USB host connector
USB OTG	One USB On-the-Go (OTG) high-speed transceiver with MICRO USB connector

1.3 System and User Requirements

You will need a PC that includes:

- Windows 98™, ME™, 2000™, XP™, or NT ™ (version 4.0) operating system
- One +5VDC, 2.4A power supply with a female (inside positive) power connector (included)

CAUTION

Never supply more than +5.5 V power to the i.MX35 3-Stack. Doing so can damage board components.

1.3.1 System Operating Specifications

Table 1.2 identifies the clock, environmental conditions, and dimensions of the i.MX35 3-Stack system.

Table 1.2 System Operating Specifications

Item	Specifications
Clock	24 MHz
Temperature: Operating Storage	 -10 °C to + 50 °C -40 °C to +85 °C
Relative Humidity	0 to 90% (noncondensing)
Power Requirements	4.5V to 5.5 V DC @1.5A
Dimensions	CPU Engine board: 72.00mm x 76.00 mm Personality board: 177.62mm x 132.00mm Debug board: 71.400mm x 174.900mm

Chapter 2
Configuration and Connections

This section contains configuration information, connection descriptions, and other operational information that may be useful during the development process.

2.1 Debug Board Configuration

The Debug board provides an interface for programming and debugging the i.MX development systems and reference platforms.

The Debug board is a small card that you can insert or remove from the platform. The ability to remove the Debug board is a major advantage to marketing and sales teams who want to demonstrate and showcase a variety of products and ideas in a streamlined, near form factor way, without the added software development bulk.

2.1.1 Debug Board Top Switches and Connectors

Figure 2-1 identifies the switches and connectors located on the top of the Debug board. Table 2.1 describes the switches and connectors.

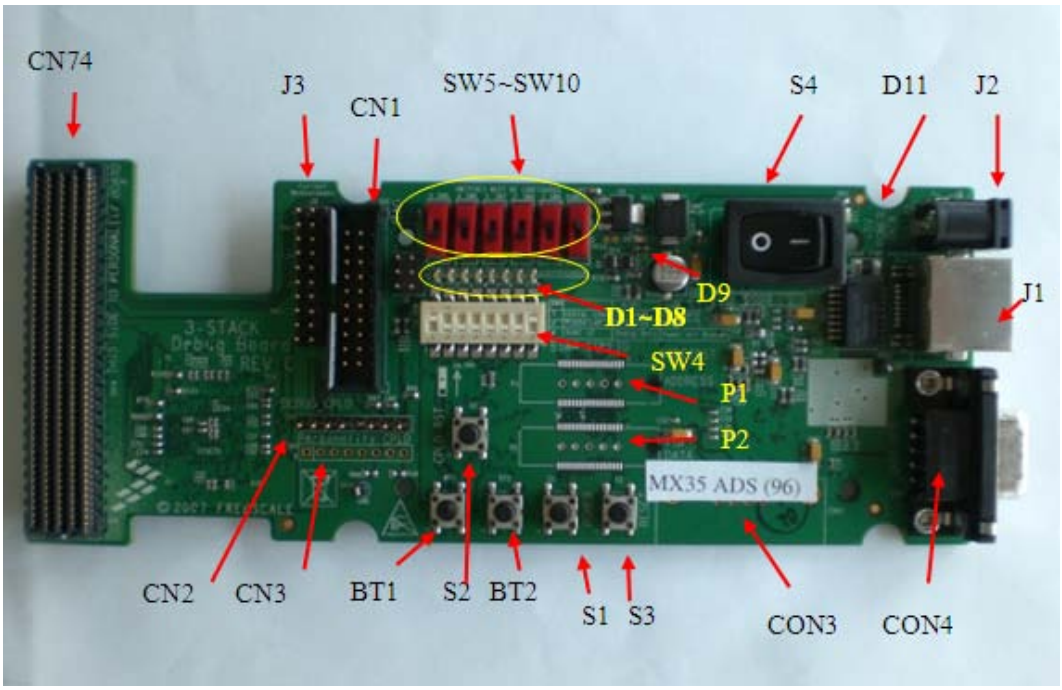

Figure 2-1 3-Stack Debug Board, Top View

Table 2.1 Debug Board, Top Components

Identifier	Component	Description
S1	Power Button	Connected to the ON1B input of the MC13783 through the 500 pin connector. The line is pulled up, and pushing it grounds the line. If MC13783 is in Off, User Off or Memory Hold Mode, the board can be powered on via pushing the button.
S2	Reset Button	Resets the Debug board.
S3	System reset switch	Connects the RESETB to MX35 The line is pulled up; pushing it grounds the line.
S4	Power on switch	Powers up the Debug board when set to 0.
J1	Ethernet connector	10/100 Base T Ethernet RJ45 Connector
J2	Power connector	5.0V DC power connector
J3	Current measurement connector	Measures the current at various points of CPU Engine and Personality board from the connector.
F1	Fuse	Re-settable fuse; re-settable over-current protection
D1 – D8	LEDs	LEDs for CPLD debug
D9	LED	LED for Debug board 3.3V power; lights when turned ON.
D11	LED	LED for DC power supply; lights when 5.0V DC power is applied
P1	WEIM Address measurement connector	Supports the CodeTest Interface Probe
P2	WEIM Data measure connector	Supports the CodeTest Interface Probe
BT1, BT2	Test buttons	Test buttons for CPLD
CN1	Connector	i.MX35 JTAG connector
CN2	Connector	Debug board CPLD JTAG connector
CN3	Connector	Personality board CPLD JTAG connector (Reserved)
CN74	Connector	500 pin connector to the Personality board
CON3	Connector	UART (DCE) DB9 male connector
CON4	Connector	UART (DCE) DB9 female connector
SW4	Enable switch	Switch designation settings (see next table):

Switch Designation	Setting	Effect
SW4-1 UART Port Select	ON	Serial port UART (DTE) CON3 is selected.
	OFF	Serial port UART (DCE) CON4 is selected.
SW4-2 NorFlash Enable	ON	Enable NorFlash on Debug board
	OFF	Disable Norflash on Debug board
SW4-8 Power Enable	ON	Power supply to three boards
	OFF	Power supply to Debug board only

2.1.2 Boot Mode Switches

Settings for SW9 and SW10 determine where the processor begins program execution. Table 2.2 shows the valid combinations of the switches.

Table 2.2 Boot Mode Settings

Boot Mode Device	BOOT1 SW9	BOOT0 SW10
Internal boot	0	0
External boot	1	0
Enter wait mode	1	1

2.1.3 Debug Board Bottom Connectors

Figure 2-2 illustrates the bottom view of the Debug board, where J4 identifies the 500-pin connector to the CPU Engine board, and F1 is the resettable fuse that provides overcurrent protection.

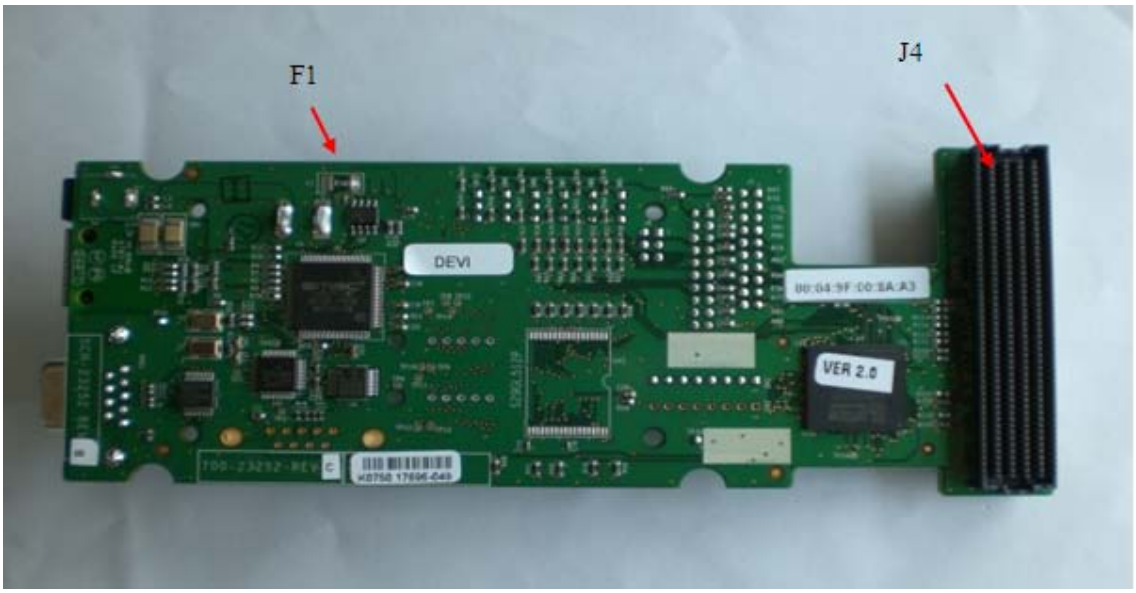

Figure 2-2 Debug Board, bottom view

2.2 Personality Board Connectors

This section describes the switches and connectors on the top of the Personality board, and the connectors on the bottom of the Personality board.

2.2.1 Personality Board Top Connectors

Figure 2-3 identifies the connectors on the top of the Personality Board.

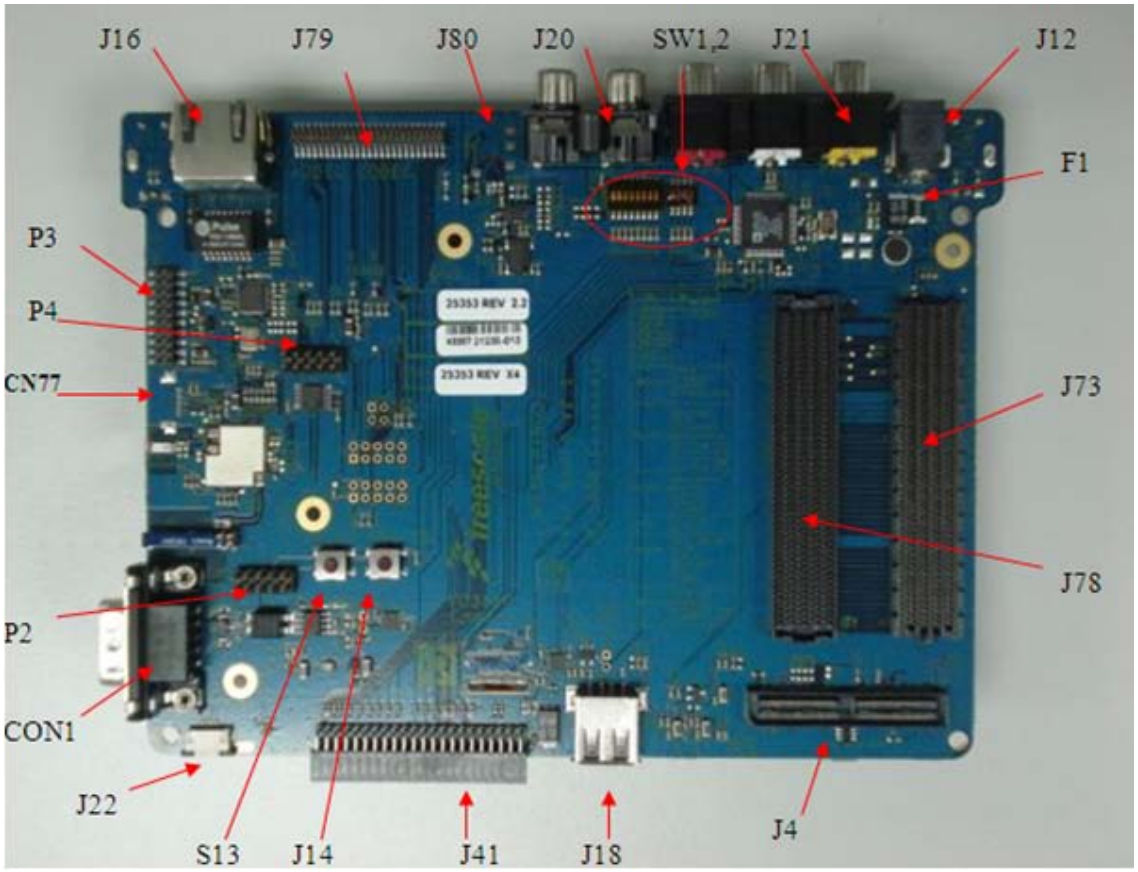

Figure 2-3 Personality Board, top view

Table 2.3 Personality Board Connectors, top

Component Identifier	Description
F1	Resettable over current-protection fuse
J4	User interface connector
J10	USB OTG micro-AB connector
J16	FEC connector
J20	Audio input connector
J21	J21 TV Y, Pr, Pb input connector

J22	Touch screen connector
J41	P-ATA module connector
J73	500 pin connector for connecting the Debug board
J78	500 pin connector for connecting the CPU board
J79	Audio codec connector
J80	Headphone connector
P2	CAN bus connector
P3	MLB module connector
P4	I2C connector
CON1	CAN connector
CN77	CE-ATA module connector
S13	RESET button
S14	POWER ON button
SW1, SW2	Boot config switch. Below is the detail function list

SW1 and SW2 Detail Function List			
SW2		SW1	
1	BT_MEM_CTL0	1	BT_USB_SRC0
2	BT_MEM_CTL1	2	BT_USB_SRC1
3	BT_MEM_TYPE0	3	
4	BT_MEM_TYPE1	4	
5	BT_PAGE_SIZE0		
6	BT_PAGE_SIZE1		
7	BT_ECC_SEL		
8	BT_BUS_WIDTH		

BT_MEM_CTL[1:0]	• 00 - WEIM • 01 - NAND Flash • 10 - ATA HDD • 11 - Expansion Device (SD/MMC, supports high storage, EEPROMs. See BT_MEM_TYPE[1:0] settings for details).

BT_MEM_TYPE[1:0]	If BT_MEM_CTL = **WEIM** then • 00 - NOR • 01 - Reserved • 10 - Reserved • 11 - Reserved If BT_MEM_CTL = **NAND Flash** • 00 - 3 address cycles • 01 - 4 address cycles • 10 - 5 address cycles • 11 - 6 address cycles If BT_MEM_CTL = **ATA HDD** • 00 = CE-ATA HDD • 01 = P-ATA HDD • 10 = reserved • 11 = reserved If BT_MEM_CTL = **Expansion Card Device** • 00 - SD/MMC • 01 - Reserved • 10 - Serial ROM via I2C • 11 - Serial ROM via SPI
BT_PAGE_SIZE[1:0]	BT_MEM_CTL = NAND FLASH 00 - 512 Bytes 01 - 2K Bytes 10 - 4KB with 128B spare 11 - 4KB with 218B spare
BT_ECC_SEL	0 - 4 bit ECC 1 - 8 bit ECC
BT_BUS_WIDTH	BT_MEM_CTL = NAND FLASH 0 - 8 bit 1 - 16 bit BT_MEM_CTL = NOR 0 - 16 bit 1 – RESERVED
BT_USB_SRC[1:0]	00 - UTMI PHY 01 - ULPI PHY 10 - Serial PHY: ATLAS 11 - Serial PHY: ISP1301

2.2.2 Personality Board Bottom Connectors

Figure 2-4 illustrates the bottom view of the Personality board. Table 2.4 describes the connectors.

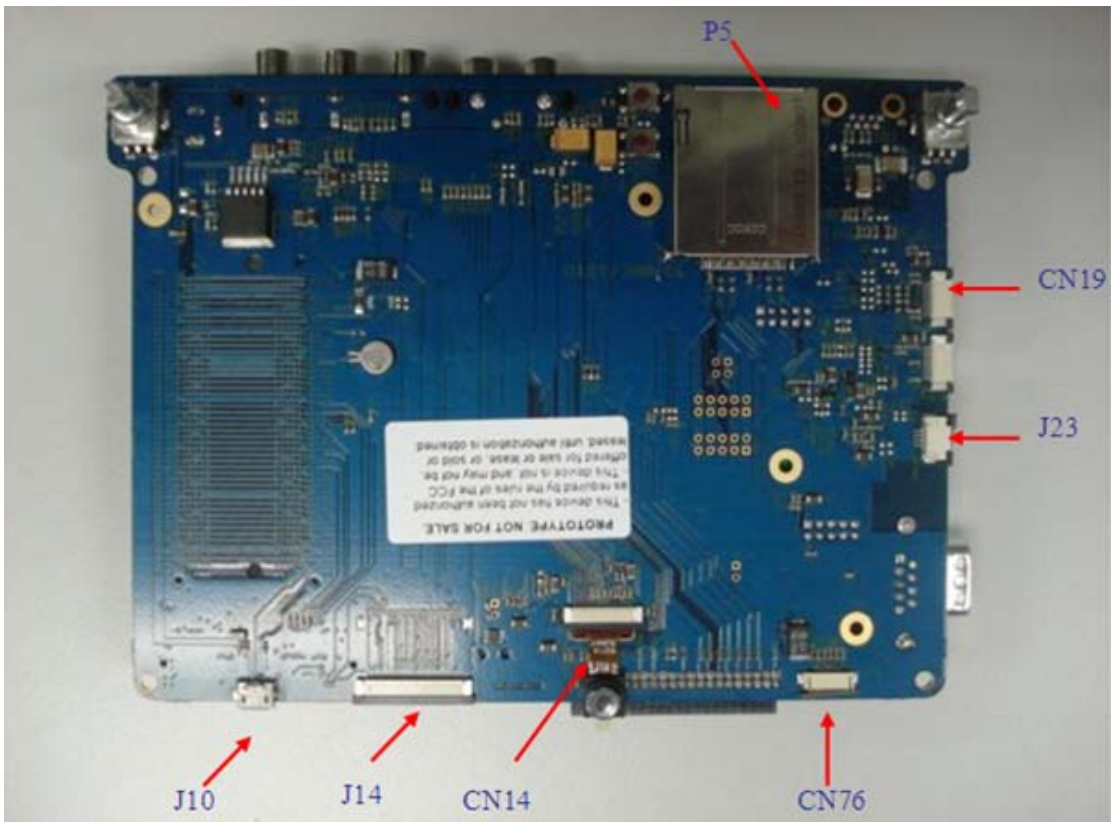

Figure 2-4 Personality Board, bottom view

Table 2.4 Personality Board Bottom Connectors

Component Identifier	Description
J10	USB OTG microAB connector
J14	CPT 7' WVGA LCD connector
J23	Touch Panel connector
CN14	CMOS module connector
CN19	GPS module connector
P5	SD card slot for MMC, SD and MS

2.3 CPU Board Connectors

2.3.1 CPU Board Top Connector

Figure 2-5 illustrates the top of the CPU board, where P1 is the ETM Connector.

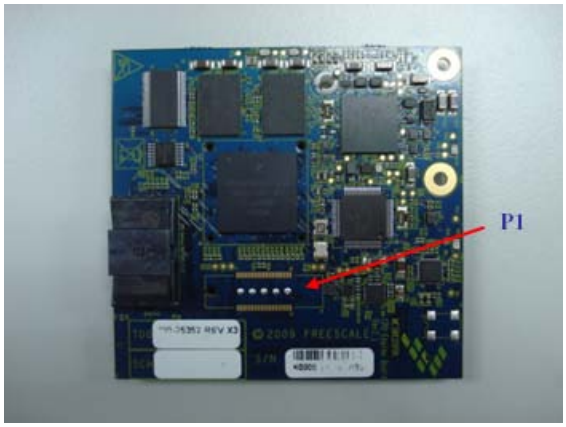

Figure 2-5 CPU Board, top view

2.3.2 CPU Board Bottom Connector

Figure 2-6 illustrates the bottom view of the CPU Engine board, where J1 is the 500-pin connector to the Personality board (for demos) or the Debug board (for development).

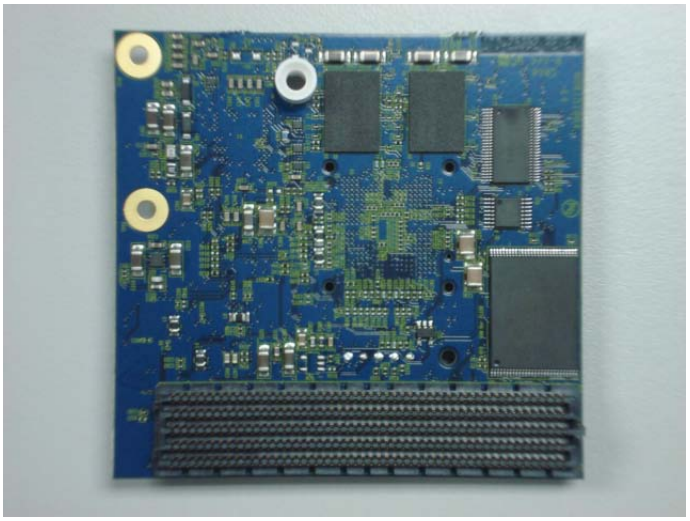

Figure 2-6 CPU Engine Board, Bottom View

2.4 Setting Up the 3-Stack Platform

2.4.1 Set the Debug Board Switches

To set the Debug board switches, use these steps:

1. Set CPU Engine and Personality board power enable switch SW4-8.
2. Set Boot Mode Switches, SW9 and SW10.
3. Make sure the switches on the Debug board are correctly configured. (refer to 2.1.1)

2.4.2 Connect the CPU and Debug Boards to the Personality Board

Figure 2-7 illustrates the connected boards.

Figure 2-7 Connected Boards

2.4.3 Install the LCD on the Personality Board

Attach the LCD to the board to enable easy use of the demo, and to protect the LCD. The panel is plastic and many screws are provided for stability.

To install the LCD, use these steps:

1. Glue the LCD to the plastic panel and attach the four screws (Figure 2-8).

Figure 2-8 Attach the LCD to the Panel

Figure 2-9 Attach the LCD to the Personality Board

2.4.4 Connect Power to the 3-Stack

The 3-Stack boards provide two DC power jacks: one in the Debug board and one in the Personality board (Figure 2-10).

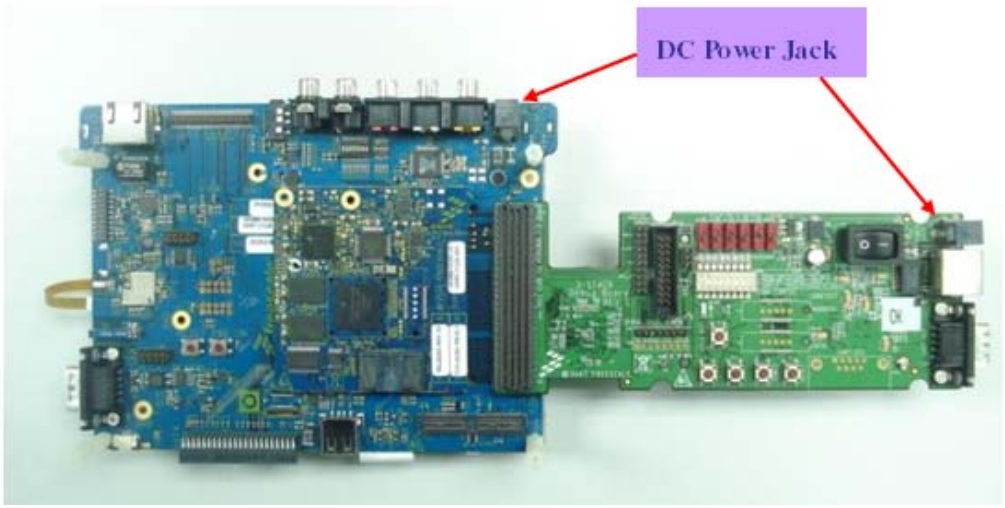

Figure 2-10 3-Stack Power Input

For software development, the three boards are assembled together. The 5.0V DC power should be plugged into the Debug board DC power jack. Press S4 on Debug board to "0" in order to power on the 3-Stack.

For demonstration purposes, the Personality board and CPU Engine board are assembled together, without the Debug board. The 5.0V DC power should be plugged into the Personality board DC power jack. The 3-Stack will be powered on directly.

Chapter 3
Functional Operation

3.1 Functional Block Diagrams

Figure 3-1 illustrates the CPU Engine Board.

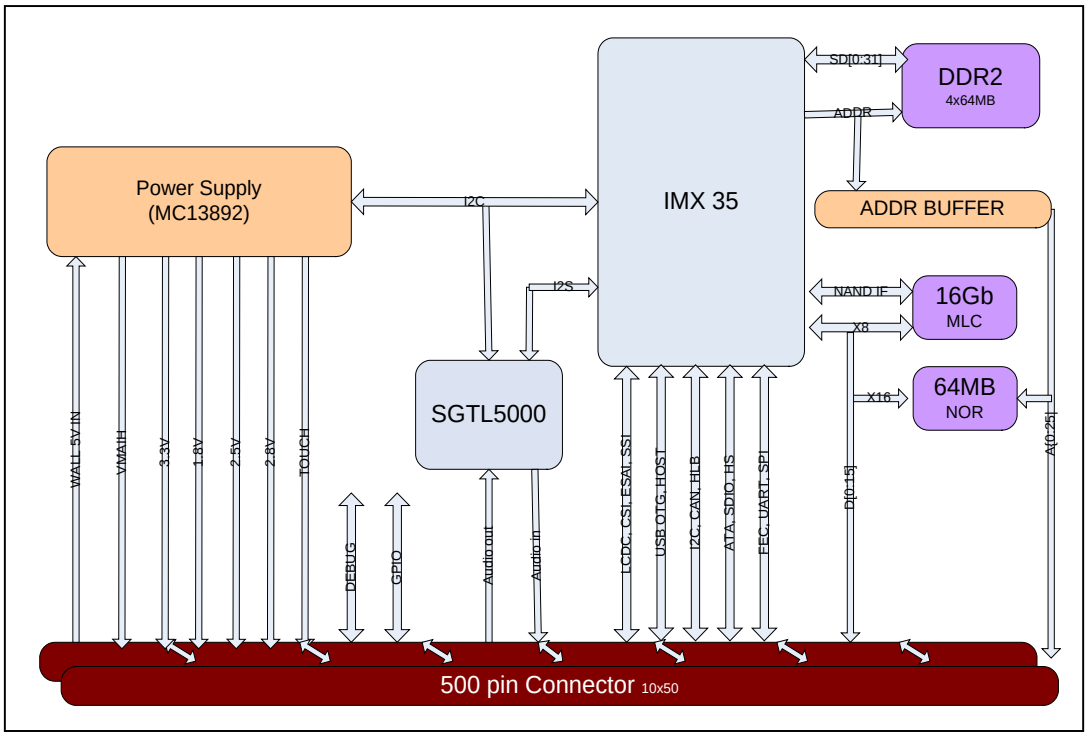

Figure 3-1 CPU Engine Board

Figure 3-2 illustrates the Debug board.

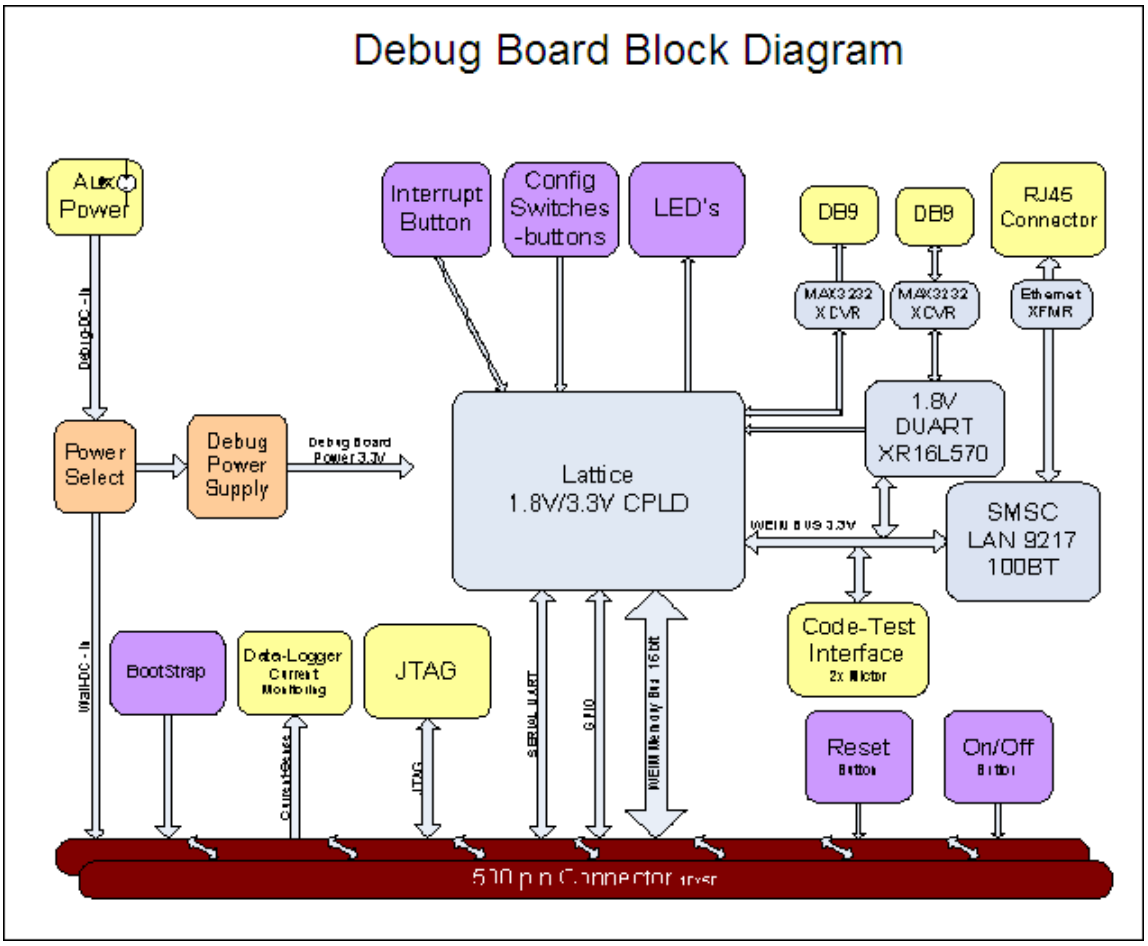

Figure 3-2 Debug Board

Figure 3-3 illustrates the Personality board.

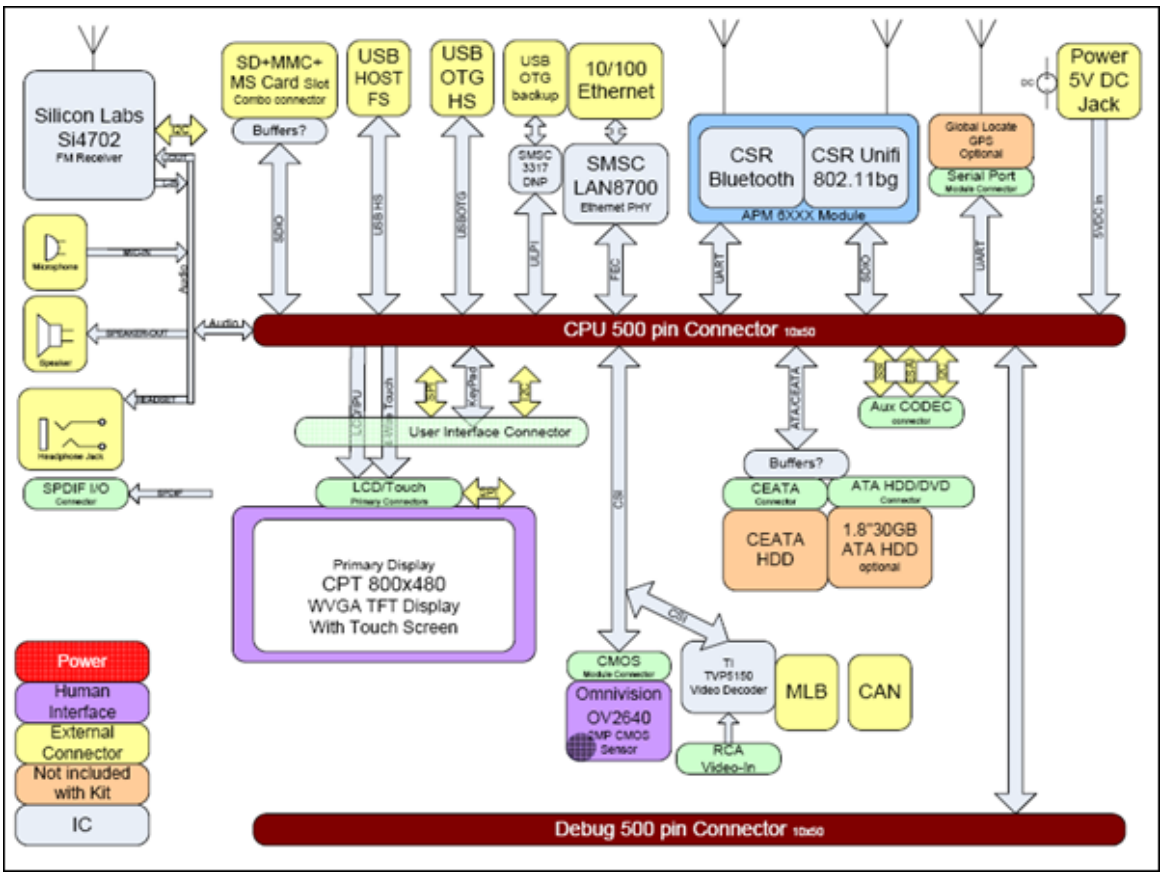

Figure 3-3 Personality Board

3.2 3-Stack Memory Map

Table 3.1 describes the memory map for the 3-Stack system. None of the memories take up the entire address space of the associated chip selects, and the software can access the same physical memory location at more than one range of address. For instance, DDR SDRAM occupies only 128 MB of the 256MB space available to CSD0, so it appears in two different ranges of addresses.

Table 3.1 Memory Map

Peripheral	Chip Select	Address Range (HEX)	Size
DDR2	$\overline{\text{CSD0/1}}$	0x8000_0000 to 8FFF_FFFF	256MB
Ethernet Controller LAN9217	$\overline{\text{CS5}}$	0xB600_0000 to B600_007F	128 bytes
External UART-A DB9-Male	$\overline{\text{CS5)}}$	0xB600_8000_ B600_8007	8 Bytes

3.3 CPLD on the Debug Board

A complex programmable logic device (CPLD) is an electronic component used to build reconfigurable digital circuits. The CPLD provides a great deal of functionality, including glue logic, which is needed to achieve compatible interfaces between two (or more) different off-the-shelf integrated circuits. For the 3-Stack board, glue logic provides peripheral bus address decoding, board control and status signals, board revision registers, and other functions, and is implemented with a CPLD on the Debug board.

3.3.1 CPLD Features

The CPLD provides the following key features:

- A 16-bit slave interface to the CPU data bus
- Address decode and control for the Ethernet controller
- Address decode and control for the external UART controller
- Level shift for Ethernet signals and UART signals
- Control and status registers for various board functions

3.3.2 CPLD Memory Map

Table 3.2 CPLD Memory Map

CS5_B	A16	A15	A14	A5	A4	A3	A2	Description
0	0	0	0	x	x	x	x	SMSC LAN9217 Ethernet 10/100BT
0	0	0	1	x	x	x	x	External UART-A
0	0	1	0	x	x	x	x	External UART-B
0	0	1	1	x	x	x	x	Reserved
0	1	0	0	0	0	0	0	Read/Write LED's (1=on, 0=off)
0	1	0	0	0	0	0	1	Read Only Switches/Buttons
0	1	0	0	0	0	1	0	Read Only Status - Interrupts, Interrupt latch
0	1	0	0	0	0	1	1	Read/Write - Interrupt Mask
0	1	0	0	0	1	0	0	Write - Interrupt reset
0	1	0	0	0	1	0	1	R/W Software Override: Set UART-B/CPU UART routing
0	1	0	0	0	1	1	0	R/W Software Override: Enable/Disable Flash Access, select CSx
0	1	0	0	0	1	1	1	Software Override 3 reserved
0	1	0	0	1	0	0	0	Read Only Returns AAAA
0	1	0	0	1	0	0	1	Read Only Returns 5555
0	1	0	0	1	0	1	0	Read Only CPLD Code Version #
0	1	0	0	1	0	1	1	Read Only Returns CAFÉ
0	1	0	0	1	1	0	0	Reserved

3.3.3 Programming the CPLD

To program the CPLD, use these steps:

1. Install Lattice ispLEVER Project Navigator Ver 6.0 on the PC.
2. From the **Start** menu, select **Programs** > **Lattice Semiconductor** > **Accessories** > **ispVM System**.
3. Connect the **Lattice CPLD ispDOWNLOAD Cable** to the PC parallel port.
4. Attach the **JTAG** connector to **CN2** on the Debug board.
5. Power on the Debug board.
6. Scan **Chain**.

   The CPLD device list is displayed (Figure 3-4).

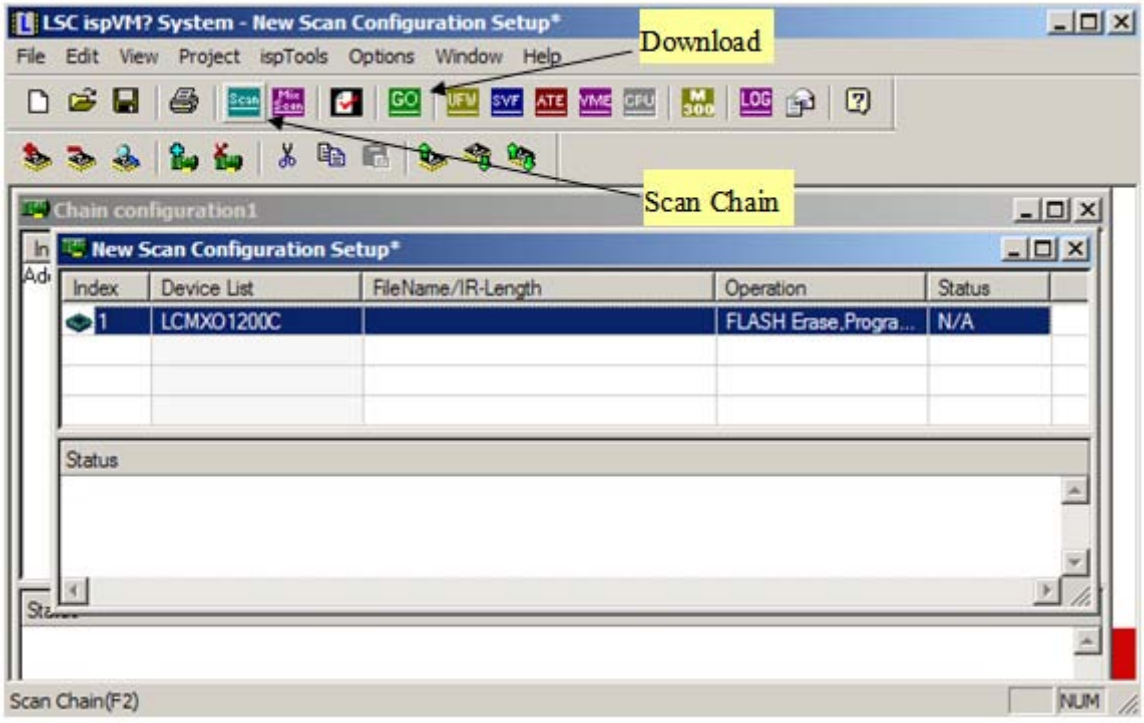

Figure 3-4 Scan CPLD Devices

7. Double-click **LCMXO1200C**.

8. Select the CPLD data file (Figure 3-5).

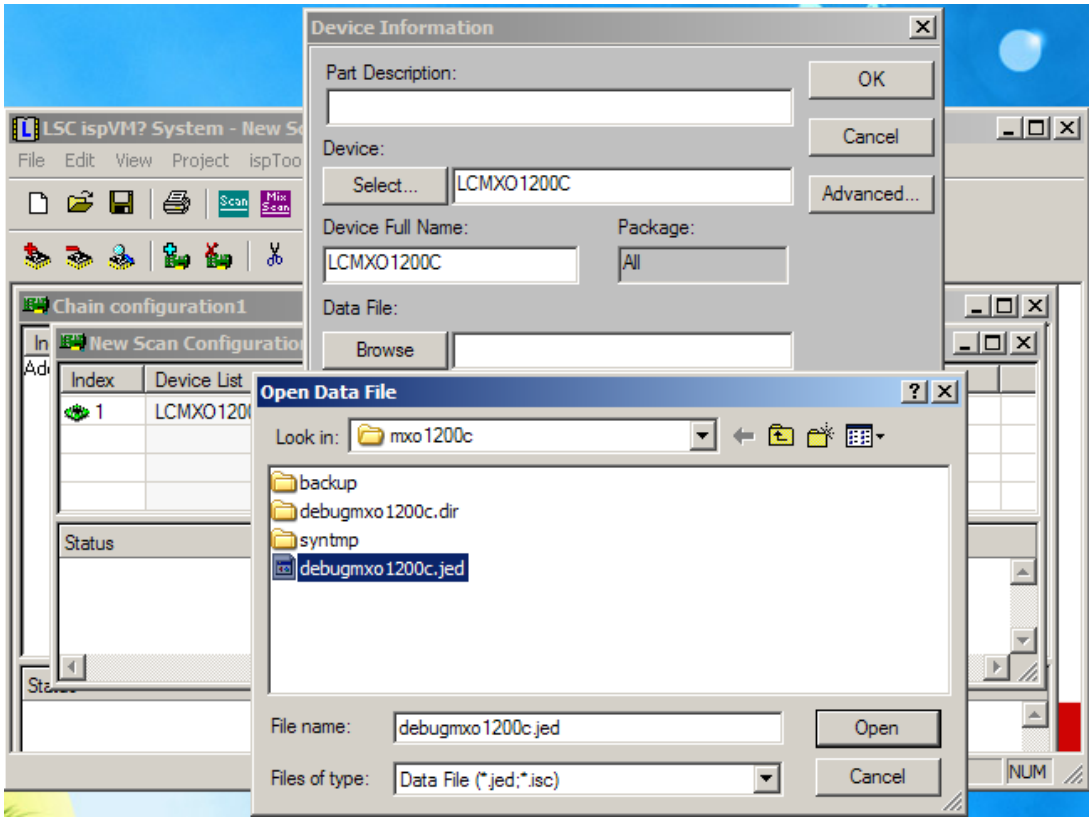

Figure 3-5 Selecting the CPLD Data File

9. Click GO to download the data file in the CPLD.
10. Wait about 10 seconds.

    When the Status section displays **PASS**, programming the CPLD is completed.

3.4 i.MX35 GPIO Grouping

The i.MX35 3-Stack uses an MCU and its GPIO to perform control operations. Table 3.3 describes the GPIO pins.

Table 3.3 MCU GPIO Grouping Descriptions

Pin location	I/O Name	I/O Description	Pull	Comment
1	PTA0/AD0	reserved		
2	PTA1/AD1	reserved		
3	PTA2/AD2	reserved		
4	PTA3/AD3	reserved		
5	PTA4/AD4	ESAI or USB host reset		
6	PTA5/AD5	Headphone Detect		
7	PTA6/AD6	USB host OC or ESAI GPIO		
8	PTA7/AD7	Interrupt to Ringo		OD
9	PTB0/AD8	KP_ROW0		
10	PTB1/AD9	KP_ROW1		
11	PTB2/AD10	KP_ROW2		
12	PTB3/AD11	KP_ROW3		
13	PTB4/AD12	KP_COL0		
14	PTB5/AD13	KP_COL1		
15	PTB6/AD14	KP_COL2		
16	PTB7/AD15	KP_COL3		
17	PTC0/AD16	SW_3V3 enable		
18	PTC1/AD17	SW_1V5 enable		
19	PTC2/AD18	MUX3_CTR		
20	PTC3/AD19	MUX4_CTR		
21	PTC4/AD20	MLB reset		
22	PTC5/AD21	MLB power down		
23	PTC6/AD22	WI-FI reset		
24	PTC7/AD23	BT reset		
25	PTD0	CAN transceiver power down		
26	PTD1	FM reset		
27	PTD2	FM and GPS 32K clock enable		
28	PTD3	GPS interrupt		
29	PTD4	SD1 plug in detect		

30	PTD5	SD1 write protect		
31	PTD6	SD2 plug in detect		
32	PTD7	SD2 write protect		
33	PTE0/TXD1	Reserved		
34	PTE1/RXD1	Reserved		
35	PTE2	Fast Ethernet enable		
36	PTE3	CMOS Sensor reset		
37	PTE4	CMOS Sensor power down control		
38	PTE5	GPS power enable		
39	PTE6	GPS reset		
40	PTE7	Speaker power down		
41	PTF0	LCD power down		
42	PTF1	WI-FI power down		
43	PTF2	I2C clock		
44	PTF3	I2C data		
45	PTF4	MUX1		
46	PTF5	HDD power down		
47	PTF6	HDD buffer enable		
48	PTF7	Fast Ethernet reset		
49	PTG0	32K crystal		
50	PTG1	32K crystal		
51	PTG2	Reserved		
52	PTG3	LCD reset		
53	PTG4	FM reset		
54	PTG5	FM CLK enable		

Chapter 4
Connectors and Signals

This chapter provides connector pin assignments and signals for i.MX35 3-Stack CPU, Personality, and Debug boards.

- The tables in this section list signal names as they appear in the board schematics.
- The use of "_B" at the end of a name indicates an active low signal.

4.1 500 Pin Board to Board Connector

Table 4-1 500 Pins Connector Pin-Out

	Row A	Row B	Row C	Row D	Row E
1	GND	USB_5V_VBUS	GND	CURRENT_MEAS_1	AUDIO_LIN_R
2	LI_BATTERY	USB_5V_VBUS	VMAIN	CURRENT_MEAS_2	RFU
3	LI_BATTERY	GND	VMAIN	GND	MIC_IN_P
4	GND	3V3	GND	CURRENT_MEAS_3	MIC_BIAS
5	1V8	3V3	1V3	CURRENT_MEAS_4	HEADPHONE_DETECT
6	1V8	GND	1V5	GND	ADC_1
7	GND	WALL_5V_IN	1V5	CURRENT_MEAS_5	ADC_2
8	LCD_BKLT_18MA_RETURN	WALL_5V_IN	GND	CURRENT_MEAS_6	GND
9	LCD_BKLT_18MA_BOOST	GND	LINEAR_D	GND	ADC_3
10	BKLT_5V_60MA_A	2V775	3V	CURRENT_MEAS_7	ADC_4
11	BKLT_5V_60MA_K	2V775	3V	CURRENT_MEAS_8	ADC_5
12	DEBUG_INT_B	RFU	SLEEP_VSTBY	CURRENT_MEAS_9	ADC_6
13	MASTER_RESET_B	RFU	GND	CURRENT_MEAS_10	GND
14	OSC_32KHz	BATTERY_TEMP	ON_OFF	PWR_EN	RFU
15	GND	OSC_26MHZ	LI_CELL	RFU	USB-HS-D0
16	UART3_RX	RFU	VDD_I2C_IO	VDD_USB_IO	USB-HS-D1
17	UART3_TX	RFU	I2C1_DATA	USB-HS_OC	USB-HS-D2
18	UART3_CTS	RFU	I2C1_CLOCK	USB-HS_RESET_B	USB-HS-D3
19	UART3_RTS	RFU	GND	HDD_PWR_EN	USB-HS_STP
20	UART2_RX	GND	I2C2_CLOCK	HDD_DMARQ	USB-HS-CLK
21	UART2_TX	RFU	I2C2_DATA	HDD_DIOW	GND
22	UART2_CTS	RFU	CSPI1_MOSI	HDD_DIOR	HDD_D0
23	UART2_RTS	DEBUG	GND	HDD_IORDY	HDD_D1
24	UART1_RX	PERSONALITY1	CSPI1_MISO	HDD_DMACK	HDD_D2
25	UART1_TX	PERSONALITY2	CSPI1_SS0	HDD_INTRQ	GND

26	UART1_CTS	PERSONALITY3	CSPI1_SS1	HDD_DA1	HDD_D3
27	UART1_RTS	CPU1	GND	HDD_DA0	HDD_D4
28	RFU	CPU2	CSPI1_SCLK	HDD_CS0	HDD_D5
29	VDD_LCDIO	CPU3	CSPI1_RDY	HDD_DA2	GND
30	LCD_SD_I	LCD_SD_DIO	LCD_DRDY0	HDD_CS1	HDD_D6
31	LCD_HSYNC	LCD_LSCLK_PLCK_FPSHIFT	GND	HDD_RESET_B	HDD_D7
32	LCD_VSYNC	LCD_RD	LCD_SER_RS_DEN	ATA_ENABLE_B	HDD_D8
33	LCD_LCS1_RST	LCD_WR	LCD_SD_CLK	ATA_DIR	GND
34	LCD_G-1	LCD_G-2	LCD_LCS0	RFU_LCD2	HDD_D9
35	LCD_R-1	LCD_R-2	LCD_VSYNC0	RFU_LCD2	HDD_D10
36	LCD_B-1	LCD_B-2	LCD_PAR_RS	RFU_LCD2	HDD_D11
37	LCD_B0_D0	LCD_CONTRAST	GND	RFU_LCD2	GND
38	LCD_B1_D1	LCD_CLS	RFU_LCD2	RFU_LCD2	HDD_D12
39	LCD_B2_D2	LCD_SPL_SPR	RFU_LCD2	RFU_LCD2	HDD_D13
40	GND	LCD_REV	RFU_LCD2	RFU_LCD2	HDD_D14
41	LCD__R5_D17	GND	RFU_LCD2	RFU_LCD2	GND
42	LCD_R3_D15	LCD_R4_D16	RFU_LCD2	RFU_LCD2	HDD_D15
43	LCD__R2_D14	RFU_LCD2/GND	RFU_LCD2	RFU_LCD2	VDD_HDD_IO
44	LCD_R0_D12	LCD_R1_D13	GND	RFU_LCD2	RFU_LCD2
45	LCD__G5_D11	RFU_LCD2/GND	RFU_LCD2	RFU_LCD2	GND
46	LCD_G3_D9	LCD__G4_D10	GND	RFU_LCD2	RFU_LCD2
47	LCD_G2_D8	RFU_LCD2/GND	RFU_LCD2	RFU_LCD2	GND
48	LCD_G0_D6	LCD_G1_D7	GND	RFU_LCD2	RFU_LCD2
49	LCD__B5_D5	RFU_LCD2/GND	RFU_LCD2	GND	GND
50	LCD_B3_D3	LCD_B4_D4	GND	USB_OTG_D_MINUS	USB_OTG_D_PLUS

Table 4.2 500 Pin Connector Signal Descriptions

Signal	Pin	Description
GND	A1, A4, A7, A15, A40, B3, B6, B9, B20, B41, C1, C4, C8, C13, C19, C23, C27, C31, C37, C44, C46, C48, C50, D3, D6, D9, D49, E8, E13, E21, E25, E29, E33, E37, E41, E45, E47, E49, F2, F14, F50, G6, H3, H6, H11, H15, H19, H23, H27, H31, H35, H40, H46, J3, J21, J25, K3, K14, K37	Signal Ground
LI_BATTERY	A2, A3	Li_battery interface
1V8	A5, A6	From Atlas SW2B, for peripheral devices use
LCD_BKLT_18MA_RETURN	A8	LCD backlight power return
LCD_BKLT_18MA_BOOST	A9	LCD backlight power
BKLT_5V_60MA_A	A10	5V, 60mA backlight drive Anode
BKLT_5V_60MA_K	A11	5V, 60mA backlight drive Negative
DEBUG_INT_B	A12	Debug board interrup
MASTER_RESET_B	A13	i.MX35 reset signal, low active, from reset button on Personality board or Debug board
OSC_32KHz	A14	32.768KHz frequency output
UART3_RX	A16	i.MX35 UART3 serial data receive
UART3_TX	A17	i.MX35 UART3 serial data transmi
UART3_CTS	A18	i.MX35 UART3 clear to send
UART3_RTS	A19	i.MX35 UART3 request to send
UART2_RX	A20	i.MX35 UART2 serial data receive
UART2_TX	A21	i.MX35 UART2 serial data transmit
UART2_CTS	A22	i.MX35 UART2 clear to send
UART2_RTS	A23	i.MX35 UART2 request to send
UART1_RX	A24	i.MX35 UART1 serial data receive
UART1_TX	A25	i.MX35 UART1 serial data transmit
UART1_CTS	A26	i.MX35 UART1 clear to send
UART1_RTS	A27	i.MX35 UART1 request to send
RFU	A28, B12, B13, B16, B17, B18, B19, B21, B22, D15, E2, A14, F2, F12, F13, F21, G7, G8, G9, G10, G11, H7, H8, H9, J13, K22,	Reserved for future use

Signal	Pin	Description
VDD_LCDIO	A29	LCD IO power supply
LCD_SD_I	A30	Data in for Serial Display, used for GPIO
LCD_HSYNC	A31	LCD Line sync
LCD_VSYNC	A32	LCD Vsync
LCD_LCS1_RST	A33	LCD module and TV-Out chip reset
LCD_G-1	A34	LCD data (for future use)
LCD_R-1	A35	LCD data (for future use)
LCD_B-1	A36	LCD data (for future use)
LCD_B0_D0	A37	LCD data0
LCD_B1_D1	A38	LCD data1
LCD_B2_D2	A39	LCD data2
LCD__R5_D17	A41	LCD data17
LCD_R3_D15	A42	LCD data15
LCD__R2_D14	A43	LCD data14
LCD_R0_D12	A44	LCD data12
LCD__G5_D11	A45	LCD data11
LCD_G3_D9	A46	LCD data9
LCD_G2_D8	A47	LCD data8
LCD_G0_D6	A48	LCD data6
LCD__B5_D5	A49	LCD data5
LCD_B3_D3	A50	LCD data3
USB_5V_VBUS	B1, B2	USB OTG 5V VBUS
3V3	B4, B5	3.3V power supply
WALL_5V_IN	B7, B8	DC 5.0V power supply
2V775	B10, B11	2.775V power supply
BATTERY_TEMP	B14	Battery temperature
DEBUG	B23	Debug board version code
PERSONALITY1	B24	Personality board version code

Signal	Pin	Description
PERSONALITY2	B25	Personality board version code
PERSONALITY3	B26	Personality board version code
CPU1	B27	CPU board version code
CPU2	B28	CPU board version code
CPU3	B29	CPU board version code
LCD_SD_DIO	B30	Data in/out for serial Display, can be used for GPIO
LCD_LSCLK_PLCK_FPSHIFT	B31	LCD shift
LCD_RD	B32	LCD Asynch. Port read
LCD_WR	B33	LCD Asynch. Port write
LCD_G-2	B34	LCD data (for future use)
LCD_R-2	B35	LCD data (for future use)
LCD_B-2	B36	LCD data (for future use)
LCD_CONTRAST	B37	LCD backlight contrast adjust
LCD_CLS	B38	LCD CLS
LCD_SPL_SPR	B39	LCD SPL
LCD_REV	B40	LCD REV
RFU_LCD2	B43, B45, B47, B49, C38, C39, C40, C41, C42, C43, C45, C47, C49, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, E44, E46, E48, F44, F45	Reserved for LCD future use
LCD_R4_D16	B42	LCD data16
LCD_R1_D13	B44	LCD data13
LCD__G4_D10	B46	LCD data10
LCD_G1_D7	B48	LCD data7
LCD_B4_D4	B50	LCD data4
VMAIN	C2, C3	Application power supply, from DC power or battery
LINEAR_A	C5	Linear regulator A
LINEAR_B	C6	Linear regulator B
LINEAR_C	C7	Linear regulator C

Signal	Pin	Description
LINEAR_D	C9	Linear regulator D
LINEAR_E	C10	Linear regulator E
LINEAR_F	C11	Linear regulator F
SLEEP_VSTBY	C12	Power management state retention
ON_OFF	C14	System On/Off signal
LI_CELL	C15	Coin cell battery
VDD_I2C_IO	C16	I2C power supply
I2C1_DATA	C17	I2C1 data
I2C1_CLOCK	C18	I2C2 clock
I2C2_CLOCK	C20	I2C2 clock
I2C2_DATA	C21	I2C1 data
CSPI1_MOSI	C22	CSPI1 Master out/ Slave in
CSPI1_MISO	C24	CSPI1 Master in/ Slave out
CSPI1_SS0	C25	CSPI1 Slave select 0
CSPI1_SS1	C26	CSPI1 Slave select 1
CSPI1_SCLK	C28	CSPI1 serial clock
CSPI1_RDY	C29	CSPI1 signal ready
LCD_DRDY0	C30	LCD DRDY/VLD
LCD_SER_RS_DEN	C32	Asynch.Serial Port data/comm, used for GPIO
LCD_SD_CLK	C33	Serial Display clock
LCD_LCS0	C34	Asynch. Port chip select
LCD_VSYNC0	C35	LCD frame sync
LCD_PAR_RS	C36	Asynch. Parallel Port data/comm
CURRENT_MEAS_1	D1	Current Measure 1 (SW1 in CPU board)
CURRENT_MEAS_2	D2	Current Measure 2 (SW2A in CPU board)
CURRENT_MEAS_3	D4	Current Measure 3 (VMAIN in CPU board)
CURRENT_MEAS_4	D5	Current Measure 4
CURRENT_MEAS_5	D7	Current Measure 5

Signal	Pin	Description
CURRENT_MEAS_6	D8	Current Measure 6 (EXT_1V8 in Personality board)
CURRENT_MEAS_7	D10	Current Measure 7 (HDD_3V3 in Personality board)
CURRENT_MEAS_8	D11	Current Measure 8 (DC power supply in Personality board)
CURRENT_MEAS_9	D12	Current Measure 9 (battery power supply in Personality board)
CURRENT_MEAS_10	D13	
PWR_EN	D14	Power enable, from Atlas GPO
VDD_USB_IO	D16	USB IO power supply
USB_HS_OC	D17	USB Host over current
USB-HS_RESET_B	D18	USB Host reset signal
HDD_PWR_EN	D19	HDD power enable
HDD_DMARQ	D20	HDD DMA signal request
HDD_DIOW	D21	HDD IO signal read
HDD_DIOR	D22	HDD IO signal write
HDD_IORDY	D23	HDD IO signal ready
HDD_DMACK	D24	HDD DMA signal accept
HDD_INTRQ	D25	HDD Interrupt signal request
HDD_DA1	D26	HDD register address 1
HDD_DA0	D27	HDD register address 0
HDD_CS0	D28	HDD Command Block Registers selection
HDD_DA2	D29	HDD register address 2
HDD_CS1	D30	HDD Control Block Registers selection
HDD_RESET_B	D31	HDD reset signal
ATA_ENABLE_B	D32	HDD buffer enable signal
ATA_DIR	D33	HDD buffer direction signal
USB_OTG_D_MINUS	D50	USB OTG data minus
AUDIO_LIN_R	E1	Audio Line in right
MIC_IN_P	E3	Microphone amplifier input

Signal	Pin	Description
MIC_BIAS	E4	Microphone supply output with integrated bias resistor and detect
HEADPHONE_DETECT	E5	Headphone insert detect
ADC_1	E6	ADC input 1(NC for i.MX35)
ADC_2	E7	ADC input 2 (NC for i.MX35)
ADC_3	E9	ADC input 3(NC for i.MX35)
ADC_4	E10	ADC input 4(NC for i.MX35)
ADC_5	E11	ADC input 5(NC for i.MX35)
ADC_6	E12	ADC input 6(NC for i.MX35)
USB-HS-D0	E15	USB Host Data 0
USB-HS-D1	E16	USB Host Data 1
USB-HS-D2	E17	USB Host Data 2
USB-HS-D3	E18	USB Host Data 3
USB-HS_STP	E19	USB Host ULPI Stop signal
USB-HS-CLK	E20	USB Host ULPI Clock
HDD_D0	E22	HDD Data 0
HDD_D1	E23	HDD Data 1
HDD_D2	E24	HDD Data 2
HDD_D3	E26	HDD Data 3
HDD_D4	E27	HDD Data 4
HDD_D5	E28	HDD Data 5
HDD_D6	E30	HDD Data 6
HDD_D7	E31	HDD Data 7
HDD_D8	E32	HDD Data 8
HDD_D9	E34	HDD Data 9
HDD_D10	E35	HDD Data 10
HDD_D11	E36	HDD Data 11
HDD_D12	E38	HDD Data 12
HDD_D13	E39	HDD Data 13

Signal	Pin	Description
HDD_D14	E40	HDD Data 14
HDD_D15	E42	HDD Data 15
VDD_HDD_IO	E43	HDD IO Power supply
USB_OTG_D_PLUS	E50	USB OTG data plus
AUDIO_LIN_L	F1	Audio Line in left
BOOTSTRAP_0	F4	Boot Strap 0
BOOTSTRAP_1	F5	Boot Strap 1
BOOTSTRAP_2	F6	Boot Strap 2
BOOTSTRAP_3	F7	Boot Strap 3
BOOTSTRAP_4	F8	Boot Strap 4
BOOTSTRAP_5	F9	Boot Strap 5
VDD_BOOTSTRAP	F10	Boot Strap Power supply
DAC	F11	DAC
USB-HS-D4	F15	USB Host Data 4
USB-HS-D5	F16	USB Host Data 5
USB-HS-D6	F17	USB Host Data 6
USB-HS-D7	F18	USB Host Data 7
USB-HS_NXT	F19	USB Host ULPI Next signal
USB-HS_DIR	F20	USB Host ULPI Direction signal
FEC_TXD2	F22	FEC interface
FEC_TXD3	F23	FEC interface
FEC_RX_ER	F24	FEC interface
FEC_TXD0	F25	FEC interface
FEC_RXD1	F26	FEC interface
FEC_RXD2	F27	FEC interface
FEC_RXD3	F28	FEC interface
FEC_TXD1	F29	FEC interface
FEC_MDIO	F30	FEC interface

Signal	Pin	Description
FEC_MDC	F31	FEC interface
FEC_CRS	F32	FEC interface
FEC_INT_B	F33	FEC interface
FEC_TX_CLK	F34	FEC interface
FEC_RXD0	F35	FEC interface
FEC_RX_DV	F36	FEC interface
FEC_RESET_B	F37	FEC interface
FEC_RX_CLK	F38	FEC interface
FEC_COL	F39	FEC interface
FEC_TX_ER	F40	FEC interface
FEC_ENABLE	F41	FEC interface
FEC_TX_EN	F42	FEC interface
VDD_FEC_IO	F43	FEC interface
EB0	F46	LSB Byte strobe WEIM data enable; Controls d[7:0]
1_WIRE_DATA	F47	1 Wire data
LBA	F48	WEIM load base address
USB_OTG_UID	F49	USB OTG ID signal
AUDIO_LOUT_R	G1	Audio Line out right
HEADPHONE_RIGHT	G2	Headphone right
HEADPHONE_RETURN	G3	Headphone return(Connect with GND)
SPEAKER_RIGHT_P	G4	Handset loudspeaker and alert amplifier positive terminal
SPEAKER_RIGHT_N	G5	Handset loudspeaker and alert amplifier minus terminal
CSI_RESET_B	G12	Camera sensor reset signal
CSI_PWDN	G13	Camera sensor power down
KP_ROW_7	G14	Keypad row 7
KP_ROW_6	G15	Keypad row 6
KP_ROW_5	G16	Keypad row 5
KP_ROW_4	G17	Keypad row 4

Signal	Pin	Description
KP_ROW_3	G18	Keypad row 3
KP_ROW_2	G19	Keypad row 2
KP_ROW_1	G20	Keypad row 1
KP_ROW_0	G21	Keypad row 0
KP_COL_7	G22	Keypad column 7
KP_COL_6	G23	Keypad column 6
KP_COL_5	G24	Keypad column 5
KP_COL_4	G25	Keypad column 4
KP_COL_3	G26	Keypad column 3
KP_COL_2	G27	Keypad column 2
KP_COL_1	G28	Keypad column 1
KP_COL_0	G29	Keypad column 0
GPIO 1V8	G30	GPS Interrupt
GPIO 1V8	G31	Accelerometer interrupt 1
GPIO 1V8	G32	Accelerometer interrupt 2
GPIO 1V8	G33	FM reset signal, low active
GPIO 1V8	G34	FM clock enable
OSC_CLKO	G35	i.MX35 clock out
D14	G36	EIM data 14
D12	G37	EIM data 12
D10	G38	EIM data 10
D8	G39	EIM data 8
VDD_EIM_DATA	G40	EIM data power supply
D6	G41	EIM data 6
D4	G42	EIM data 4
D2	G43	EIM data 3
D0	G44	EIM data 2
ECB_WAIT	G45	End Current burst

Signal	Pin	Description
EB1	G46	LSB Byte strobe WEIM data enable; Controls D[15:8]
OE_B	G47	Memory output enable
CS4_B	G48	Chip select 4
CS2_B	G49	Chip select 2/ SDRAM sync flash chip select
CS0_B	G50	Chip select 0
AUDIO_LOUT_L	H1	Audio Line out Left
HEADPHONE_LEFT	H2	Headphone Left
SPEAKER_LEFT_P	H4	Handset earpiece speaker amplifier output positive terminal
SPEAKER_LEFT_N	H5	Handset earpiece speaker amplifier output minus terminal
VDD_CSI_IO	H10	Camera sensor power supply
CSI_HSYNC	H12	Camera sensor horizontal Sync
CSI_VSYNC	H13	Camera sensor vertical Sync
CSI_MCLK	H14	Camera sensor master clock
CSI_PIXCLK	H16	Camera sensor data latch clock
CSI_D0	H17	Camera sensor data 0
CSI_D1	H18	Camera sensor data 1
CSI_D2	H20	Camera sensor data 2
CSI_D3	H21	Camera sensor data 3
CSI_D4	H22	Camera sensor data 4
CSI_D5	H24	Camera sensor data 5
CSI_D6	H25	Camera sensor data 6
CSI_D7	H26	Camera sensor data 7
CSI_D8	H28	Camera sensor data 8
CSI_D9(MSB)	H29	Camera sensor data 9
GPIO 1V8	H30	GPS module power enable
GPIO 1V8	H32	GPS reset, active low
GPIO 1V8	H33	Wi-Fi reset, active low
GPIO 1V8	H34	Bluetooth reset, active low

Signal	Pin	Description
D15	H36	EIM data 15
D13	H37	EIM data 13
D11	H38	EIM data 11
D9	H39	EIM data 9
D7	H41	EIM data 7
D5	H42	EIM data 5
D3	H43	EIM data 3
D1	H44	EIM data 1
BCLK	H45	EIM burst clock
RW_B	H47	EIM read/write signal
CS5_B	H48	Chip select 5
CS3_B	H49	Chip select 3
CS1_B	H50	Chip select 1
TOUCH_X0	J1	Touch screen X0
TOUCH_X1	J2	Touch screen X1
TV_DAC_C_RETURN	J4	TV DAC return (reserved for future use)
TV_DAC_B_RETURN	J5	TV DAC return (reserved for future use)
TV_DAC_A_RETURN	J6	TV DAC return (reserved for future use)
SIM_CLK	J7	Sim card interface (reserved for future use)
SIM_RST	J8	Sim card interface (reserved for future use)
SIM_VEN	J9	Sim card interface (reserved for future use)
VDD_SIM_IO	J10	Sim card power supply
CHRG_LED	J11	Charge LED
VDD_JTAG	J12	JTAG power supply
CPLD_PGM_TDI	J14	CPLD JTAG interface (Reserved for future use)
CPLD_PGM_TDO	J15	CPLD JTAG interface (Reserved for future use)
CPLD_PGM_TMS	J16	CPLD JTAG interface (Reserved for future use)
CPLD_PGM_TCK	J17	CPLD JTAG interface (Reserved for future use)

Signal	Pin	Description
SSI1_STXD	J18	SSI1 interface TxD signal
SSI1_SRXD	J19	SSI1 interface RxD Signal
SSI1_SFS	J20	SSI1 interface Frame Sync
SSI1_SCK	J22	SSI1 interface Serial Clock
SSI2_STXD	J23	SSI2 interface TxD signal
SSI2_SRXD	J24	SSI2 interface RxD Signal
SSI2_SFS	J26	SSI2 interface Frame Sync
SSI2_SCK	J27	SSI2 interface Serial Clock
SD1_D0	J28	SD card 1 data 0
SD1_D1	J29	SD card 1 data 1
SD1_D2	J30	SD card 1 data 2
SD1_D3	J31	SD card 1 data 3
VDD_SD2_IO	J32	SD card 2 power supply
SD2_D0	J33	SD card 2 data 0
SD2_D1	J34	SD card 2 data 1
SD2_D2	J35	SD card 2 data 2
SD2_D3	J36	SD card 2 data 3
VDD_EIM_ADDR	J37	EIM address power supply
A24	J38	EIM address 24
A22	J39	EIM address 22
A20	J40	EIM address 20
A18	J41	EIM address 18
A16	J42	EIM address 16
A14	J43	EIM address 14
A12	J44	EIM address 12
A10	J45	EIM address 10
A8	J46	EIM address 8
A6	J47	EIM address 6

Signal	Pin	Description
A4	J48	EIM address 4
A2	J49	EIM address 2
A0	J50	EIM address 0
TOUCH_Y0	K1	Touch screen Y0
TOUCH_Y1	K2	Touch screen Y1
TV_DAC_C	K4	TV DAC (reserved for future use)
TV_DAC_B	K5	TV DAC (reserved for future use)
TV_DAC_A	K6	TV DAC (reserved for future use)
SIM_RX	K7	Sim card interface (reserved for future use)
SIM_PD	K8	Sim card interface (reserved for future use)
SIM_TX	K9	Sim card interface (reserved for future use)
JTAG_TRST_B	K10	JTAG TAP Reset
JTAG_TDI	K11	JTAG TAP Data In
JTAG_TMS	K12	JTAG TAP Mode select
JTAG_TCK	K13	JTAG TAP clock
JTAG_RTCK	K15	JTAG ARM Debug Test Clock
JTAG_DE_B	K16	JTAG Debug Enable
JTAG_TDO	K17	JTAG TAP data out
JTAG_RESET_B	K18	JTAG reset signal
MLB_SIG	K19	Reserved for Future use
MLB_DAT	K20	Reserved for Future use
MLB_CLK	K21	Reserved for Future use
CAN TX1 RFU	K23	Reserved for Future use
CAN RX1 RFU	K24	Reserved for Future use
CAN TX2 RFU	K25	Reserved for Future use
CAN RX2 RFU	K26	Reserved for Future use
VDD_MLB	K27	Reserved for Future use
SD1_CMD	K28	SD card 1 Command signal

Signal	Pin	Description
SD1_DET	K29	SD card 1 Detect signal
SD1_WP	K30	SD card 1 write protect
SD1_CLK	K31	SD card 1 clock signal
VDD_SD1_IO	K32	SD card 1 power supply
SD2_CMD	K33	SD card 2 Command signal
SD2_DET	K34	SD card 2 Detect signal
SD2_WP	K35	SD card 2 write protect
SD2_CLK	K36	SD card 2 clock signal
A25	K38	EIM Address 25
A23	K39	EIM Address 23
A21	K40	EIM Address 21
A19	K41	EIM Address 19
A17	K42	EIM Address 17
A15	K43	EIM Address 15
A13	K44	EIM Address 13
A11	K45	EIM Address 11
A9	K46	EIM Address 9
A7	K47	EIM Address 7
A5	K48	EIM Address 5
A3	K49	EIM Address 3
A1	K50	EIM Address 1

4.2 TV-In Jack and Audio-In Jack

Figure 4-1 illustrates the jacks.

Jack J20 (left, two holes) is the audio jack, where:

- White = left audio
- Red = right audio

Jack J21 (right, three holes) is the TV in Jack. The holes correspond to the Y Pr Pb TV in signals, where:

- Red = Pr signal
- Blue – Pb signal
- Green = Y signal

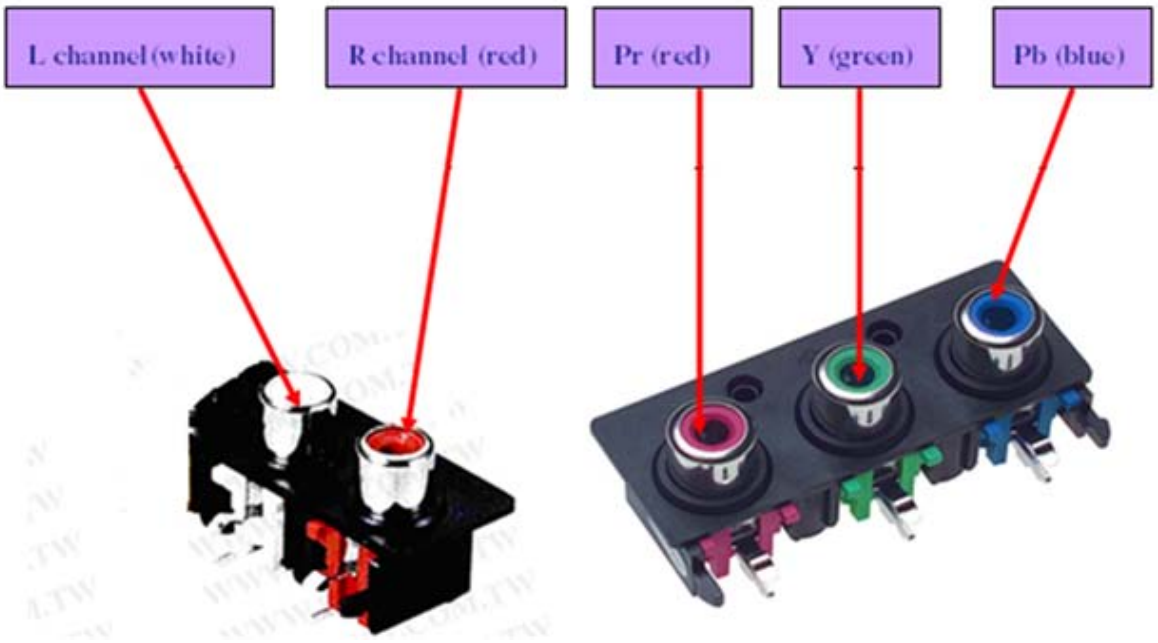

Figure 4-1 TV-In and Audio-In Jacks

4.3 LCD Connector

On the Personality board, J14 is the connector to the CPT 7 WVGA TFT Display CLAA070VC01. Table 4.3 provides the pin information, where the column abbreviations are as follows:

`I=input pin, O=output pin, R=reference pin, P=power supply pin, NC = not connected`

Table 4.3 LCD Connector Pin-Out

Pin No.	Symbol	Function	I/O	Remarks
1	YU	Y-Top	R	Touch Panel
2	XR	X_Right	R	Touch Panel
3	YD	Y_Bottom	R	Touch Panel
4	XL	X_Left	R	Touch Panel
5	GND	Ground	P	
6	GND	Ground	P	
7	VSYNC	Vertical Synchronous Signal	I	Display Interface
8	HSYNC	Horizontal Synchronous Signal	I	Display Interface
9	DE	Data Enable Signal	I	Display Interface
10	GND	Ground	P	
11	PCLK	Data Clock	I	Display Interface
12	GND	Ground	P	
13	B0	Display Data	I	Blue Data LSB
14	B1	Display Data	I	Blue Data
15	B2	Display Data	I	Blue Data
16	B3	Display Data	I	Blue Data
17	B4	Display Data	I	Blue Data
18	B5	Display Data	I	Blue Data MSB
19	GND	Ground	P	
20	G0	Display Data	I	Green Data LSB
21	G1	Display Data	I	Green Data
22	G2	Display Data	I	Green Data
23	G3	Display Data	I	Green Data
24	G4	Display Data	I	Green Data
25	G5	Display Data	I	Green Data MSB
26	GND	Ground	P	

Pin No.	Symbol	Function	I/O	Remarks
27	R0	Display Data	I	Red Data LSB
28	R1	Display Data	I	Red Data
29	R2	Display Data	I	Red Data
30	R3	Display Data	I	Red Data
31	R4	Display Data	I	Red Data
32	R5	Display Data	I	Red Data MSB
33	GND	Ground	P	
34	XRESET	Reset	I	L: Reset Active
35	XCS	Chip Select	I	I: Chip Select Active
36	SCLK	Serial Clock	I	Command Interface
37	DIN	Serial Data	I	Command Interface
38	NC		N.C.	not connected
39	GND	Ground	P	
40	VDDI	VDDI	P	1.8 volts
41	VDDI	VDDI	P	1.8 volts
42	VDD	VDD	P	2.8 volts
43	VDD	VDD	P	2.8 volts
44	LED_K	LED Cathode	P	Cathode
45	LED_A	LED Anode	P	Anode

Chapter 5
i.MX35 PDK Hardware Release Notes

This release of the i.MX35 3-Stack provides four multiplexing control signals. Table 5.1 describes the signal settings and functionality.

Table 5.1 Multiplexing Control Signals

Signal	Setting	Function	Description
MUX1_CTR Controls the gating of SS5 and SPDF function.	0	SS5 is used as SS5	SSI5TXD,SSI5RXD and SSI5CLK from SSI5 is used as the SSI5 function
	1	SS5 is used as SPDF	SSI5TXD,SSI5RXD and SSI5CLK from SSI5 is used as the SPDF_IN ,SPDF_OUT and SPDF_CLK of SPDF
MUX2_CTR Controls the gating of FEC and UART3 function.	0	FEC is used as UART3 on the GPS module	FEC_TXCLK,FEC_RXCLK,FEC_RXDV and FEC_COL from FEC is used as the RX,TX,CTS and RTS of UART3
	1	FEC is used as FEC	FEC_TXCLK,FEC_RXCLK,FEC_RXDV and FEC_COL from FEC is used as the FEC function
MUX3_CTR Controls the gating of BT USB interface and USB HOST	0	USB_FS is used as USB HOST	USB_FS_D_MINUS and USB_FS_D_PLUS from USB FS is used as the USB HOST function
	1	USB_FS is used as Bluetooth USB interface	USB_FS_D_MINUS and USB_FS_D_PLUS from USB FS is used as the Bluetooth USB interface
MUX4_CTR Controls the gating of WI-FI SD interface and 8 bit SD1 function	0	SD2 is used as a Wi-Fi SD interface	SD2_D0,SD2_D1, SD2_CLK and SD2_CMD from SD2 is used as the Wi-Fi SD interface
	1	SD2 is used as SD1 (8 bit)	SD2_D0,SD2_D1, SD2_CLK and SD2_CMD from SD2 is used as the high 4 bits of the 8 bit SD1 function