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User Manual for NXP Real Time Clocks PCF85x3, PCF85x63, PCA8565, PCF2123, and PCA21125

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Document information

Info	Content
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Abstract	This user manual aims to assist a user of above mentioned Real Time Clocks in achieving successful design-in and application. It contains useful hints with respect to electrical schematic and PCB layout as well as code examples for the well-established NXP PCF8563 and related Real Time Clocks. Also the more recent Real Time Clocks PCF2123 and PCA21125 have been taken into account.

Revision history

Rev	Date	Description
2.1	20150723	Fixed readability issue with certain browsers for Fig 9
2	20150717	Second version. Updated section 6.2
01	20081223	Initial version. This application note / user manual is a complete update of a previous publication titled: “Application note for the Philips Real Time Clocks PCF8563,73,83,93” which did not have an official AN/UM number and is superseded by this document. The contents were revised with lots of additional information added and errors in the examples corrected. Additionally it includes information with respect to recently introduced RTCs.

Contact information

For more information, please visit: http://www.nxp.com

1. Introduction

The real time clocks from NXP (previously Philips Semiconductors) have a long tradition and are used in numerous application fields. Starting from applications like VCR, they have been used in a wide variety of products like burglar alarm systems, water sprinklers, (platform) timers, e-metering, time-and-attendance monitoring, building access control, Point-of-Sale terminals, industrial applications, cars and trucks, telecom applications such as mobile phones and in gaming machines. In those applications they are used for functions like keeping calendar time, tariff switching, watch-dog, time stamping or waking up a system periodically to initiate certain actions, for example making measurements.

This application note deals with the PCF85x3 family with focus on the PCF8563, and with the more recent additions to the NXP RTC portfolio PCF2123 and PCA21125. The PCF2123 is an extremely low power RTC which allows fine tuning of the clock using an offset register (electronic tuning). PCA21125 is targeted at automotive applications. Where appropriate, comparisons to other devices are made.

PCF2120 is a low power 32.768 kHz oscillator with two integrated oscillator capacitances and a CLKOUT pin (32.768 kHz only), but without time, date and configuration registers. This application note is valid for the PCF2120 as well, particularly information with respect to oscillator, crystal, crystal and capacitor selection and layout guidelines.

Chapters 2 and 3 describe the features of these RTCs and include a comparison of the various types. Starting from chapter 4 more technical details are described that need to be understood in order to achieve successful application of these real time clocks. Chapters 4 and 5 deal with the power-on reset and voltage-low detection. Chapters 6 through 10 deal with the heart of the RTC; the oscillator, the crystal, crystal and capacitor selection, accuracy and oscillator tuning. Chapter 11 contains a description of how century change, leap years and daylight savings time is handled or needs to be handled in an application. This is followed by some examples in chapter 12 about how to initialize the RTC and how to set alarm and timer. Providing backup power when the rest of the system is not powered is covered in chapter 13. In order to make a reliable and accurate application it is important that the PCB layout is designed carefully and guidelines to achieve this are listed in chapter 14. This is followed by some further design tips in chapters 15 and 16 about partial circuit switch down and low power consumption.

Sometimes a component behaves different from what one may initially expect. This does not imply that it behaves wrongly, but in order to properly deal with it, it is important to be aware of such behavior. Chapter 17 describes how inaccurate timer performance can be avoided. Chapter 18 explains why the RTC will lose time if I^2C and SPI read and write operations are not finalized within one second of initiating it.

The application note is concluded with a short chapter on trouble shooting.

2. Features

The NXP real-time clock portfolio includes types for low power, types for automotive and other high temperature applications and applications that need additional RAM. A third family of highly accurate temperature compensated real time clocks will be dealt with in a separate application note. Designed for a range of demanding applications, these real-time clocks/calendars are driven by a low-power 32.768 kHz quartz oscillator, use the SPI or I^2C-bus for serial data transfer, and typically consume less than 1 µW of power.

Key features

- Oscillator requires 32.768 kHz external quartz crystal
- Resolution: seconds, minutes, hours, weekday, day, month, and year in 12- or 24-hour (military) format. All time and alarm registers are in BCD format. Two types include a $1/10^{th}$ and $1/100^{th}$ second resolution register
- Clock operating voltage: 1.0 V to 5.5 V or wider, see Table 2
- Low backup current: Ranging from 100 nA to 2 µA at V_{DD} = 1 V and T_{amb} = 25 °C
- Three line SPI with separate I/O or I^2C serial interface
- Freely programmable timer and alarm functions, each with interrupt capability
- Freely programmable Watchdog timer
- Programmable clock output for peripheral devices: 32.768 kHz, 1024 Hz, 32 Hz and 1 Hz (not all types)
- One or two integrated oscillator capacitors (connected to the output of amplifier OSCO in case of only one integrated capacitor)
- Internal power-on reset
- Open-drain interrupt pin
- Wide variety of packages available including naked die

Addresses and data are transferred serially via an SPI bus with a maximum speed of 7.0 Mbps (PCF2123, PCA21125) or via a two-line, bidirectional I^2C-bus that operates at a maximum speed of 400 kbps (Fast-Mode, PCF8563 and PCA8565) or 100 kbps (Standard-Mode, PCF8583 and PCF8593). The built-in word address register is incremented automatically after each data byte is written or read.

With the PCF8583, the address pin A0 is used to program the software address, so that two devices can be connected to the same I^2C-bus without additional hardware.

Each RTC has an internal power-on reset and a programmable clock output with open drain configuration to drive peripheral devices. A low voltage detector (not included on the PCF8583,93 and PCA21125) warns if the integrity of all clock functions is no longer guaranteed.

Power consumption is kept to a minimum in all the devices. The PCF2123 and PCF8563, optimized for battery-powered applications, consume as little as 100 nA at 2 V and 250 nA at 1 V respectively. With careful selection of the crystal used, the PCF2123 consumes less than 100 nA on a 1.5 V supply.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in Binary Coded Decimal (BCD) format. This format is popular with RTCs for the reason that time and date in BCD format can easily be displayed in human-readable style without conversion.

In BCD every digit of the decimal system is represented by a 4-bit group. For example: 157_{10} = 0001 0101 0111_{BCD}

This is not the same as binary representation. It is clear that BCD is not the most efficient way of coding since every 4-bit group (nibble) could represent numbers 0 through 15, but in BCD never represents numbers bigger than 9. But for some applications it is convenient to use BCD and real time clocks are one such application.

Each 8-bit register contains two digits each represented by one nibble. Each 4-bit nibble can represent the value of 0 up to 9 in BCD, but for some digits the maximum value to be represented will be lower. The minute register for example will never have to count higher than 59. The upper most digit can here be represented by 3 bits, freeing up one bit that can be used to indicate something else.

Not all NXP real-time clocks have exactly the same register implementation and thus the datasheet of the particular device should be consulted. As an example the register organization of the PCF8563 is given below. Note that this is just one example and that register organization of other types is not necessarily exactly the same.

Table 1. Register overview PCF8563

Bit positions labelled as x are not implemented. When setting a register, also a value must be written for the 'x' bit positions. When these are read back, the read back values may differ from what was previously written.
Bit positions labelled with 0 should always be written with logic 0; if read they could be either logic 0 or logic 1.

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00_{HEX}	control / status 1	TEST1	0	STOP	0	TESTC	0	0	0
01_{HEX}	control / status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
02_{HEX}	seconds	VL	<seconds 00 to 59 coded in BCD>						
03_{HEX}	minutes	x	<minutes 00 to 59 coded in BCD>						
04_{HEX}	hours	x	x	<hours 00 to 23 coded in BCD>					
05_{HEX}	days	x	x	<days 01 to 31 coded in BCD>					
06_{HEX}	weekdays	x	x	x	x	x	<weekdays 0 to 6>		
07_{HEX}	months / century	C	x	x	<months 01 to 12 coded in BCD>				
08_{HEX}	years	<years 00 to 99 coded in BCD>							
09_{HEX}	minute alarm	AE	<minute alarm 00 to 59 coded in BCD>						
$0A_{HEX}$	hour alarm	AE	x	<hour alarm 00 to 23 coded in BCD>					
$0B_{HEX}$	day alarm	AE	x	<day alarm 01 to 31 coded in BCD>					
$0C_{HEX}$	weekday alarm	AE	x	x	x	x	<weekday alarm 0 to 6>		
$0D_{HEX}$	CLKOUT control	FE	x	x	x	x	x	FD1	FD0
$0E_{HEX}$	timer control	TE	x	x	x	x	x	TD1	TD0
$0F_{HEX}$	timer	<timer countdown value>							

The PCA8565 and PCA21125 oscillators operate over a wider temperature range (up to 125 ºC) and are suitable for use in the harsh environments found within automobiles. Power consumption remains low — only 700 nA at 2 V. Serial interface is I^2C or SPI.

All the RTCs have ESD protection that exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115. Charge Device Model values vary from 500 V to 2000 V CDM per JESD22-C101. Refer to the datasheet of the respective device. Latch-up testing, performed in accordance with JEDEC Standard JESD78, exceeds 100 mA.

3. Comparison

Table 2 on the next page gives a quick overview of the features, specifications and differences between the RTCs dealt with in this User Manual. The PCF8573 which belongs to the PCF85x3 family is no longer in production and has thus not been included in the table. However, this user manual is useful for this type as well.

Further there are some derived types from the main types listed in the table with small differences in for example delivery form or the number of integrated oscillator capacitors. Consult NXP for more details.

3.1 Event counter mode

Two real time clocks, PCF8583 and PCF8593, have an extraordinary feature. It is the event counter mode which can be selected by setting the appropriate bits in the control register. In this mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This mode can be used to count pulses applied to the oscillator input OSCI. There is no crystal in the circuit and OSCO is left open circuit. The event counter stores up to 6 digits of data. Events are stored in BCD format. The 6 digits use three 8 bit registers (hundredth of a second, seconds, and minutes). D5 is the most significant and D0 the least significant digit. Every digit can contain values ranging from 0 to 9 and thus up to 999 999 events can be stored.

It is also possible to set an event counter alarm. When this function is enabled, the alarm occurs when the event counter registers match the programmed value. In this event the alarm flag is set. The inverted value of this flag can be transferred to the interrupt pin by setting the alarm interrupt enable in the alarm control register. In this mode the timer increments once for every one, one hundred, ten thousand or 1 million events, depending on the programmed value of the alarm control register. In all other events, the timer functions are as in clock mode.

Note that immediately following power-on, all internal registers are undefined and must be defined by software. It is also possible that upon power-on the device is initially in event-counter mode in which event the oscillator will not operate until the correct settings are written into the control registers.

The count value will increment on the falling edge. However, after a new count value has been programmed at least one rising edge must have occurred before events will be detected on the falling edge.

Table 2. Comparison of six real time clocks

Features	PCx85x3 family				PCx212x family	
	PCF8563	PCA8565	PCF8583	PCF8593	PCF2123	PCA21125
Unique features	Very low power consumption	AEC-Q100 automotive qualification	High resolution, RAM, event counter	High resolution, event counter	Extremely low power consumption, electronic tuning	AEC-Q100 automotive qualification
Type of interface	I^2C	I^2C	I^2C	I^2C	SPI	SPI
Interface bus speed	400 kHz	400 kHz	100 kHz	100 kHz	7 MHz	7 MHz
Scratch pad RAM	no	no	240 bytes	no	no	no
Year / leap year tracking	yes / yes	yes / yes	yes / yes	yes / yes	yes / yes	yes / yes
Year counter	2 digit + 1 century bit	2 digit + 1 century bit	2 bit (4 years)	2 bit (4 years)	2 digit (99 years)	2 digit (99 years)
100 ms, 10 ms time register	no	no	yes	yes	no	no
Electronic tuning register	no	no	no	no	yes	no
Programmable alarm and timer functions	yes	yes	yes	yes	yes	yes
Low voltage detector	yes	yes	no	no	yes	no
Event counter mode	no	no	yes	yes	no	no
Option to select between two I^2C addresses	no	no	yes	no	no	no
Integrated oscillator capacitor	1 at OSCO	1 at OSCO	1 at OSCO	1 at OSCO	2	1 at OSCO
Supply voltage range	1.8 V – 5.5 V	1.8 V – 5.5 V	2.5 V – 6.0 V	2.5 V – 6.0 V	1.6 V – 5.5 V	1.6 V – 5.5 V
Clock operating voltage	1.0 V – 5.5 V	1.8 V – 5.5 V	1.0 V – 6.0 V	1.0 V – 6.0 V	1.1 V – 5.5 V	1.3 V – 5.5 V
Typical current consumption	250 nA at V_{DD} = 1 V	650 nA at V_{DD} = 3 V	2 µA at V_{DD} = 1 V	1 µA at V_{DD} = 2 V	100 nA at V_{DD} = 2 V	550 nA at V_{DD} = 3 V
Operating temperature range	-40 °C to +85 °C	-40 °C to +125 °C	-40 °C to +85 °C	-40 °C to +85 °C	-40 °C to +85 °C	-40 °C to +125 °C
AEC-Q100 qualified	no	Yes (TSSOP8)	no	no	no	yes
Packages	U [1], DIP8, SO8, TSSOP8, HVSON10	TSSOP8, HVSON10	U [1], DIP8, SO8, HVQFN20	DIP8, SO8	U [1], HVQFN16, TSSOP14	TSSOP14

[1] Naked die

Some derived versions are available such as PCF8563A and PCA8565A which include two integrated oscillator capacitors and are also available as naked die.

4. Power-on reset (POR)

Traditionally a power-on reset circuit is a circuit that generates a reset pulse once the supply voltage has reached a certain value upon power-up. The purpose is to ensure a defined behavior at start-up. This type of power-on reset is not present in these RTCs.

The power-on reset circuit (POR) for these RTCs does not look at the supply voltage, but instead it is based on an internal reset circuit which is active whenever the oscillator is stopped, refer to Fig 1. When power is applied to the device it will take some time for the oscillator to start and during this time the circuit will generate a reset. Also when during operation the OSCI- or OSCO-pin is pulled to ground, causing oscillation to stop, the POR will generate a reset pulse. In the reset state the serial bus logic is initialized and all registers are reset according to the register reset values. Not all registers will be reset. The only registers that are reset are the ones that control a function i.e. decide on clock mode, enable an alarm etc. Refer to the datasheet of the respective device for details.

The power on reset duration is thus directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits on-board testing of the device would take longer too. In order to speed up this, a mechanism has been built in to disable the POR (not for PCF8583, PCF8593 and PCF2123). This is called Power-on reset override. Again, refer to the respective datasheet for details. Once the override mode has been entered, the device stops immediately being reset and set-up operation e.g. entry into the external clock test mode, may commence via the serial interface.

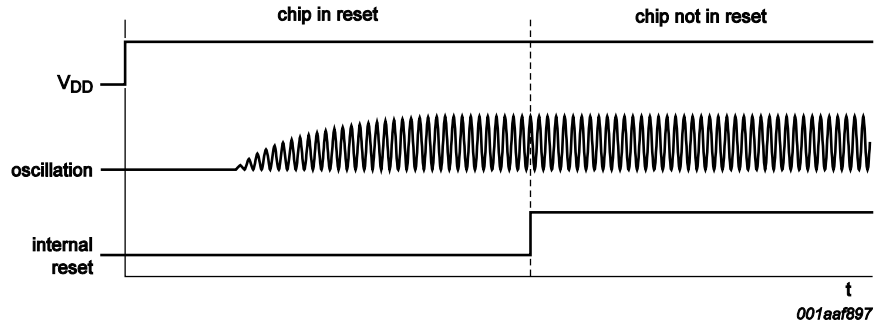


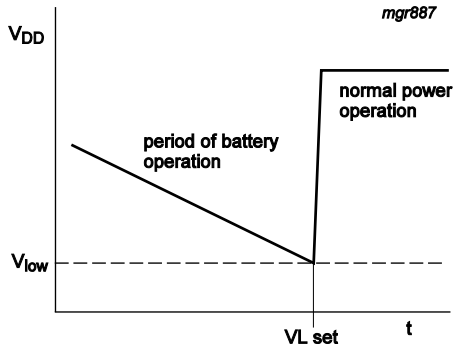
Fig 1. Power-on reset

5. Voltage-low detector

PCF8563, PCA8565 and PCF2123 have an on-chip voltage-low detector, see Fig 2 and Fig 3. When V_{DD} drops below a certain limit defined as V_{low}, bit VL in the seconds register of PCF8563 and PCA8565 is set. Generally the VL-bit is intended to indicate that the time might be wrong, not that it necessarily is wrong. It will be set if one of the following four conditions occur:

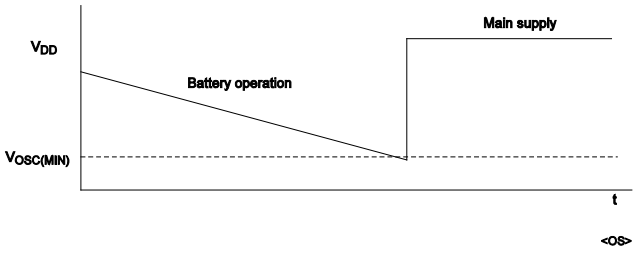
- The power has just been applied;
- The power has dipped down and then recovered;
- The power has gone away and then come back again;
- When the oscillator stops running.

The implementation in the PCF2123 is slightly different. There a bit OS (Oscillator Stopped) is present instead of VL. The OS flag is set whenever the oscillator is stopped, and therefore also when this is due to the supply voltage dropping too low. The flag can only be cleared by software and only if the oscillator is running again.



(1) Valid for PCF8563 and PCA8565

Fig 2. Voltage-low detection



(2) Valid for PCF2123

Fig 3. Oscillator-stop detection

In the case of PCF8563/PCA8565 bit VL set indicates that the integrity of the clock information is no longer guaranteed. If the oscillator hasn't stopped, the clock information will still be ok, but with V_{DD} having dropped below V_{low} there is no guarantee that this still is the case because there is no way to be sure that the oscillator kept running. The VL flag can only be cleared by software.

Both VL and OS are intended to detect the situation when V_{DD} is decreasing slowly, for example under battery operation. Should V_{DD} reach the limit where the flag is set before power is re-asserted, then the flag VL or OS will indicate that time may be (VL) or is (OS) corrupted. V_{DD} dropping below V_{low} or $V_{osc(min)}$ in itself does not cause any register to be reset. Once the oscillator stops some registers will be reset.

6. Oscillator

A crystal oscillator as used in a real-time clock, see Fig 4, is built on the principle of Pierce and uses an inverting amplifier with a crystal in the feedback path and load capacitors C_{IN} and C_{OUT} to provide the necessary additional phase shift. Some phase shift is contributed as a result of the amplifier's non-zero output impedance in combination with C_{OUT}. The oscillator operates at the frequency for which the crystal is anti-resonant (i.e. parallel resonant) with the total capacitive load of the oscillating circuit as seen from the pins of the crystal. This total capacitance is called the load capacitance.

The load capacitance is defined as the capacitance seen from the pins of the crystal and is formed by C_{IN}, C_{OUT} and C_{STRAY} indicated in Fig 4. Electrically the crystal's C_0 is also a load capacitance which affects oscillator characteristics. However, it is not part of the defined 'load capacitance'. During manufacturing the crystal is tuned to the specified frequency with a specified load capacitance connected to the crystal. Since C_0 is part of the crystal, it is automatically taken into account during the adjustment procedure.

C_{STRAY} is a result of parasitic capacitances due to PCB traces, IC pins etc. and is directly in parallel with C_0 of the crystal. In a practical situation care needs to be taken to keep these parasitic capacitances as low as possible since it will add to the load capacitance and this load capacitance must meet the specified value for the crystal that is being used. If the load capacitance presented to a crystal is smaller than what the crystal was designed for, the oscillation frequency will be too high and thus if used with an RTC, the clock will run too fast.

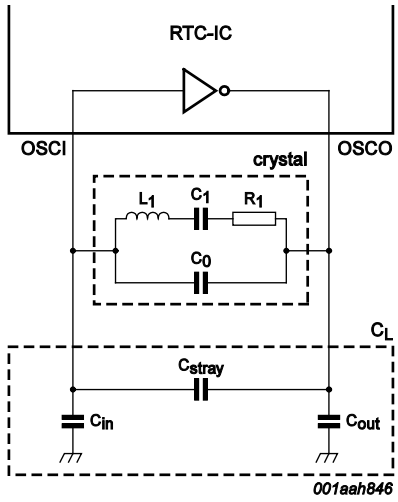


Fig 4. Pierce Oscillator equivalent diagram

The inverting amplifier (with feedback resistor, and drive resistor which are not included in Fig 4) is incorporated within the integrated circuit device. On the other hand, the quartz crystal is a discrete device external to the integrated circuit. In the PCF85x3, PCA8565 and PCF2123, PCA21125 the output capacitor C_{OUT} is integrated on the integrated circuit. PCF8563A, PCA8565A and PCF2123 also include C_{IN}, see Table 3 for overview.

Table 3. Overview of internal and external oscillator capacitors

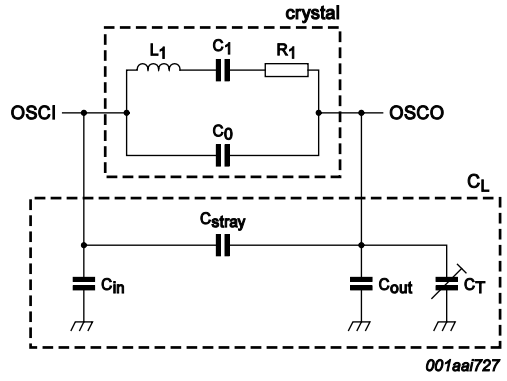
Features	PCx85x3 family				PCx212x family	
	PCF8563	PCA8565	PCF8583	PCF8593	PCF2123	PCA21125
Integrated oscillator capacitor	1 at OSCO	1 at OSCO	1 at OSCO	1 at OSCO	2	1 at OSCO
Targeted crystal load capacitance	12.5 pF	12. 5 pF	12.5 pF	12. 5 pF	7 pF [1]	12.5 pF
Value of integrated C_{IN}, typ.	-	-			14 pF	-
Value of integrated C_{OUT}, typ.	25 pF	25 pF	40 pF	25 pF	14 pF	25 pF
Theoretically required at pin OSCI	25 pF	25 pF	18 pF	25 pF	0 pF	25 pF

[1] Can be used with 9 pF and 12.5 pF as well if external capacitance is added

The values used in practice will be a bit smaller than the theoretically required values due to parasitic capacitances present in the application which add to the external physical capacitor.

For the PCF2123 the integrated C_{IN} and C_{OUT} are dimensioned for a crystal which requires a load capacitance of 7 pF. If a crystal with required load capacitance of 12.5 pF is used still a small external capacitor is required, otherwise the clock will run too fast. For the other types the input capacitor C_{IN} is external and needs to be mounted on the printed circuit board. The power consumed by the oscillator circuit is through the amplifier and losses in R_1 of the crystal. Oscillation will start if the loop gain at 360° phase shift is higher than one. The oscillator amplitude increases until the over-all loop gain is reduced to exactly 1 through either nonlinear effects of the amplifier (self-limiting Pierce) or through some form of AGC (Automatic Gain Control) designed in into the amplifier.

The resonating frequency can be pulled by changing the value of the capacitor at OSCI or by adding a variable capacitor C_T at OSCO as shown in Fig 5. External capacitors at OSCI and OSCO should be connected to GND, except for PCF8573, PCF8583 and PCF8593. For the latter three it is better to connect these external capacitors to V_{DD} instead because these devices are manufactured in a process that has the substrate connected to V_{DD} (n-substrate). In the other RTCs the substrate is at V_{SS} (p-substrate).



(1) For PCF8573, PCF8583 and PCF8593 connect C_{IN} and C_{OUT} (and C_T if applicable) to V_{DD}

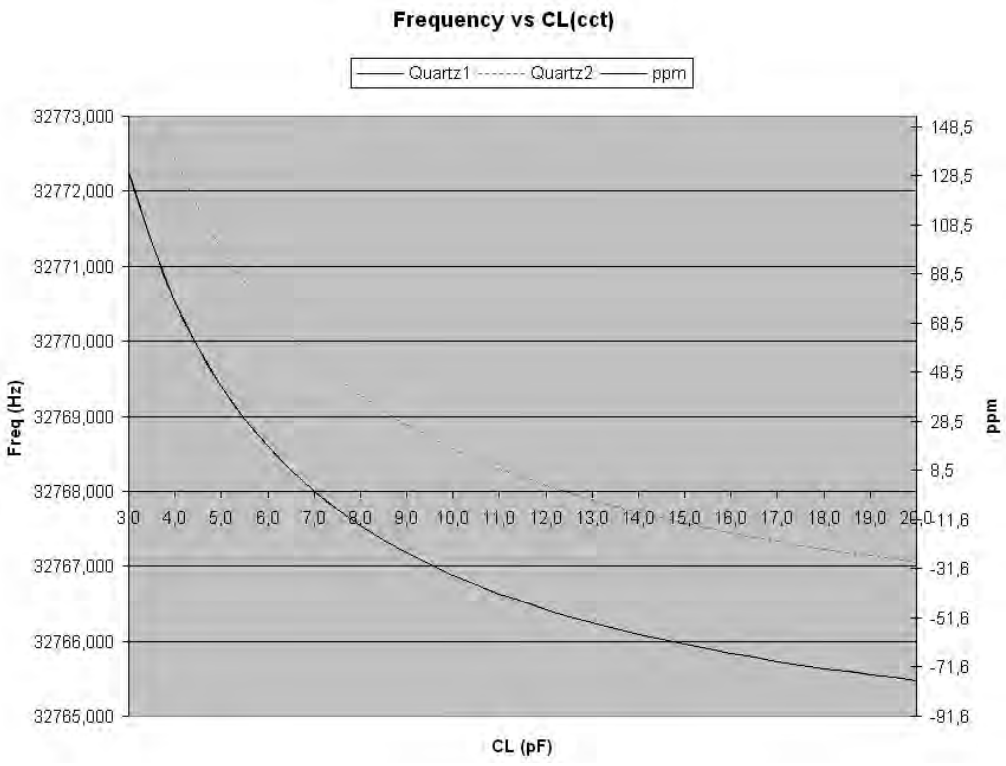
Fig 5. Oscillator frequency determining components

The reactive components indicated in Fig 4 and Fig 5 determine the oscillating frequency. Near the resonance frequency the equivalent circuit of the crystal consists of the motional inductance L_1, the motional capacitance C_1 and the motional resistance R_1 (in various literature also called series resistance R_S). In parallel with this series circuit is the static or shunt capacitance C_0. It is the sum of the capacitance between the electrodes and the capacitance added by the leads and mounting structure. If one were to measure the reactance of the crystal at a frequency far away from a resonance frequency, it is the reactance of this capacitance that would be measured.

When a crystal is chosen, such a crystal has a specified load capacitance C_L. During production the crystal manufacturer has adjusted the resonance frequency of the crystal using exactly this capacitance as the load for the crystal. The actual value of C_L as seen by the crystal in the application is determined by the external circuitry and parasitic capacitances. The external components of the oscillator have to be chosen such that the

actual value of C_L matches the specified value of C_L. If there is mismatch the crystal will not run exactly at its specified frequency resulting in the clock running slow or fast.

The crystal manufacturer can manufacture crystals for any load capacitance, but in practice some standard values are used. For use in real-time clocks you may find crystals specified for load capacitances of 7 pF, 9 pF and 12.5 pF with 12.5 pF the most common value.



(1) Frequency on the left scale and the equivalent deviation from the nominal frequency in ppm on the right scale

Fig 6. Graph of oscillator frequency as function of load capacitance C_L

Fig 6 depicts the influence of the load capacitance applied to the crystal on the oscillator frequency. The lower curve represents a crystal with a specified C_L of 7 pF, the upper curve represents a crystal with a specified C_L of 12 pF. From this graph it is obvious that the 7 pF crystal is more sensitive to deviations from the specified C_L. If the applied C_L is 1 pF lower than specified, the frequency deviation will be 18 ppm, whereas the 12.5 pF crystal will only show a frequency deviation of 6 ppm if the applied C_L is 1 pF below the specified value. This is not surprising since the same absolute change in load capacitance is a larger relative change if the load capacitance is smaller. A lower load capacitance however will result in lower power consumption and in cases where this is an important requirement a crystal with lower required C_L could be selected.

Now in order to determine the value of C_L resulting from C_{IN}, C_{OUT} (plus C_T if mounted) and C_{STRAY} it is necessary to realize that seen from the crystal, C_{IN} and C_{OUT} are

effectively in series; the 32 kHz signal goes from OSCI through C_{IN} to ground, via ground to C_{OUT} and then through C_{OUT} to OSCO. In parallel with this series circuit is C_{STRAY}. For the remainder of this discussion, whenever in formulas C_{OUT} is written this represents either the value of C_{OUT} only, or in case a trimming capacitor C_T is present too, the sum of C_{OUT} and C_T. Now the load capacitance C_L is given by:

$$C_L = \frac{C_{IN} \cdot C_{OUT}}{C_{IN} + C_{OUT}} + C_{STRAY}$$

Since C_0 is in parallel with C_L the total capacitance in parallel with the motional arm L_1-C_1-R_1 is given by

$$C_{PAR} = \frac{C_{IN} \cdot C_{OUT}}{C_{IN} + C_{OUT}} + C_{STRAY} + C_0$$

The motional arm is a series circuit, which forms a closed circuit because there is a capacitance C_{PAR} connected in parallel to this series circuit. Of course the crystal itself can't oscillate stand alone, but the equivalent capacitance C which determines together with L_1 the resulting resonance frequency is now given by the series circuit of C_{PAR} and C_1. Thus C is given by

$$C = \frac{C_1 \cdot \left\{ \frac{C_{IN} \cdot C_{OUT}}{C_{IN} + C_{OUT}} + C_{STRAY} + C_0 \right\}}{C_1 + \left\{ \frac{C_{IN} \cdot C_{OUT}}{C_{IN} + C_{OUT}} + C_{STRAY} + C_0 \right\}}$$

Typical values for crystal parameters are given in Table 4. From these values it is clear that C_1 is several orders of magnitudes smaller than the other capacitances in this expression and therefore C_1 dominates. C will be in the order of magnitude of C_1 but it will be a bit smaller as a result of C_{PAR} in series.

With $\omega = \frac{1}{\sqrt{LC}}$ and $Q = \frac{1}{\omega C} \cdot \frac{1}{R_1}$ the resulting resonance frequency and quality factor can be calculated.

Because C_1 is orders of magnitude smaller than the other capacitances Q can be approximated by

$$Q_a = \frac{1}{\omega C_1} \cdot \frac{1}{R_1}$$

Taking the numbers from Table 4 yields for L_1 and Q:

$$L_1 = \frac{1}{(2\pi \cdot f_0)^2 \cdot C_1} = \frac{1}{(2\pi \cdot 32768)^2 \cdot 2.1 \cdot 10^{-15}} = 11234\ H$$

$$Q = \frac{1}{(2\pi \cdot f_0) \cdot C_1 \cdot R_1} = \frac{1}{(2\pi \cdot 32768) \cdot 2.1 \cdot 10^{-15} \cdot 55 \cdot 10^3} = 42053$$

This L of around 11000 H resulting in a Q of around 42000 explains why starting up the oscillator as well as stopping it can easily take more than a second. An oscillating quartz crystal is actually a mechanical oscillation and starting or stopping this takes time. Calculations of startup time and more in-depth theory about the oscillator and load capacitance are beyond the scope of this user manual, but can be found in AN10716 “Background information and theory related to Real Time Clocks and crystals”.

The use of AGC’s improve start up by high drive initially to get it going and then reduce drive for low power.

Table 4. Typical values for crystal and surrounding capacitors

Parameter	Value	Unit	Source
f_0	32768	Hz	[2]
$\Delta f / f_0$	±100	ppm	[2]
Aging; $\Delta f / f_0$	±3…±5	ppm	[2]
B, freq(T)	-0.035	ppm / °C^2	[2]
C_1	2.1	fF	[2]
C_0	1.2…1.5	pF	[2]
C_{IN}	25 ± 10	pF	[1]
C_{IN}, temp co.	+47	ppm/°C	[1]
R_1	50…80	kΩ	[2]
C_T variable	4…25	pF	[3]
C_T, temp co.	300	ppm/°C	[3]
C_T fixed 0603	Any	pF	[4]
C_T fixed, tc	±30 for C0G	ppm/°C	[4]

Sources for values in table 4:

[1] NXP, Datasheet PCF8563, February 2008.

[2] Product Data Sheets, MicroCrystal.

[3] Murata TZB04 trim capacitor

[4] Vishay Beyschlag, datasheet ceramic multilayer capacitor, C0G

6.1 Oscillation allowance

Fig 4 shows the Pierce oscillator schematic with the external crystal. For an oscillation to take place the real component of the oscillator impedance has to be larger than the motional resistance R_1 (sometimes called R_S or ESR). If R_1 is too large no oscillation will take place since no operating point can be reached.

Similarly, if the supply voltage is too low or the temperature is too low, no oscillation can build up.

A method to test how much margin the design has is to include a resistor R_X in series with the crystal. The value of the resistor is changed (a trimmer is useful here) to see at which values of R_X oscillation starts and stops. Starting from a large value of R_X the resistance is lowered until oscillation starts. This value of R_X is called $R_{X\text{-start}}$. Now the value is increased again until oscillation stops, R_X is called $R_{X\text{-stop}}$.

The oscillation allowance OA is defined as:

$$OA = R_{X\text{-start}} + R_1$$

As a rule of thumb, the motional resistance of the crystal chosen should be

$$R_1 \leq \frac{OA}{5}$$

This test can be done in the lab under room temperature. This should give enough safety margins to allow for production spread of IC and crystal and to deal with the increasing value of R_1 under influence of increased temperature.

6.2 Using an external oscillator

It is possible to supply a clock signal from an external oscillator instead of using the internal oscillator if for some reason it is desired to not use the internal oscillator. In this case no crystal will be connected to the OSCI and OSCO pins. Instead, the external oscillator is connected to the OSCI pin while the OSCO pin must be left floating. The external oscillator should provide a signal with about 500 mV amplitude, swinging around a +250 mV bias (i.e. never going negative) as would be seen if the crystal was being used. These are general guidelines and some real time clocks require different input as discussed below. Additionally, values mentioned here are for guideline only and for every application correct operation must be verified.

6.2.1 RTC family PCF85x63, PCF8563, PCF8564A, PCA8565, PCF8523

A good starting point is to supply a signal with amplitude between 500 mV and 1000 mV, with the bias such that the signal doesn't go negative and operates in the same region as would have been the case with a crystal.

Suppose that amplitude of the external CLK is 5 V (from 0 V to 5 V). Using 1 M and 100 k resistors the signal could be reduced to (100 / 1100) x 5 V = 450 mV. This is better in line with the signals that the internal circuitry handles when an external crystal is used as is the case in the standard application. This reduced signal can then be applied to the OSCI

pin directly or via a small capacitor of e.g. 22 pF - 100 pF. Alternatively a capacitive divider circuit can be used to reduce the signal amplitude.

Either square or sine wave is ok.

6.2.2 PCF2123

As other RTCs, but the required amplitude should be somewhat smaller, around 300 mV.

6.2.3 PCF8583 and PCF8593

When used with a crystal the signal would swing around a bias about 100 mV below VDD. If these RTCs are fed with an external signal, it should be either AC coupled, or swinging with amplitude of around 1 V below VDD, where the lower value may be lower than 1 V below VDD.

7. Crystal and crystal selection

Select a crystal of the tuning fork type with a nominal frequency of 2^{15} Hz = 32768 Hz. The allowed tolerance depends on the requirements for the application and on whether a trimming capacitor will be used. If a trimming capacitor will be used even a tolerance of ±100 ppm is ok since it can be compensated. Either through hole or surface mount crystals can be used where the latter provide the smallest dimensions which makes the circuit less susceptible to noise pick up.

As previously pointed out crystals used for RTCs come in three versions, optimized for three standard values for C_L with 12.5 pF the most common. Generally, an RTC using a 12.5 pF crystal has a timekeeping current of about 1.6x more than an RTC using a 7 pF crystal. If lowest power consumption is a key consideration, a 7 pF crystal (some manufacturers use 6 pF) should be selected. The PCF2123 has been optimized for use with such a crystal. The other RTCs include load capacitance optimized for a 12.5 pF crystal. Using a 7 pF crystal would require an external capacitor of about 9.7 pF and thus the capacitances at OSCI and OSCO would not be balanced. In general this may have a detrimental influence on start-up behavior but no problems are expected when a 7 pF crystal is used in combination with the PCF8563 because it uses an AGC in its oscillator.

An oscillator using a 12.5 pF crystal will be more stable and less susceptible to noise and parasitic capacitances. One reason for this is that the capacitors on the input and output will have higher values and therefore create a higher load for noise. Further these higher values make the parasitic capacitance relatively smaller for the same PCB.

Besides technical considerations there are also procurement issues. Crystals designed for a 12.5 pF load capacitance are readily available through many distributors. Crystals designed for a load capacitance of 7 pF or 9 pF are not as readily available and may have longer lead times or require a minimum quantity to be purchased.

The series resistance R_1 should ideally remain below 50 kΩ. If higher values are used (up to 100 kΩ is ok) the current consumption of the oscillator will increase a bit. If the value is really too high startup problems may occur, but up to 100 kΩ no startup problems are expected. See 6.1”Oscillation allowance”.

The frequency accuracy of the oscillator depends mainly on the accuracy of the crystal and on how well the crystal is matched to the oscillator capacitive load (C_L). A too small capacitive load results in the oscillator running fast, if the capacitive load is greater than what the crystal was designed for the oscillator and thus clock runs slow. This initial error

is indicated in Fig 7 as Δf_{off}. The largest influence on accuracy is a result of the temperature dependence of the crystal.

7.1 Modes which don't work

To keep time with an adequate accuracy it is necessary to use a quartz crystal and thus the use of a quartz crystal is always assumed in this application note. A very low power crystal oscillator as used in an RTC requires a different set of parameters compared to a universal oscillator accepting crystals, RC- and LC networks or a ceramic resonator. The oscillator circuit is not designed for operating with RC or LC networks neither for use with a ceramic resonator. Ceramic resonators have a much shorter start up time than crystals, about 100 times faster. However, they have lower frequency accuracy (initial tolerance, temperature variations, drift) and since in an RTC accurate timekeeping is the goal, ceramic resonators are not a good choice for an RTC. Use a crystal.

7.2 Effect of temperature

A tuning fork crystal is usually cut such that its frequency over temperature is a parabolic curve centered around 25 °C, see Fig 7. This means that a tuning fork crystal oscillator will resonate close to its target frequency at room temperature, but will slow down when the temperature either increases or decreases from room temperature.

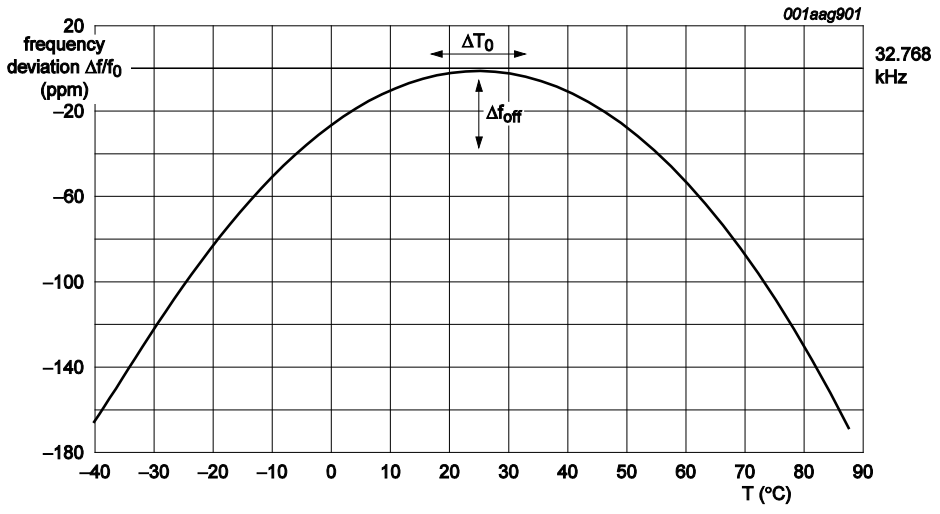


Fig 7. The deviation in frequency vs. temperature of a typical 32.768 kHz crystal

The frequency of a typical crystal at a specific temperature T is given by:

$$f = f_0\left[1 + B(T - T_0)^2\right]$$

Further f_0 can be considered to consist of two components as

$$f_0 = f_{nom} + f_{off}$$

Here f_{nom} is the nominal frequency as specified and f_{off} the offset from this nominal frequency which is a result of production spread, both at room temperature.

$$f = \left(f_{nom} + f_{off} \right) \cdot \left[1 + B(T - T_0)^2 \right]$$

For the frequency deviation $\frac{\Delta f}{f_{nom}} = \frac{f - f_{nom}}{f_{nom}}$ and expressed in ppm, this results in:

$$\frac{\Delta f}{f_{nom}} = \left\{ B(T - T_0)^2 + \frac{f_{off}}{f_{nom}} \left[1 + B(T - T_0)^2 \right] \right\} \cdot 10^6 \qquad (7.1)$$

In these equations f is the frequency, f_0 is the frequency at room temperature, B is the parabolic coefficient, T is the temperature and T_0 is the turnover temperature where the apex of the drift versus temperature curve occurs.

Three variables in equation (7.1) influence the frequency as a function of temperature. These are the parabolic coefficient B, the turnover temperature T_0 and the room temperature offset f_{off}. The crystal manufacturer specifies these parameters and typical values are B = - 0.035 ppm/°C^2 to - 0.04 ppm/°C^2, T_0 = 25 °C, ΔT_0 = ± 5 °C and f_{off} = 30 ppm. The coefficient B has a very small spread for various crystals of one type, but it has the largest effect on the parabolic nature of the frequency deviation as a function of temperature. Variation in the turnover temperature T_0 will shift the deviation curve left or right, variation in the offset at room temperature will shift it up or down. In practice the combination of variation in T_0 and offset at room temperature easily results in a (lack of) accuracy of ±30 ppm at room temperature which equates to a time deviation of around 15 minutes per year.

Application note AN10652 “Improved timekeeping accuracy with PCF8563 using external temperature sensor” describes how accuracy over temperature can be improved using an external temperature sensor and a software algorithm. It can be used for the other RTCs in this manual too in conjunction with the respective datasheets.

PCF2123 contains an offset register which allows fine tuning of the clock. This can be used to compensate for crystal aging and temperature variations. See section 10.1.

Automotive RTCs PCA8565 and PCA21125 operate also at high ambient temperatures of 125 °C. Obviously also the crystal selected for these applications should be able to handle this temperature. Generally metal can quartzes are not recommended for high temperatures because the thermal cycling (expansion of package) will cause leakages in the hermetically sealed package. Micro Crystal of Switzerland manufactures a wide range of crystals which include crystals designed to operate up to 125 °C.

8. Capacitors and capacitor selection

The influence of temperature on the accuracy of the RTC application due to the temperature coefficient of the capacitances C_{IN} and C_{OUT} is far less than due to the temperature coefficient of the crystal. Nevertheless it is good to be aware of some differences between the various types of capacitors (dielectric) around.

Ceramic capacitors tend to have low inductance because of their flat plate construction. Most other types of capacitor are wound and thus inductive. Nowadays SMD capacitors are dominant in small signal applications.

The EIA (Electronic Industries Alliance) has issued EIA-535 which defines capacitor dielectric classes. Class I and Class II dielectrics have been defined. Within these classes several types of dielectric exist. The most common ceramic types are C0G/NP0, X7R, Y5V and Z5U but others exist too.

C0G (EIA) or NP0 is the highest quality of these with the lowest capacitance / temperature dependence (Negative-Positive Zero), but has a lower permittivity, which means that its capacitance range is more restricted. NP0 refers to the shape of the capacitor's temperature graph and for NP0 this graph is nearly flat. It also exhibits a negligible capacitance and dissipation factor change with voltage or frequency.

X7R is a reasonably stable high-permittivity dielectric which allows capacitance values up to 1µF into a reasonable package. The available range is in the order from 100 pF to 22 µF in SMT, larger values are available in leaded packages. X7R formulations fall into EIA Class II materials. X7R is the most popular of these intermediate dielectric constant materials. Its capacitance variation as a function of temperature is within ±15 % from -55 °C to +125 °C. This capacitance change is non-linear and therefore difficult to express in ppm/°C since it changes over the temperature range. Capacitance for X7R varies under the influence of electrical operating conditions such as voltage and frequency. This rules out many applications, leaving only the general purpose applications like coupling and decoupling. The leakage current is sufficiently low.

Y5V formulations are for general-purpose use in a limited temperature range. Available range is from 1 nF to 22 µF in SMT, larger in leaded packages. They have a wide capacitance change of +22 % to –82 % over the operating temperature range of –30°C to +85°C. As an example, at 31% of the rated voltage (5 V over a 16 V capacitor) the resulting capacitance will have reduced to a quarter of the rated value. The effective decoupling capacitance present may thus be much less than expected. Y5V's high dielectric constant allows the manufacture of the highest capacitance value in a given case size. These characteristics make Y5V ideal for decoupling applications within limited temperature range. When specifying the values, the dependence on temperature and applied voltage must be taken into account.

Z5U shows in comparison to the previous types a much worse performance. Its capacitance changes by over 50 % with changes in temperature and applied voltage. Its temperature range is only +10 °C to +85 °C. Its initial tolerance can be as high as -20 % to +80 %. Its only redeeming feature is its high permittivity which allows high capacitance values, typically ranging from 1 nF to 4.7 µF. Good for bypass and coupling applications. It has low price, small size and low temperature stability.

Conclusion: For the oscillator only C0G types should be used. This will almost always automatically be the case since the other types are usually not available in such small values. For the decoupling of the RTC, use a capacitor with X7R dielectric. Using SMD

packages results in the lowest parasitic inductances and the small dimensions enable the smallest loops which reduces sensitivity to EMI.

A more expensive alternative for the decoupling X7R capacitor is a film capacitor using Polyethylene naphthalate (PEN), another form of polyester. It has very good heat resistance, but is otherwise much like polyester. It is available in larger sizes than C0G ceramic, lower temperature drift than polyester, and lower leakage than X7R. PEN capacitors are available to 125 °C. It is commonly found in SMD capacitors, including large values (>1 µF).

9. Accuracy

How accurate is accurate??

The international System of Units (SI) has defined the second as the duration of 9,192,631,770 cycles of radiation corresponding to the transition between two energy levels of the ground state of the cesium-133 atom. This definition makes the cesium oscillator (often called an atomic clock) the primary standard for time and frequency measurements. Its accuracy is extremely high with deviations of only a second per several million years. This equates to accuracy in the order of 10^{-8} ppm or better.

In dealing with RTCs it is common to express accuracy in ppm, parts per million. But what does it mean in more human units? A clock going too fast 1 s/day has an accuracy of 1 / (number of seconds in a day) = 1 / (24 x 3600) = 11.57 ppm. The other way around, 20 ppm is about 1 minute per month.

1 s/week = 1.65 ppm, 1 s/month = 0.4 ppm and 1 s/year = 0.031 ppm. In contrast, a good mechanical watch has a deviation of less than 12 s/day or 1300 ppm.

Fig 8 compares the magnitude of the different spreads and variations.

The RTC accuracy dominantly depends on the parameters of the resonating crystal. The initial frequency tolerance f_{off} can be compensated by tuning the external capacitance. The temperature coefficient of the external capacitances has almost no effect. The main contribution comes from the temperature coefficient of the crystal. In contrast to AT-cut crystals tuning fork crystals have the parabolic temperature dependence indicated in Fig 7 which results in a slowdown of the clock if the temperature is lower or higher than T_0 which is in the range of 25 to 28 degrees. The same type of crystal is also used in wrist watches and the turnover temperature of the crystal matches well with the temperature at the wrist which is typically about 28 °C and quite stable.

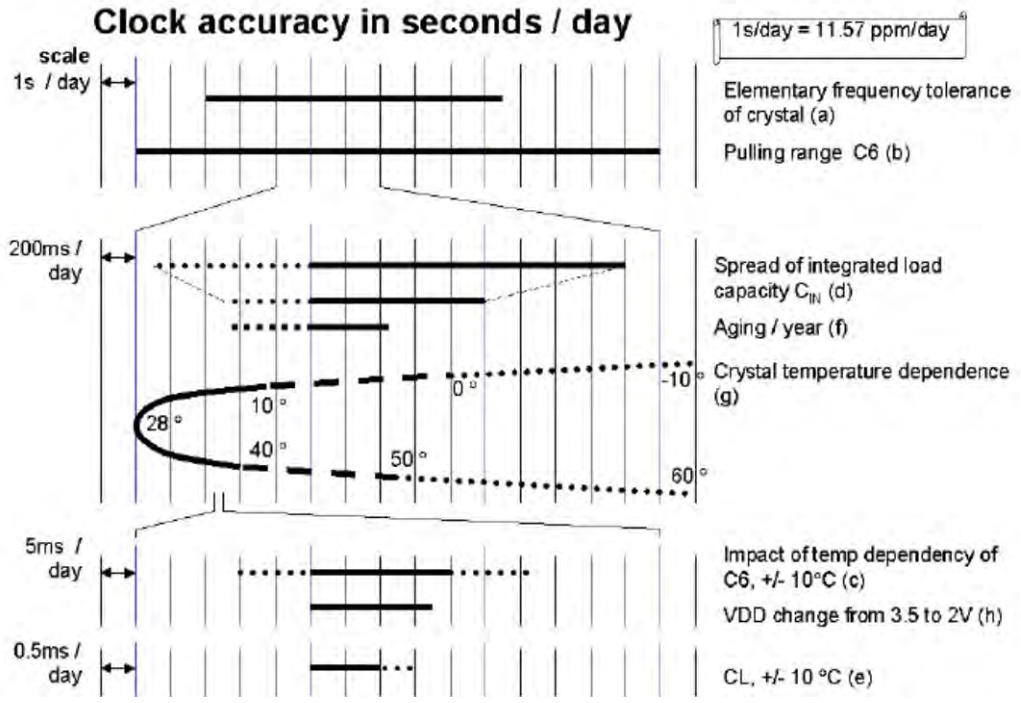


Fig 8. Influences on time accuracy

The various influences indicated in Fig 8 are described below:

1. The line at the top indicates the frequency tolerance of the crystal in this example. The distance between two vertical lines represents (at the top) 1 s/day or 11.57 ppm. The crystal spread covers about 8.5 lines and thus indicates a spread of about 100 ppm.
2. The production spread of the crystal can be compensated by adjusting the pulling capacitor C_T (in the graph called C_6) as long as the value of C_T is chosen correctly. Here the pulling range is large enough to compensate for a spread of ±175 ppm. Typically a variable capacitor has a temperature coefficient of ±300 ppm/°C to 500 ppm/°C. This capacity change has a very small influence on the accuracy of the oscillator and its influence is shown in the third line from the bottom of the graph. The solid line shows the impact of C_T (here C_6) if the value is small. If C_T is large the variation is larger as indicated with the dotted line.
3. Zooming in on a range of about 35 ppm…
4. The integrated load capacitance has a finite production spread and its potential influence on the accuracy of the oscillator depends on the value of the integrated capacitor. Whether the internal capacitor is connected to the input (C_{IN} or to the output C_{OUT}) doesn't make a difference. The solid line (third solid line from the top) covers a range of 1.8 s/day, or around 21 ppm. A greater value of C_{IN} could have a larger influence indicated by the dotted line.

5. Tuning C_T will increase the initial accuracy, indicated by reducing the range covered to the spread of C_{IN}. Depending on how well C_T is tuned, the initial spread can be well compensated for.
6. Here the influence on accuracy due to aging of the crystal is given. This shift occurs mainly during the first year of the crystal's life and in the graph a range of about 420 ms/day to 850 ms/day is indicated (±10 ppm). So if the RTC were running correctly initially, after a year it could be fast or slow by about 0.4 s/day.
7. As already mentioned and illustrated in Fig 7, the largest impact on the accuracy is due to the temperature dependence of the crystal. The parabolic nature of this dependence is indicated here as well and covers about 40 ppm over the temperature range -10 °C to +60 °C.
8. The impact of a change in V_{DD} is small; a ΔV_{DD} of 1.5 V will change the clock speed by about 17 ms/day.

From this an important recommendation follows: If possible place the crystal and IC-circuit at the spot with the least temperature variations.

10. Oscillator tuning

The PCF8563, PCF2123, PCA8565 and PCA21125 all have a CLKOUT pin which is an open drain output. It provides the option to output the buffered crystal frequency (or a lower frequency derived from the crystal frequency using division by a power of 2) which can be achieved by enabling CLKOUT in the appropriate control register and choosing the desired frequency. Refer to the datasheet of the actual device used for details on how to enable CLKOUT and set the frequency at this pin. Possible output frequencies for the PCF8563 and PCA8565 are 1 Hz, 32 Hz, 1024 Hz and 32768 Hz. The PCF2123 and PCA21125 offer some additional choices and the possible frequencies at the CLKOUT pin are 1 Hz, 1024 Hz, 2048 Hz, 4096 Hz, 8192 Hz, 16384 Hz and 32768 Hz.

PCF8573, PCF8583 and PCF8593 do not include a CLKOUT pin.

Having the CLKOUT pin enables easy tuning of the crystal frequency. A designers' initial impulse may be to connect an oscilloscope probe to the OSCO pin, but this is not a good idea. It may cause the oscillator to stop, but even if the oscillator keeps running the added capacitance of the probe will cause a drift in oscillator frequency. By connecting a pull-up resistor to the CLKOUT pin and measuring the frequency there, a much more accurate result can be achieved. The frequency can now be tuned by adjusting the variable capacitor C_T.

Remark: Touching the adjustment screw often causes the capacitance to shift. The setup is shown in Fig 9.

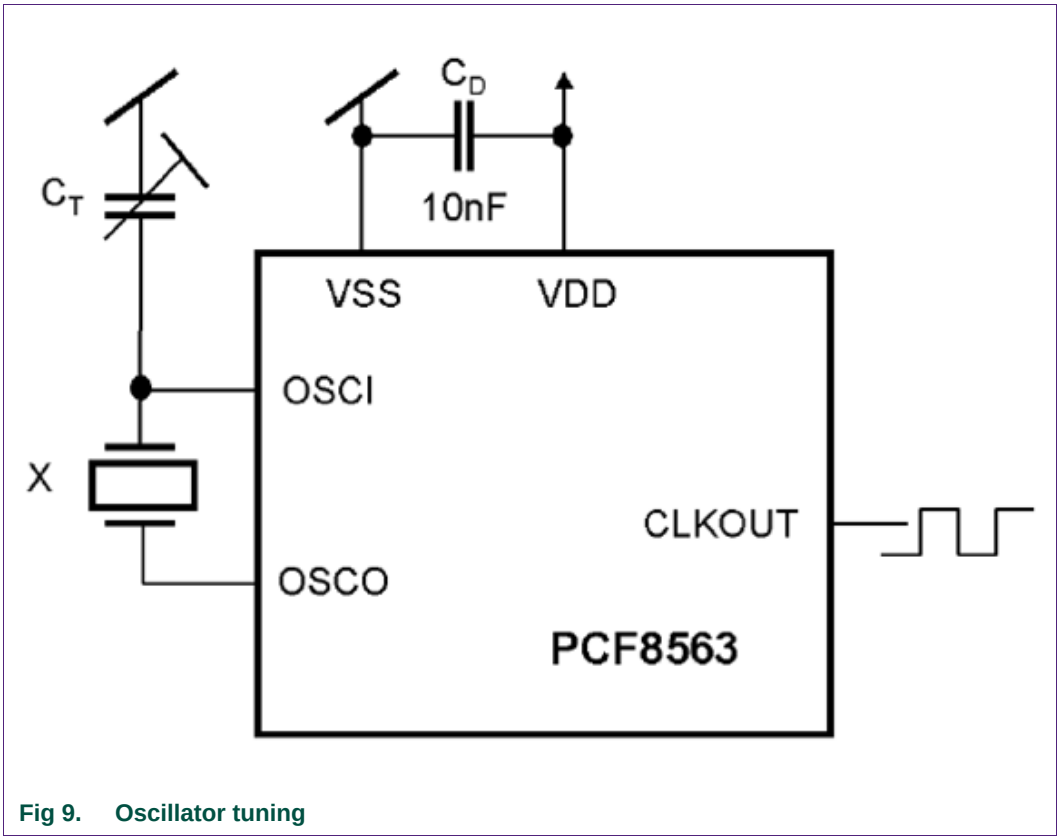


Fig 9. Oscillator tuning

Accuracy:

In order to be able to adjust the clock with accuracy better than 1 s/day, the frequency counter used to check the output at CLKOUT should have at least an 8 digit reading with an accuracy of 1 ppm.

Given a nominal frequency of 32.768 kHz, 1 ppm = 32.728 mHz (milli Hertz). Therefore +1 ppm = 32768.0327 Hz, -1 ppm = 32767.9673 Hz. Tune the oscillator while it is at the average operating temperature of the application.

The PCF8573 can be tuned by monitoring the 128 Hz signal at the FSET output.

Tuning the PCF8583/93 is somewhat more difficult since no buffered clock signal is available. There are four different options, all with their own drawbacks:

- Measure the period of the 1 s output signal (countdown timer). This however is time consuming;
- Attach the frequency counter probe to the OSCO-pin. This adds capacity to the OSCO-pin and detunes (lowers) the oscillator frequency by Δf. The frequency adjustment now needs to be lower by the same Δf in order for the clock to run at the correct speed after the probe has been removed again. Obviously the difficulty here lies in determining how big Δf is;
- In the watch industry the frequency is coupled out acoustically. A sensitive microphone is placed near the crystal. The signal is then fed as input to the tuning gear.

- In the datasheets of PCF8583 and PCF8593 the following method is described: Using the alarm function (via the I^2C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer. Procedure:
  - Power-on;
  - Initialization (alarm functions).

  Routine:
  - Set clock to time T and set alarm to time T + ΔT
  - At time (T + ΔT) (Interrupt) repeat the routine.

  However, this only works well when ΔT is an integer number of seconds. The 1/10 s and the 1/100 s are derived from a combination of 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz etc. signals. The accuracy is therefore only < ± 5 ms. Generating an alarm after T + ΔT with ΔT = 20 ms will show a jitter of plus or minus 5 ms which makes automatic tuning very complicated.

10.1 PCF2123 Offset register

The PCF2123 incorporates an offset register which can be used to implement several functions, e.g.:

- Ageing adjustment
- Temperature compensation
- Accuracy tuning

The offset is made once every two hours in the normal mode, or once every hour in the course mode. Each LSB will introduce an offset of 2.17 ppm for normal mode and 4.34 ppm for course mode. These values are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB's to -64 LSB's. The correction is made by adding or subtracting 64 Hz clock correction pulses, thereby changing the period of a single second.

In normal mode, the correction is triggered once every two hours and then correction pulses are applied once per minute until the programmed correction value has been implemented.

In course mode, the correction is triggered once per hour and then correction pulses are applied once per minute up to a maximum of 60. When absolute correction values of greater than 60 are used, additional correction pulses are made in the 59th minute.

It is possible to monitor when correction pulses are applied. The correction interrupt enable (CIE) mode will generate a 1/128 second pulse on $\overline{INT}$ for every correction applied. In the case where multiple correction pulses are applied, a 1/128 second interrupt pulse will be generated for each correction pulse applied. Correction is applied to the 1 Hz clock. Any timer or clock output using a frequency of 1 Hz or below will also be affected by the correction pulses. For more details, refer to the PCF2123 datasheet.

11. Century and leap year, Daylight Saving Time

For details on how to implement century tracking and year / leap year tracking, please refer to the datasheets of the respective RTC since register set up differs from type to type. The product comparison in Table 2 shows which parts include century, year and leap year tracking.

11.1 Century tracking

The PCF8563 and PCA8565 contain an 8-bit year register which holds the current year coded in BCD format. These two RTCs further contain a century flag which is toggled when the year counter proceeds from 99 to 00.

PCF8583 and PCF8593 have a four year calendar only and no provision to deal with century change. Also the PCF8573 has no provision to deal with century change.

PCF2123 and PCA21125 contain an 8-bit year register which holds the current year coded in BCD format. There is no century flag. Therefore application firmware needs to deal with century change.

11.2 Year and leap year tracking

A leap year (or intercalary year) is a year containing one extra day in order to keep the calendar year synchronized with the astronomical or seasonal year. Adding an extra day to the calendar every four years compensates for the fact that a solar year is *almost* six hours longer than 365 days. However, the duration of a solar year is slightly less than 365.25 days and therefore some exceptions to this rule are required. Years that are evenly divisible by 100 are not leap years unless they are also evenly divisible by 400. For example, 1600 and 2000 were leap years, but 2100, 2200 and 2300 will not be.

The PCF8563, PCA8565, PCF2123 and PCA21125 all contain an 8-bit year register which can hold values from 00 to 99 in BCD format. These real time clocks compensate for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00. Therefore in the year 2100 these RTCs add one day to February, where they shouldn't because it is not a leap year. Until then however leap year correction is correct and automatic.

PCF8583 and PCF8593 have a four year calendar only, which includes leap year tracking. The application firmware needs to deal with keeping track of the actual year.

The PCF8573 has a time counter which counts minutes, hours, days, and months, however, no years. It provides a calendar function in which firmware needs to track the years and which needs to be corrected once every four years to allow for leap year.

11.3 Daylight Saving Time (DST)

There is no provision to deal with day light saving time. Since DST is not implemented equally worldwide and can change often, it is usually better not to implement DST in the RTC but to have the application firmware deal with it. Therefore customers whose applications depend on proper adjustment to DST are advised to design their products such that firmware handles DST changes.

12. Initialization and setting of alarm and timer

Setting the clock is a straightforward procedure, setting first the mode and then the actual time. This example is for the PCF8563 and for reference its block diagram is given in Fig 10 which shows the registers and their addresses. The procedure for the other RTCs is similar but there are small differences in register structure and therefore the appropriate datasheet should be consulted first.

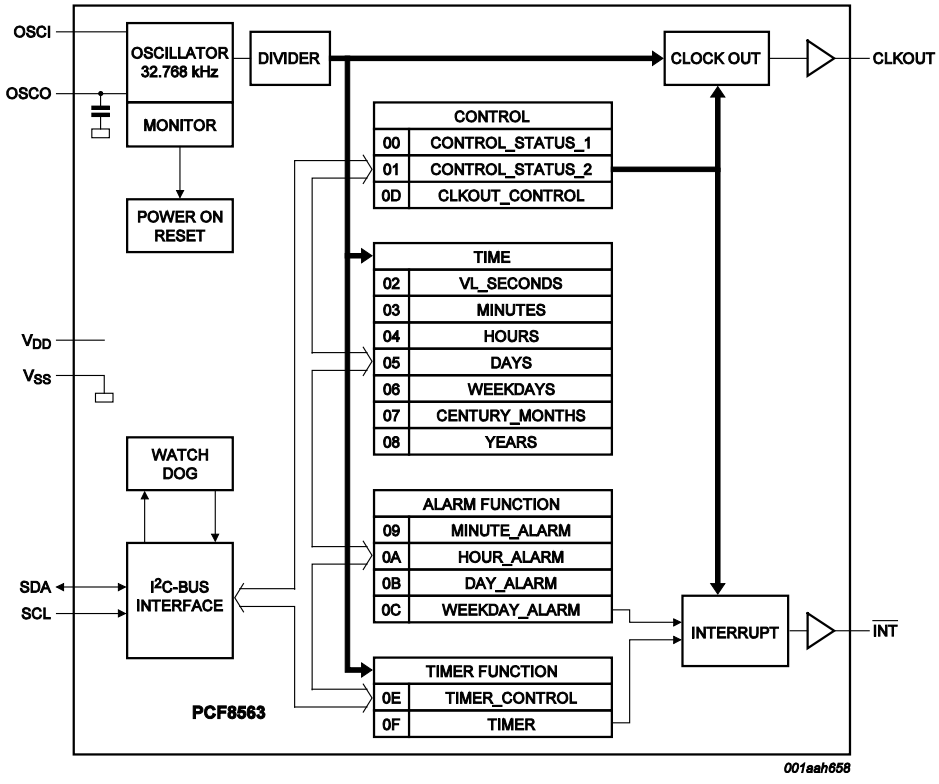


Fig 10. Block Diagram PCF8563

Examples for initialisation and setting of time, alarm and timer are given below.

12.1 Initialization of the RTC and setting the time

Table 5 on the next page shows the sequence of commands to be sent to the RTC for initialization and setting the time.

In this example the time to be set is Friday, July 16 2008, 2:45 pm.

Table 5. Setting the time and date

Sequence of commands / data to be sent

Binary (BCD)	HEX	Register Address	Comments
			generate I^2C start condition
1 0 1 0 0 0 1 0	A2		I^2C slave address, write
0 0 0 0 0 0 0 0	00		word address 0, next bytes are data
0 0 0 0 0 0 0 0	00	00	control/status 1, no test modes or POR override
0 0 0 0 0 0 0 0	00	01	control/status 2, no alarm/timer flags or interrupts
0 0 0 0 0 0 0 0	00	02	set seconds, clear voltage low detector
0 1 0 0 0 1 0 1	45	03	set minutes to 45
0 0 0 1 0 1 0 0	14	04	set hours to 14
0 0 0 1 0 1 1 0	16	05	set days to 16
0 0 0 0 0 1 0 1	05	06	set weekdays to Friday, Monday is day 1
1 0 0 0 0 1 1 1	87	07	set month to 7 and century bit to 1
0 0 0 0 1 0 0 0	08	08	set years to 08
1 0 0 0 0 0 0 0	80	09	disable minute alarm and reset to 00
1 0 0 0 0 0 0 0	80	0A	disable hour alarm and reset to 00
1 0 0 0 0 0 0 0	80	0B	disable day alarm and reset to 00
1 0 0 0 0 0 0 0	80	0C	disable weekday alarm and reset to 00
1 0 0 0 0 0 0 0	80	0D	set frequency out to 32768 Hz e.g. for tuning
0 0 0 0 0 0 0 0	00	0E	timer switched off
			generate I^2C stop condition

12.2 Alarm

It is possible to program several types of alarm. Let's take the example to set an alarm such that always 15 minutes past the hour the alarm flag AF is set and an interrupt generated.

Table 6. Setting the alarm

Sequence of commands / data to be sent

Binary (BCD)	HEX	Register Address	Comments
			generate I^2C start condition
1 0 1 0 0 0 1 0	A2		I^2C slave address, write

Binary (BCD)	HEX	Register Address	Comments
0 0 0 0 1 0 0 1	09		word address 9 for minute alarm
0 0 0 1 0 1 0 1	15	09	minute alarm enabled and set to 15 minutes
1 0 0 0 0 0 0 0	80	0A	hour alarm is disabled
1 0 0 0 0 0 0 0	80	0B	day alarm is disabled
1 0 0 0 0 0 0 0	80	0C	weekday alarm is disabled
			generate I^2C start condition (repeated start)
1 0 1 0 0 0 1 0	A2		I^2C slave address, write
0 0 0 0 0 0 0 1	01		word address 1, next bytes are data
0 0 0 0 0 0 1 0	02	01	Control/status 2, clear alarm flag and enable alarm interrupt
			generate I^2C stop condition

Remark: The interrupt is only set at the counter transition from 14 to 15. This is indicated by the dashed line in Fig 11. The interrupt has to be reset by software.

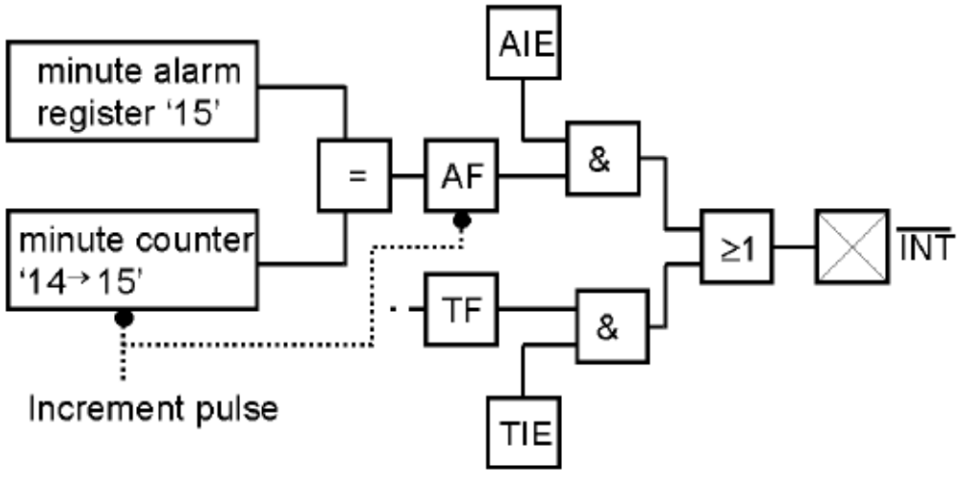


Fig 11. Alarm function

12.3 Setting the timer

The internal timer is an 8-bit countdown timer which is controlled by the timer control register. The timer counts down from a software-loaded 8-bit binary value. It can be clocked by four different source clock frequencies: 4096 Hz, 64 Hz, 1 Hz or 1/60 Hz.

This example for the PCF8563 generates an interrupt after 10 ms:

- Clock to be used 4096 Hz;
- Number of clock pulses needed = 0.01 x 4096 = 40;
- Error = 40 / 4096 Hz – 0.01 = -234 µs;
- Length of I^2C-bus initialization: 3 start conditions, 3 pulses each + 9 bytes, 9 pulses each = 90 clocks @ 400 kHz = 225 µs. Creating the clock asynchronously also gives an error of up to 1 clock pulse (see Chapter 17 “First period inaccuracy when using the timer”.). The interrupt will generate an output pulse after 9.991 ms or if the counter is set to 41 the interrupt will start after 10.236 ms.
- The timer is started by the acknowledge of the start timer instruction.

Table 7. Setting the timer

Sequence of commands / data to be sent

Binary (BCD)	HEX	Register Address	Comments
			generate I^2C start condition
1 0 1 0 0 0 1 0	A2		I^2C slave address, write
0 0 0 0 0 0 0 1	01		word address 1 (control/status register 2)
0 0 0 0 0 0 0 1	01	01	clear all flags, enable timer interrupt
			generate I^2C start condition (repeated start)
1 0 1 0 0 0 1 0	A2		I^2C slave address, write
0 0 0 0 1 1 1 1	0F		Word address $0F_{HEX}$ for timer value
0 0 1 0 1 0 0 0	28	0F	Timer value set to 40, 28_{HEX}
			generate I^2C start condition (repeated start)
1 0 1 0 0 0 1 0	A2		I^2C slave address, write
0 0 0 0 1 1 1 0	0E		word address OE for timer control byte
1 0 0 0 0 0 0 0	80	0E	Select clock frequency 4096 Hz and start timer
			generate I^2C stop condition

Refer to chapter 17 “First period inaccuracy when using the timer” for further details on timer operation.

13. Backup power supply

A real time clock is a clock that keeps track of the time as humans use it (hours, minutes, seconds, years etc.) and usually even when the rest of the system is turned off. Therefore in order to be able to always represent Real Time, real time clocks need a power supply even if the rest of the system is off. This backup power supply is often a dedicated battery or super capacitor. A super cap is a special low voltage capacitor that offers an unusual high capacitance of for example 0.47 F or 1 F in a relatively small package, especially developed for backing up volatile memory or RTCs. In case a battery is used, it may be a primary cell (non rechargeable) or a secondary cell (rechargeable) like NiCd or NiMH. Although we tend to use the words ‘battery’ and ‘cell’ interchangeably, there is a difference. Batteries comprise cells (e.g., the well-known 9-V battery contains six 1.5-V cells, while the omnipresent AA ‘battery’ and many others are just single cells). Here the common terminology is used, even though it may be at times technically incorrect.

All RTCs in this manual incorporate neither a dedicated switch-over circuit nor a charger and therefore this has to be realized with some external components. Only a few components are necessary to realize this as is illustrated in some example circuit diagrams.

If an RTC will be backed up by a battery or capacitor the current demands of the RTC, the required lifetime and the energy available in the backup source need to be matched. Backup source properties are dependent on the ambient conditions in which the application has to operate or will be stored and therefore it is important to consider these when making a choice of how to provide backup power. Criteria such as expected system life time, ambient temperature, manufacturing requirements, cost and legal regulations must be taken into account. The table below gives an indicative overview of possible backup power sources and key selection criteria.

Table 8. Overview of common backup supply components and key selection criteria

Technology	Operating Temperature [° C]	Self-discharge rate	Charging circuit and nr. of cycles	Backup time	Cost	Restrictions on disposal and safety
Primary Lithium	-30 to +80	Low	n.a.	Long	Low	High
Rechargeable (NiCd / NiMH)	0 to +40 (during charging)	Medium	Simple / ± 500	Short	Medium	Medium
Super Capacitor	-40 to +85	High	Simple / unlimited	Short	Medium / High	Low

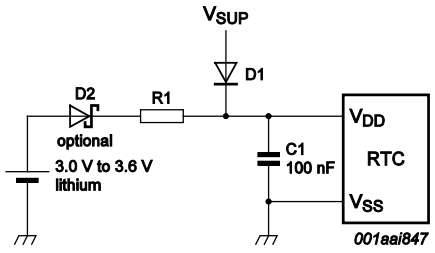
13.1 Lithium Primary cells

Amongst the primary cells, the lithium battery has the highest energy density and a very low self-discharge rate. This enables a long backup time without taking up too much space in the application. Lithium batteries, when not used properly, may constitute a risk of fire and therefore for the end product to get safety approval, certain guidelines must be taken into account. Refer to IEC/UL 60950.

Recognized lithium batteries are classified as either rechargeable or non-rechargeable. Non-rechargeable lithium batteries (primary cells) require two blocking components

(diode) or a blocking component and a current limiting component (resistor) in its circuit. A rechargeable lithium battery (secondary cell) only requires a current limiting component. In order to charge such a battery properly, a relatively complicated circuit is necessary which controls both voltage and current and which will not be discussed here.

The mentioned IEC/UL standard states that circuits employing lithium batteries shall be designed to prevent forced charge and discharge if this would result in a hazard. Practically this means that the application must ensure that both charging and discharging currents will be limited to safe values under any circumstances in order for the application to pass Underwriters Laboratories safety approval, or other similar standards. If a series diode is added meeting full UL requirements is not difficult. An example schematic is given in Fig 12. Further refer to the relevant UL/IEC documents and the specification of the battery used.



(1) D2 may not always be necessary. Refer to text.

Fig 12. Backup circuit using primary lithium cell

3.0 V or 3.6 V Lithium batteries are suitable and sizes are available that can power an RTC for over 10 years. The battery can simply be connected via a diode D_2 to V_{DD} of the RTC and ground. If for D_2 a Schottky diode is chosen, voltage drop is limited. However, since the voltage of a lithium cell remains rather stable over its life time this is usually not necessary. Depending on the soldering method used the battery can often only be placed after the board has been soldered to avoid short circuiting of the battery during the soldering process or damaging the lithium cells due to the high temperatures that occur during soldering; cell temperature must remain typically below 85 °C. Therefore a holder must be provided in which the battery is placed after soldering, or the battery must be soldered separately on the board after the other components have been placed. This increases cost.

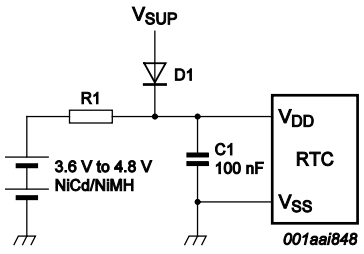
Self-discharge at room temperature and below is typically less than 1% per year. At higher temperatures, say above about 60 °C, self-discharge increases quickly. Obviously, this self-discharge also occurs when the RTC is not battery powered, the lithium cell is always there. Therefore the storage and operating temperature of the application is to be considered as well. During battery discharge the voltage remains stable such that at the end of life the voltage is almost the same as with a fresh battery and then suddenly dropping fast.

Many countries govern disposal of electronics products including the batteries at end of life. In some cases the manufacturer is responsible for complying with such regulations which may need some attention during design of the product.

In order to calculate the possible backup time, based upon the current consumption of the RTC, divide the cell capacity in ampere-hours by the timekeeping current draw of the RTC. For example, a BR1220 battery with a capacity of 35 mAh would have a theoretical life time while supplying 250 nA to a PCF8563 of 35 mAh/250 nA = 140 000 hours. This equals about 16 years. However, this is only true at room temperature where electrolyte evaporation can be neglected. At elevated temperatures of for example 60 °C electrolyte evaporation will be much higher. Refer to the manufacturer's datasheet. Vendors of lithium batteries include Panasonic, Sanyo and Varta.

13.2 NiCd and NiMH secondary batteries

The well-known Nickel-Cadmium and Nickel-Metal Hydride batteries can also be used to provide backup power to an RTC. In many countries use of NiCd batteries will be restricted in favor of NiMH batteries due to environmental considerations (cadmium). NiMH batteries also suffer less from the memory effect than NiCd batteries. As a further plus, NiMH batteries provide a higher energy density than NiCd batteries, but on the other hand have a higher self-discharge rate (about 20 % per month at room temperature) than NiCd batteries (about 10 % per month). The timekeeping current draw of an RTC is so low that often – depending on the selected battery capacity - the self-discharge is the determining factor for the available backup time, which in that case would make the NiCd more suitable for backup applications. The typical operating temperature range during charging is approximately 0 °C to +40 °C. During discharge the permitted operating temperature range is a bit wider, in the order of -10 °C to +50 °C. Just like lithium cells NiCd and NiMH batteries must be separately soldered or placed in a battery holder after the board has gone through reflow soldering. The charging circuit for NiCd and NiMH batteries in this application can be very simple; just trickle charge it via a resistor or other form of current limiting. Ordinary NiMH batteries are less suitable for trickle charging than NiCd batteries which is another reason that often NiCd batteries are better in this application. However, as pointed out before, use of NiCd batteries will be restricted in many countries due to environmental considerations. Therefore it will be harder to find NiCd batteries for backup purposes. They are being replaced by newer NiMH batteries in the same form factor and which are suitable for trickle charging. An application diagram is given in Fig 13.



(1) Due to the low RTC current consumption, a parallel diode over R_1 (directed from the battery to the RTC) will not be of any use. The voltage drop over R_1 is small

Fig 13. Backup circuit using secondary cell (NiCd or NiMH)

The capacity of a battery is expressed as C. The charge or discharge current can now also be expressed in relation to the capacity of the battery. Assume a battery with a capacity of one ampere-hour (1 Ah). A discharge current of C/10 now equals 1 Ah / 10 h = 100 mA. The recommended charge current is also specified as a fraction of C.

The recommended trickle charge current for a NiCd or NiMH is expressed as a fraction of C and is typically in the range C/50…C/20. Refer to the datasheet of the selected battery. A too small trickle current will not properly keep the battery fully charged, a too high current leads to overcharging and this will limit the life time of the battery. A diode D1 is necessary to prevent the backup battery from supplying circuitry other than just the RTC. Battery life time is limited by the number of charge / discharge cycles. Typically after 500 cycles the capacity has dropped to 60% of the original capacity which is defined as end of life for the battery.

As an example the selected battery (Varta 3/V150H) is a 3.6 V NiMH type with a capacity of 150 mAh. The recommended trickle charge current is 4.2 mA. This equals C/36. If the supply voltage V_{SUP} = 5.5 V, then R_1 = (5.5 – 0.5 – 3.6) V / 4.2 mA = 330 Ω. At such small currents, the forward voltage of a diode is less than 0.7 V and was assumed to be 0.5 V.

Vendors of NiCd and NiMH batteries include Panasonic, Sanyo and Varta.

13.3 Capacitors

In order to provide backup power to applications like RTC and volatile memory a special type of capacitor (supercap) was developed which combines a high capacitance, low-leakage and relatively small dimensions. Common values are a few mF up to 1 Farad and sometimes even more. These supercaps do not have a dielectric like ordinary capacitors but use a physical mechanism that generates a double electric field which acts like a dielectric. They are also referred to as EDL capacitors, Electric Double Layer capacitors. Charging-discharging occurs in the ion absorption layer which is formed on the surfaces of the positive and negative electrodes. Manufacturers of this type of capacitor use two types of electrolyte. One is water-soluble and the other is non-water-soluble. The latter can withstand higher voltage per cell. This type of capacitor thus uses special techniques in order to achieve such high capacitance values in a compact package. Just like an electrolytic capacitor it is polarized.

The equivalent circuit consists of many RC series circuits, connected in parallel. The capacitor is comprised of many small capacitances having resistances of various values in series. Therefore the current through the capacitor can be regarded as the sum of the currents flowing through each of the small capacitors. Due to the internal resistances, it will take many hours before the capacitor is fully charged, also when it is connected without external series resistor directly to a voltage source.

Capacitors are used for applications where backup power needs to be provided for relatively short times. Due to the low current consumption of an RTC it is possible to get several weeks of backup operation using a supercap. Using the PCF2123 or PCF8563 with a value of 1 F or 1.5 F will even result in several months of backup time. Advantages of a capacitor over batteries are amongst others the ability to be soldered together with the other components in wave or reflow soldering. There are also no regulations regarding disposal because they don’t contain any heavy metals. Just like the NiCd or NiMH batteries, the capacitor needs to be charged during normal operation and will provide backup power when the application is off since the RTC still needs to keep track of time. The application is very simple, refer to Fig 13. Here the supercap takes the place

of the battery. Connecting the supercap directly in parallel with the normal decoupling capacitor between V_{DD} and V_{SS} is possible, but it is recommended to use a series resistor R_1. The capacitance of the capacitor will change over its lifetime, especially at higher temperatures. An increase of temperature by ten degrees results in a 50% decrease of lifetime. Therefore be sure to specify extra backup time initially to allow for this decrease.

If backup is only needed for a few minutes to deal with short interruptions in power, it is possible to use a small inexpensive electrolytic capacitor.

Supercaps cannot be bought from as many vendors as ordinary electrolytic capacitors. They are available from such vendors as Panasonic, AVX and Cornell Dubilier. Important specifications are working voltage and leakage current. If the rated working voltage is only slightly exceeded, lifetime may be reduced. The leakage current should be as small as possible. A standard electrolytic capacitor has a leakage current several times larger than the timekeeping current consumption of the RTC and will limit the backup time severely. Also leakage current of super capacitors can easily exceed the timekeeping current consumption of an RTC and careful selection will result in longer backup time.

In most applications the lifetime of a supercap will exceed the lifetime of a NiCd or NiMH battery. It decreases however with increasing temperature, humidity, applied voltage and current. Although a supercap will often be the better choice as backup source compared to rechargeable batteries in terms of available backup time, life time and cost (both for relatively short backup times), for every specific application pros and cons of both must be evaluated.

13.3.1 Charging the backup capacitor

Although not strictly necessary it is advised to charge the capacitor via a resistor in order to limit the charge current. A resistor in series with a capacitor creates an RC-time constant T. In order to calculate the charging time of the capacitor the following parameters are important:

- Capacitor value (i.e. 1 F)
- Capacitor starting voltage (i.e. 0 V)
- Series resistor (i.e. 4.7 kΩ)

The time constant T of the circuit equals R·C. The capacitor can be considered charged after a time t = 5T. For this example t = 5 x 1 x 4700 = 23500 seconds. This is about 6.5 hours. This is the theoretical charging time of a capacitor with series resistance, but for a supercap it may take even longer to become fully charged due to the many internal series resistances with various values.

In this example the capacitor is charged to the supply voltage. Since the time keeping voltage is lower than the supply voltage that is used in a typical application, it does not take a time t = 5T for the capacitor to reach a voltage where it can start backing up the RTC if main power would be interrupted.

13.3.2 Estimation of backup time with capacitor

In order to keep the calculations simple a constant current draw of the RTC is estimated also when the supply voltage drops as the capacitor gets discharged. It is assumed that the capacitor is fully charged. The following data is necessary for the calculations:

- $V_{Cbackupstart}$: The backup capacitor voltage when backup starts.

- $V_{Cbackupend}$: The backup capacitor voltage when backup ends, which equals the minimum oscillator operating voltage, specified in Table 2 as clock operating voltage.
- I_{RTC} : The time keeping current consumption of the RTC. For lowest current consumption disable CLK-OUT.

Using C·V = I·t:

$$t_{backup} = \frac{C \cdot \left(V_{Cbackupstart} - V_{Cbackupend}\right)}{I_{RTC}}$$

Assuming that the PCF8563 is used, that $V_{Cbackupstart}$ = 3.3 V, that the RTC current consumption is 250 nA and a backup capacitor value of 0.47 F it is possible to estimate the available backup time. The oscillator stops running when V_{DD} drops to 1.0 V.

$$t_{backup} = \frac{0.47\ F \cdot \left(3.3\ V - 1.0\ V\right)}{250 \cdot 10^{-9}\ A} = 4324000\ s$$

As one day contains 86400 seconds this thus corresponds to 50 days. In order to reserve for capacitor and supply current tolerances and variations in temperature, a 30% margin should be included. This means reducing the backup time by 30% resulting in 35 days.

In this calculation example the leakage currents through diode D_1 and through the super cap have been ignored. In a similar way the required capacitance value can be calculated if the required backup time is known.

13.4 Diode selection

In order to optimize possible backup time it is useful to select a low leakage diode for D_1, i.e. a diode with a low reverse current. If without further consideration a common small signal diode is chosen, its reverse current may be in the order of the current consumption of the RTC when the RTC is just keeping time without being accessed. The common 1N4148 for example has a specified maximum reverse current of 25 nA at 25 °C which however can increase to 300 nA at 80 °C. Whether this is a problem depends on the application. If it is, special low leakage diodes are available which in some cases limit reverse current to a few picoampere. In Table 9 some diodes are suggested which limit reverse current I_R to a few nanoampere. These diodes are all available from NXP.

Table 9. Some suggestions for diode D1

	1N4148	BAS45A	BAS45AL	BAS716	BAS116	BAV170
Package	leaded	leaded	SMD	SMD	SMD	SMD
Typ. reverse current I_R at 25 °C	-	0.2 nA	0.2 nA	0.2 nA	3 pA	3 pA
Max. reverse current I_R at 25 °C	25 nA	1 nA	1 nA	5 nA	5 nA	5 nA
Price indication, relative w.r.t. 1N4148	1 (0.02 $)	7x	8x	3.5x	3x	3x

BAS116 is the cheapest alternative here and shows low leakage current. BAV170 is equally good and for the same price it offers two diodes in a 3-pin package, with common cathode. By interchanging the positions of D_2 and R_1 in Fig 12 this component can be used such that it represents both D_1 and D_2.

As stated before, usually it is not necessary to select a Schottky diode. In case some application requires ultra-low voltage drop over the diode, an option is the PMEG3005EB which shows very small forward voltage drop at the expense of a higher reverse current.

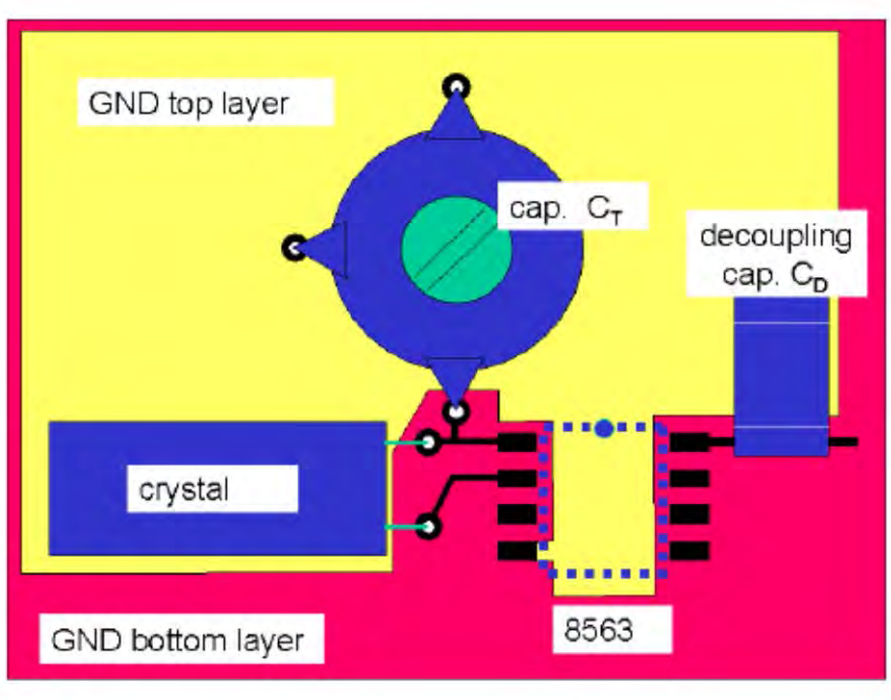
14. PCB layout guidelines

The tuning fork crystal's drive level is extremely low (< 1 µW) and the input of the amplifier used in the oscillator (pin OSCI) has a very high impedance. This makes the circuit susceptible to signals generated by other circuits on the board, or further away. Generally the lower the timekeeping current, the more susceptible the crystal connections will be to noise, since lower current consumption implies higher impedance nodes. The track from crystal to amplifier input can easily work as an antenna and therefore should be kept as short as possible. The output of the amplifier OSCO is connected to the other side of the crystal and is thus a sensitive node as well. In order to ensure proper operation some PCB guidelines should be strictly adhered to.

- Traces between the oscillator input and output pins, the crystal and the external load capacitors, should be as short as possible. Place also a 100 nF – 470 nF decoupling capacitor close to the RTC with short tracks to V_{DD} and V_{SS}.
- The external load capacitor's layout preferably is symmetrical and both ground connections should be as close as possible.
- In order to avoid direct signal coupling, OSCI and OSCO traces should be routed as far away as possible from each other.
- Routing on inner layers and vias of the oscillator signals must be avoided. Vias form an inductance.
- Digital signal lines should be kept as far as possible from the crystal (this includes the serial bus signals to the RTC).
- Digital signal lines or other signal lines with high frequency content should not be routed on inner layers under the crystal / RTC area.
- Route the CLKOUT signal away from the crystal connections. If possible route a ground or power track between the CLKOUT signal and crystal connections.
- The crystal housing (metal-can packages) should be connected to ground (not for the PCF8573, PCF8583 and PCF8593; here connect the housing to V_{DD}).
- The PCA8565A and PCF2123 (here for C_L = 7 pF) include two integrated oscillator capacitors and thus don't need external oscillator capacitances. This also means that no compensation can be made by choosing slightly smaller values if the layout introduces parasitic capacitance due to ground signals or planes.
- A dedicated RTC ground plane should be placed beneath the crystal and the input/output capacitors, possibly also running beneath the RTC itself. Input/output capacitors can be connected to this ground plane. This ground plane should be connected with a short trace to V_{SS} of the real-time clock, and should not be connected to any other ground signals. Therefore only one connection between this ground plane and general GND exists and thus it is ensured that no unknown

currents will run via the dedicated RTC ground plane. Remember that success in noise/disturbance-free design depends on always knowing where all the currents flow (and keeping them away from where they are not wanted).

A layout proposal using leaded components is shown in Fig 14. In this example the external oscillator capacitor is adjustable. Often a fixed capacitor will be used. In this case place it horizontally such that the loop from the RTC via the capacitor to GND is as small as possible. See also Fig 15 which shows a layout example with SMDs.



(1) In practice the input capacitor C_T will in most cases be a fixed capacitor

Fig 14. PCB layout proposal for PCF8563 using leaded components

Alternatively to the last point listed above and in order to achieve highest noise immunity, a guard ring can be placed around the crystal which must be tied to ground to isolate the crystal from unwanted noise pickup. It should be tied to V_{SS} of the real time clock at one place only to avoid unforeseen currents running via the guard ring. In addition another local ground plane on an adjacent PCB layer can be added under the crystal. Also this ground plane should be isolated from the regular PCB ground plane and connected to V_{SS} of the RTC. The dimensions of this ground plane shouldn't be much larger than the perimeter of the guard ring, but optimally should include the complete crystal and RTC. Be aware that this ground plane will create parasitic capacitances on the OSCI and OSCO pins because on the adjacent outer layer the tracks to the crystal will run. A sketch of such a layout is given in Fig 15. Here the use of SMD components is assumed which is recommended because the smaller dimensions will result in smaller loop areas.

Both examples use the PCF8563. The same principles apply when one of the other RTCs is used, with some small modifications due to differences in pinning.

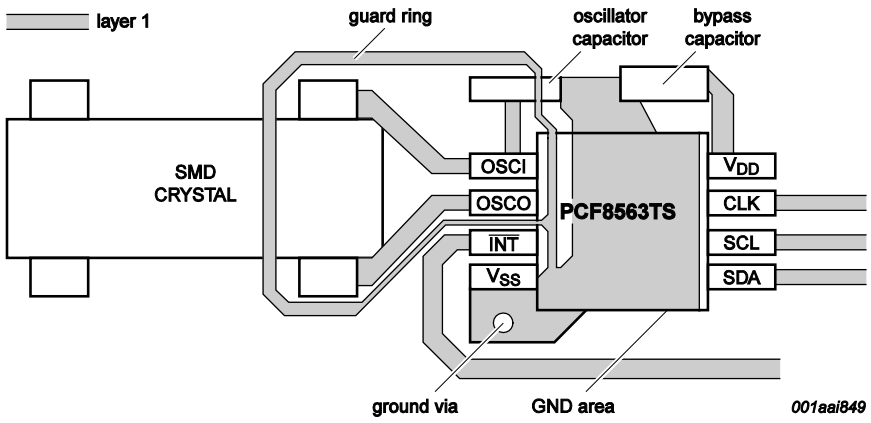


Fig 15. PCB layout proposal for PCF8563 using SMD components and guard ring

Remark: Take precautions when cleaning PCBs containing tuning fork crystals using ultrasound. The resonance vibration may damage the crystal. Consult the supplier of the crystal in case of doubt.

15. Partial circuit switch down

The I²C-bus RTC circuits PCF8563, PCA8565 and PCF8593 have on the pads SDA, SCL and $\overline{INT}$ a diode clamping circuit without an upper clamping diode to V_{DD}, refer to Fig 16.

Therefore it is possible to partially switch off V_{DD} such that the RTC is powered down or working at a lower supply voltage than the rest of the circuit without the risk that via such (upper) clamping diodes SDA, SCL and $\overline{INT}$ would be pulled down as well.

The other way around with only the RTC powered in order to keep time and the rest of the circuit switched off will be a more common situation. If during normal operation the complete application is powered by a certain V_{DD} of for example 3.3 V or 5 V, then during standby just the RTC can be operating and powered from a backup source as discussed in Chapter 13. See Fig 16 and Fig 18 plus Fig 19.

PCF8583 has no protection diode from $\overline{INT}$ to V_{DD} but has protection diodes from the I²C-bus pins to V_{DD} ! Battery backup will work, but with the RTC powered down the I²C-bus may get stuck.

The SPI-bus RTC circuits PCF2123 and PCA21125 have on pins SDI and SCL only one clamping diode from V_{SS} to the pin. On pin SDO an additional clamping diode to V_{DD} is integrated. This allows for partial circuit switch down where the RTC still runs and the rest of the application is powered down.

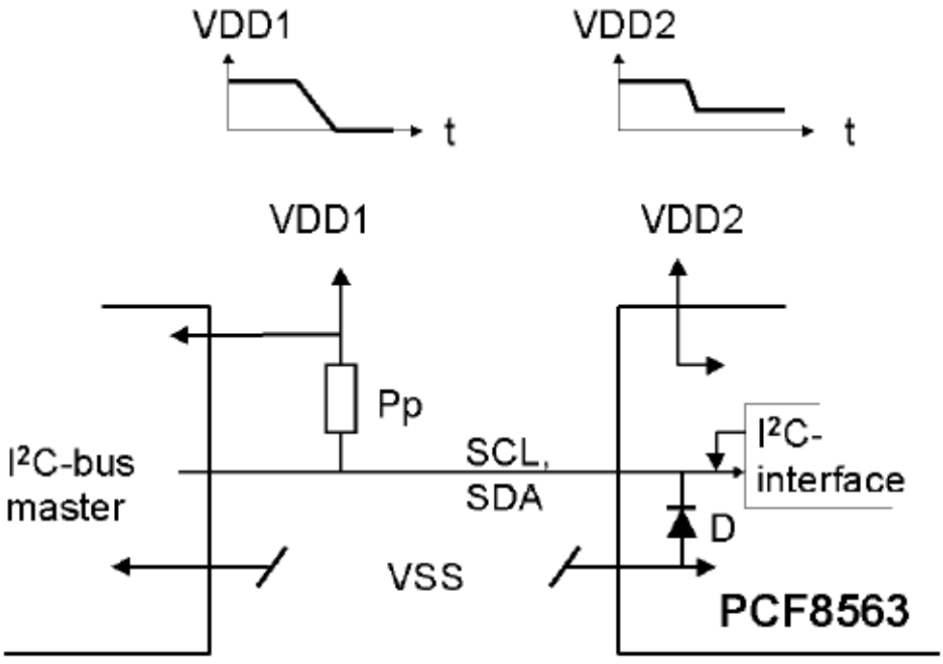


Fig 16. Protection diodes

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16. Hints to keep power consumption low

For some applications low power consumption is a key requirement. Power consumption can be minimized by applying several measures:

- Select PCF8563 (I^2C) or PCF2123 (SPI-bus). The PCF2123 has the lowest power consumption which is further decreased when a crystal is selected that has a load capacitance of 7 pF instead of the more standard 12.5 pF (a lower load capacitance results in a lower power consumption, but not all RTCs allow to select a crystal that requires a C_L in that range);
- Select a crystal with a low motional resistance. The higher the resistance the higher the losses. For lowest power consumption, aim to find a crystal with $R_1 < 40\ k\Omega$;
- The timer source clock frequency influences power consumption which is highest at 4096 Hz. The difference in power consumption between the other three clock frequencies is negligible;
- Use lowest possible V_{DD}. See the application examples given in Fig 18 and Fig 19. During normal operation a diode charges a super cap of for example 0.47 F or 1 F. During standby the RTC is supplied by this super cap. General purpose small signal diodes may have leakage currents in the order of magnitude of the current consumption of these low power RTCs. In order to maximize the RTC backup time it is advisable to select a low leakage current diode. See section 13.4;

- Access the RTC as little as possible in order to reduce the dynamic current consumption by the I²C-bus or SPI;
- Disable the CLKOUT in battery backup mode. If CLKOUT needs to be enabled select the pull-up resistor as large as possible. However, CLKOUT enabled will dominate current consumption and severely limit battery backup time;
- Do not connect the pull-up resistors for the serial interface to V_{DD} of the RTC but connect them to the supply of the rest of the circuit (V_{DD1} in Fig 16). This avoids unnecessary battery current drain from the battery via the pull-up resistors. If in "Power-Off" everything gets powered down except the RTC, the bus lines will often not be high impedance. In this case current could run from the battery via the pull-up resistors and the bus to GND which would severely reduce the possible battery backup time, if the pull-ups were connected to V_{DD} of the RTC;
- Select the I²C-bus pull-up resistors as large as possible. The value of the pull-up resistors is a compromise between current consumption and maximum clock frequency. Lower values result in lower RC time constants and thus faster rise time of the SCL and SDA lines. Using the I²C-bus, data transfers can be made up to 100 kbit/s in Standard-mode and up to 400 kbit/s in Fast-mode. The corresponding required maximum rise times are 1 µs for Standard-mode and 300 ns for Fast-mode. The rise time is a product of bus capacitance and the value of the pull-up resistor. The bus capacitance is the total capacitance of wire, tracks, connections and pins. First estimate the capacities. Track capacities can be calculated with the standard formula for a capacitor. Depending on the PCB material used, values for ε may differ.

  For this example a track length of 3 cm is assumed, with a track width of 0.5 mm on a copper backed 0.7 mm strong PC-board made from FR4 glass epoxy.

$$C_{tr} = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d} = \frac{8.85 \cdot 10^{-12} \cdot 4.6 \cdot 0.03 \cdot 0.0005}{0.0007} = 0.9 \cdot 10^{-12}\ F$$

  Further capacitances are:

Microcontroller pin capacitance	C_i = 7 pF	(assumption)
RTC pin capacitance	C_i = 7 pF	(max value for PCF8563)

  Adding these capacitances to the 0.9 pF track capacitance results in a bus capacitance of 14.9 pF.

  Consider the V_{DD} related input threshold of $V_{IH} = 0.7V_{DD}$ and $V_{IL} = 0.3V_{DD}$ for the purposed of RC time constant calculation. Then $V(t) = V_{DD}(1 - e^{-t/RC})$, where t is the time since the charging started and RC is the time constant.

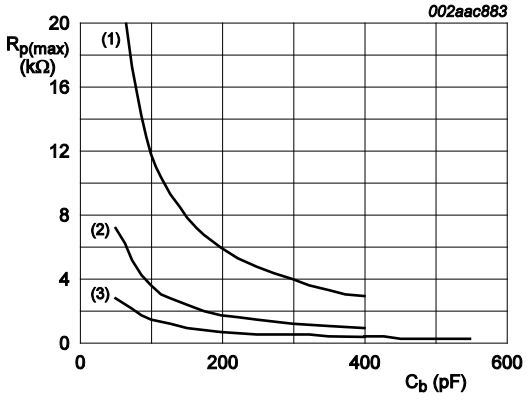
  $V(t1) = 0.3 \times V_{DD} = V_{DD}(1 - e^{-t1/RC})$; then $t1 = 0.3566749 \times RC$

  $V(t2) = 0.7 \times V_{DD} = V_{DD}(1 - e^{-t2/RC})$; then $t2 = 1.2039729 \times RC$

  $T = t2 - t1 = 0.8473 \times RC$

  The graph in Fig 17 and the equation below show maximum R_P as a function of bus capacitance for Standard-mode, Fast-mode and Fast-mode Plus. For each mode the $R_{P(max)}$ is a function of the rise time maximum and the estimated bus capacitance C_b.

$$R_{P(\max)} = \frac{t_r}{0.8473 \cdot C_b}$$



(1) Standard-mode
(2) Fast-mode
(3) Fast-mode Plus

Fig 17. $R_{p(max)}$ as a function of bus capacitance

Below $R_{p(max)}$ is calculated for both Standard-mode and Fast-mode I²C bus. The result has been rounded down to E6 standard values.

400 kHz I²C bus: $R_{P-400kHz} = \frac{t_r}{0.8473 \cdot C_b} = \frac{300 \cdot 10^{-9}}{0.8473 \cdot 14.9 \cdot 10^{-12}} = 22\ k\Omega$

100 kHz I²C bus: $R_{P-100kHz} = \frac{t_r}{0.8473 \cdot C_b} = \frac{1 \cdot 10^{-6}}{0.8473 \cdot 14.9 \cdot 10^{-12}} = 68\ k\Omega$

Two examples of an application diagram are shown in Fig 18 and Fig 19. In these examples the $\overline{INT}$ output is left unused. If used, a pull-up to V_{DD} is required.

The first example is using PCF8563 (Fig 18), the second example is using PCA21125 (Fig 19). In both examples the optional backup supply is realized using a 1 F capacitor.

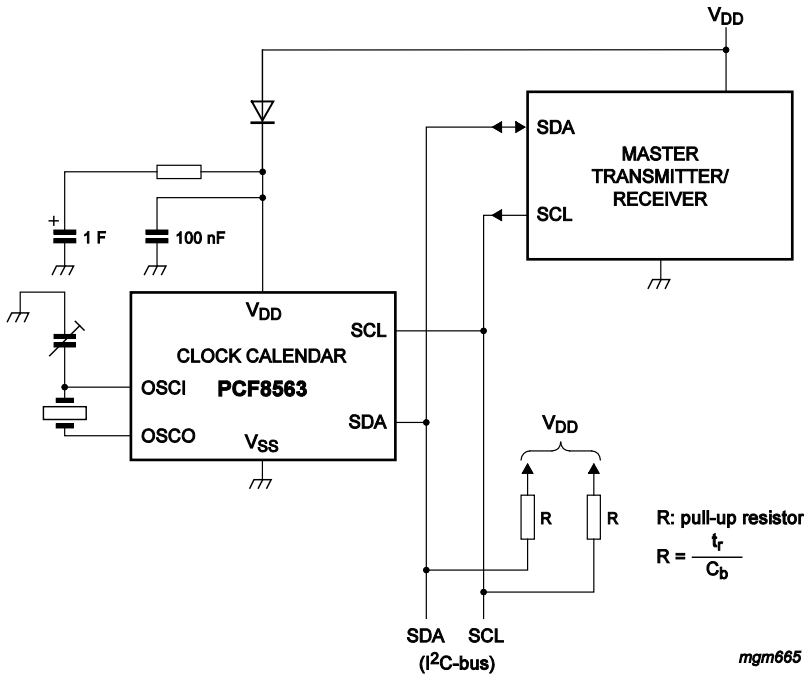
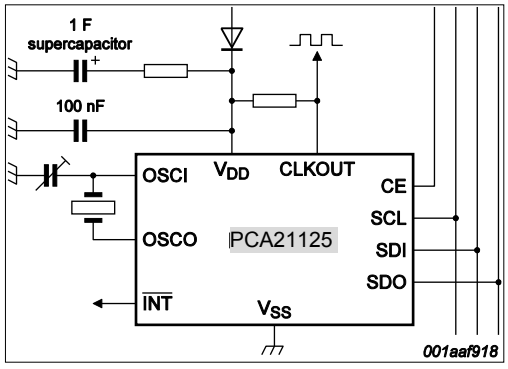


Fig 18. Application diagram 1, I²C-bus interface

The following example is with PCA21125 and SPI interface.



The 1 Farad capacitor is used as a standby/backup supply. With the RTC in its minimum power configuration i.e. timer off and CLKOUT off, the RTC may operate for several months.

Fig 19. Application diagram 2, SPI interface

Remark: CLKOUT and $\overline{INT}$ are open drain outputs. If a pull-up resistor is used, it should not be connected to voltages higher than the maximum operating voltage as specified for the RTC. If the outputs need to be used to switch signals connected to a higher potential, it is necessary to use an external transistor.

17. First period inaccuracy when using the timer

This chapter describes why the programmed delay is not always exactly as expected and what to do in order to be as accurate as possible. The enable instruction for the timer is generated by the I^2C or SPI interface clock. This clock is asynchronous to the timer source clock. The timer source clock is derived from the 32.768 kHz crystal frequency. The consequences will be described here.

The RTCs for which this user manual was written include a countdown timer function, except PCF8583 and PCF8593. The 8-bit countdown timer is controlled by the timer control register. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz or 1/60 Hz), and enables or disables the timer.

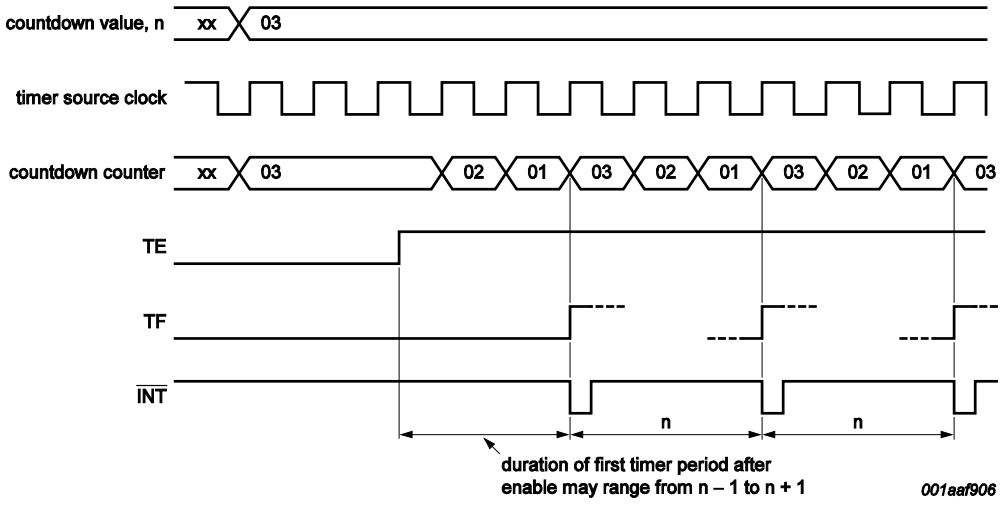
Table 10. Timer delays

Range of possible timer delays dependent on selected source clock frequency and n

Timer Source clock frequency [1]	delay for n = 1	delay for n = 255
4096 Hz	244 µs	62.256 ms
64 Hz	15.625 ms	3.984 s
1 Hz	1 s	255 s
1/60 Hz	60 s	4 hrs 15 min

[1] If the timer is not used, set source clock frequency to 1/60 Hz for power saving

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency will result in deviation in timings.



In the example it is assumed that the timer flag is cleared before the next countdown period expires and that the $\overline{INT}$ is set to pulsed mode

Fig 20. General countdown timer behaviour

The timer counts down from a software-loaded 8-bit binary value, n. Loading the counter with 0 effectively stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown Timer Flag (TF) will be set and the counter automatically re-loads and starts the next timer period. The timer has two operating modes, TI and TP. If the timer interrupt is enabled, the bit TI/TP determines the operating mode. For more details see below. Reading the timer will return the current value of the countdown counter (see Fig 20).

If a new value of n is written before the end of the current timer period, then this value will take immediate effect. It is not recommended (especially when using the faster time source clocks) to change n without first disabling the counter. The counter is disabled by setting Timer Enable TE = 0. The update of n is asynchronous to the timer clock, therefore changing it without setting TE = 0 may result in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. However, the probability of this happening depends on the selected timer source clock. If the timer clock is not first stopped then there is a possibility that the timer clock and the interface clock which is loading the countdown timer could arrive at the same time. This may corrupt the countdown value. With a 1-minute clock (1/60 Hz) this is unlikely to happen, especially when the application software waits for the timer to trigger and then straight away sets a new value for n. As long as this new value is written within 1 minute here, there is no problem. The same reasoning is valid for the other timer source clocks but obviously there is much less time to do so. If the 1-second clock is selected this would work too if the microcontroller communicating with the RTC is fast. For faster timer source clocks it gets unreliable and should be avoided.

Also in the case where the timer clock and the interface clock arrive at the same time which may corrupt the first count down value, the countdown value n will however be correctly stored and correctly loaded on subsequent timer periods.

When starting the timer for the first time, the first period will have an uncertainty which is a result of the enable instruction being generated from the interface clock (I^2C or SPI) which is asynchronous from the timer source clock. Subsequent timer periods will have no such delay. Therefore only the first timer period will exhibit this uncertainty. The amount of delay for the first timer period will depend on the chosen source clock, see Table 11.

Table 11. First period delay for timer counter value n

Timer source clock	minimum timer period	maximum timer period
4096 Hz	N	n + 1
64 Hz	N	n + 1
1 Hz	(n-1) + 1/64 Hz	n + 1/64 Hz
1/60 Hz	(n-1) + 1/64 Hz	n + 1/64 Hz

When reading the timer, the current countdown value is returned instead of the initial value n. For accurate read back of the countdown value, the SPI or I^2C bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

As an example, the desired timer period is 5 seconds. If the timer source clock frequency is set to 1 Hz and n = 5, the minimum possible timer period will be (5-1) + 15.625 ms = 4.015625 s. The maximum possible timer period will be 5 + 15.625 ms = 5.015625 s. The resulting timer period will have a duration somewhere within these limits.

Similarly, if the desired timer delay is 1 minute, one option would be to choose the timer source clock 1/60 Hz and set n = 1. However, then there would be only one timer period and it has an uncertainty. The duration is not exactly defined. A better way is to select the 1 Hz source clock and set n = 60. There will be an uncertainty in the first period too but the consecutive 59 periods are exact and the resulting total uncertainty is 60 times smaller.

The conclusion is that for a given desired delay, minimum uncertainty will be achieved by choosing a higher setting of n combined with a higher timer source clock.

At the end of every count down the timer sets the Timer Flag (TF). The TF may only be cleared by software. The asserted TF can be used to generate an interrupt signal on pin $\overline{\text{INT}}$ provided that this mode is enabled. Refer to the relevant datasheet for details on how the interrupt can be controlled which is done via certain bits in the control registers. The timer has two operating modes, TI and TP. If the timer interrupt is enabled, the bit TI/TP determines the operating mode. If bit TI_TP is set to 1, the chosen timer mode is ‘pulsed’. In this mode an interrupt is generated after the timer period elapses. This is independent of the timer flag and will thus happen every time the timer period elapses, periodically. The clearing of the timer flag is only necessary if TI mode is chosen, if the consecutive interrupt is to happen. In the TI mode the signal remains permanently high as long as the Timer Flag is active.

18. Timing requirements for I²C read and write

Reading to and writing from the time and date registers is an event which is controlled by the interface bus (I²C or SPI) but which is asynchronous to the internal 32.768 kHz clock of the RTC. It happens at random instants with respect to the automatic update of the internal registers. Without precautions, two types of read errors could occur when the time and date registers increment while being read. First, the data could change while a single register is being read. Second, the data could change during the time between reading two registers. Assume for example that the clock increments from 09:59:59 to 10:00:00 during a read of the seconds, minutes and hours registers. The time read could be 10:00:59 and this is incorrect. A similar reasoning applies to writing. Measures must be taken to prevent such read and write errors. In the NXP RTCs this is realized by freezing the contents of all counters when one of the RTC registers is read or written. This is called time counter freeze. Therefore faulty reading of the clock/calendar during a carry condition is prevented.

Fig 10 shows the block diagram of the PCF8563 with attached to the I²C-interface a watchdog. More details are given in Fig 21 where a block diagram representing some blocks in the RTC has been drawn. In Fig 22 a sequence of events after a read operation starts is depicted.

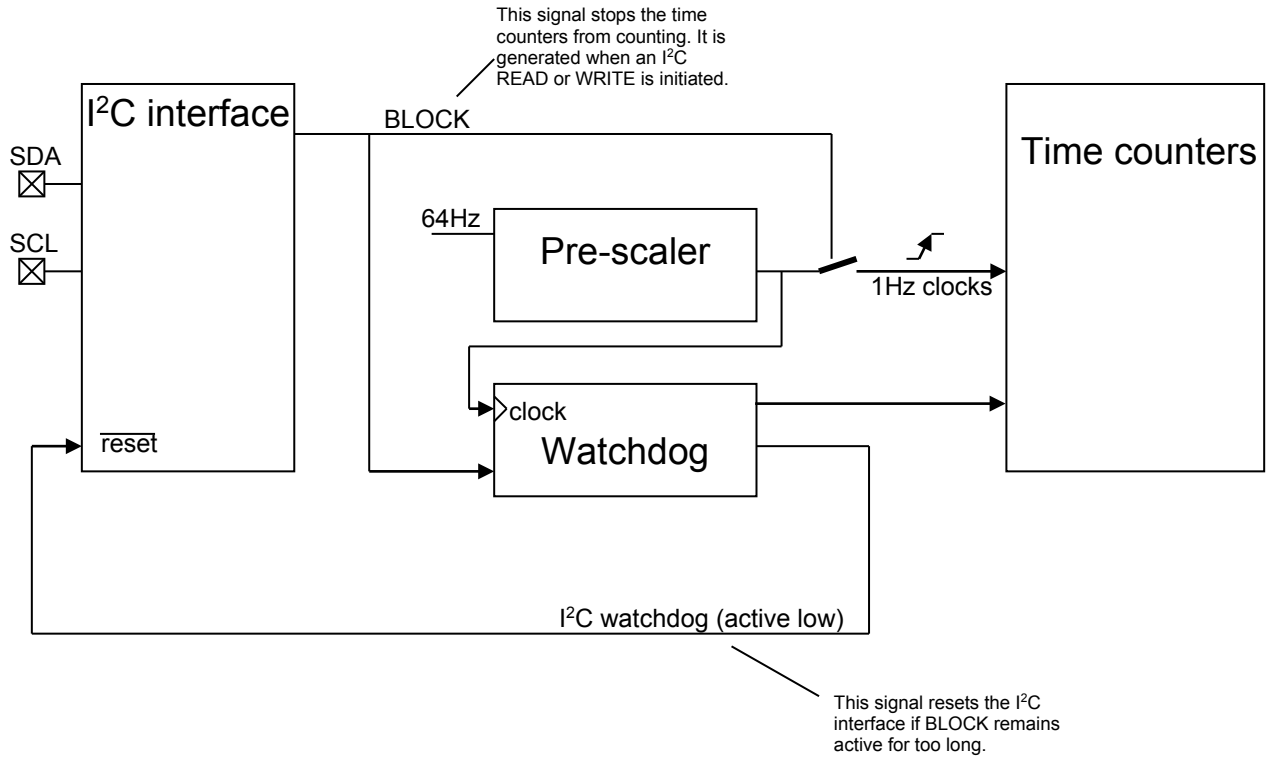


Fig 21. Block diagram I²C interface and Time counters

When there is no I²C activity the RTC is counting normally. Once an I²C read or write operation is initiated, the I²C interface asserts the signal BLOCK. This signal stops the time counters from counting. Additionally this results in the watchdog no longer being reset. At the next rising edge of the 1 Hz clock, time does not increment because the registers have been frozen. However, the watchdog counter increments now. Thus the increase in time is recorded and after the read operation has completed BLOCK goes low again. Now the stored clock in the watchdog is used to give an extra pulse to the time counters to make sure that correct time is kept. Also the watchdog will be reset.

The maximum watchdog value is 2. If at the second rising edge of the 1 Hz clock after a read operation was initiated, the reading operation has not been completed yet, BLOCK will still be high. The time counters don't increase and the watchdog counter increases and reaches its maximum value. Its output is set active which resets the I²C interface which in turn resets the BLOCK signal. Again one pulse (not two) is sent to the time counters and the watchdog is reset. But now two rising edges of the 1 Hz clock didn't reach the time counters and only one was compensated for. The RTC loses one second. The exact sequence of events is depicted in Fig 22.

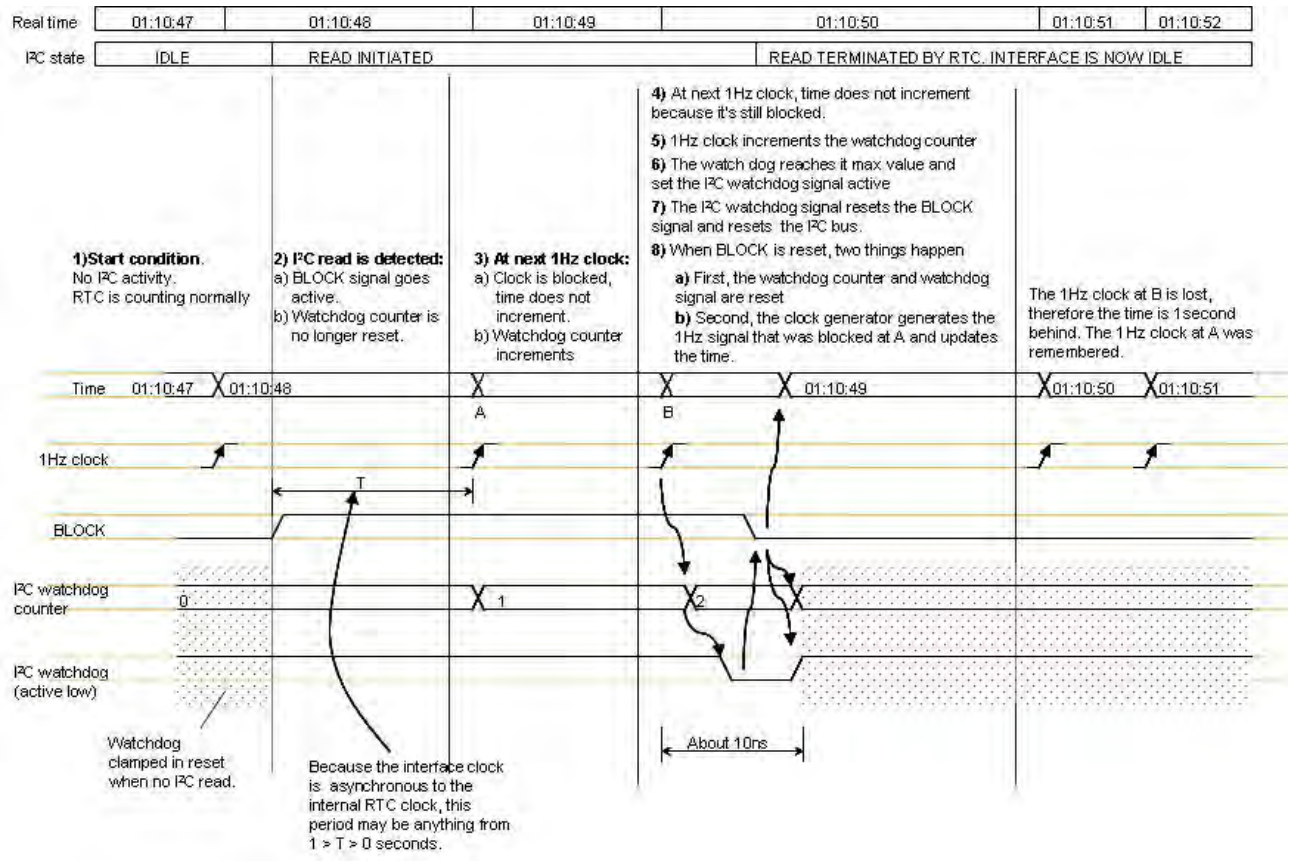


Fig 22. Sequence of events (example READ)

From this follows:

- A I²C read must be terminated within one second of initiation;
- The RTC will automatically terminate the read if it remains active for longer than one second;
- Each time auto termination occurs, the RTC loses one second;
- The signal BLOCK is also active during a write. A write must also last less than one second;
- BLOCK is necessary for a write since the registers must not update whilst new data is being written. That is impossible anyway, since the clock is switched from the 1 Hz clock to the internal I²C clock.

Remark: The RTCs allow to set the word address in order to address a particular register, for example the seconds register. If the application software is written such that separate bus accesses are used to read the individual time/date registers it is possible that after reading/writing those registers the time as read or written by the system controller is not correct. This is because time counter freeze – implemented to avoid such errors - is active only during one access, starting from the START condition and ending when the STOP condition occurs. Now still the errors mentioned in the introduction of this

chapter could occur. First, the data could change while a single register is being read. Second, the data could change during the time between reading two registers. Therefore in order to avoid this from happening it is necessary to read all time registers in one single read operation, using the auto-increment function. The same goes for writing all registers in one single write operation when time and date is set.

19. Troubleshooting

This chapter provides some tips to troubleshoot an application if problems are encountered, for example when a new design is made.

19.1 Oscillator startup time

Assuming that a proper crystal was selected and that the layout guidelines given in this user manual were followed, the oscillator should start up without problems. As already mentioned starting times are relatively long due to the very high value of L resulting in a very high Q-factor. The start-up will mostly take less than a second and should definitely be achieved within five seconds. Oscillator start-up times are highly dependent on crystal characteristics and PCB layout. High ESR and excessive capacitive loads are the major causes of too long start up times, or the oscillator not starting at all. Oscillator start up depends also on the ambient temperature.

19.2 Checking for oscillation

In order to check whether the oscillator is running, the initial thought may be to connect an oscilloscope to the oscillator out pin in order to observe the waveform. When dealing with an RTC this is the wrong thing to do. As pointed out before the oscillator is very sensitive to disturbance due to the low power it consumes. Adding the probe capacitance will detune the oscillator which usually will stop it. Sometimes what seems to be a useable waveform may be seen but it will precisely tell you nothing due to the capacitance added by the probe. In some cases applying a scope probe can even cause a faulty oscillator design to start up, hiding design issues.

The simplest way to check for oscillation is to use the CLKOUT. If the design does not include a pull-up resistor to the CLKOUT, then add one temporarily. Applying a scope probe to the CLKOUT should reveal a block signal with a frequency that depends on the settings in the control registers. Don’t forget to first enable CLKOUT. Refer to the datasheet for details on initializing the RTC.

Another good method is to read the real time clock as time advances and see time readings adjust accordingly by looking at the seconds register. These methods will however not work if communicating with the RTC doesn’t work due to problems with the serial bus.

19.3 No communication via I²C-bus

When no communication with the RTC is possible, it is also not possible to set and read time. Normally the I²C-bus will not get stuck, but especially during the development phase problems may occur that hang up the bus. One reason may be that spikes on the bus lines are interpreted as additional pulses which then would convey data not in line with the I²C-protocol. Also timing violations when for example two GPIOs are used to emulate an I²C-bus sometimes lead to unexpected results. On I²C-devices a scope may be used to verify whether the RTC sends an acknowledgement at the end of each byte. Over the past years oscilloscopes have been introduced that allow trigger and decode for serial bus protocols, including I²C and SPI. Also timing violations can be easily found with such equipment. These include rise and fall times, setup time, hold times and also voltage levels.

If the bus gets stuck first it needs to be determined how exactly it is stuck. There are two “bus stuck scenarios”:

- SCL (clock) stuck low: There is nothing that can be done about this but to hard reset the device (remove power) because the I²C-bus requires clock edges to clock the data;
- SDA (data) stuck low, but clock ok: A start condition can’t be sent because this requires a high to low transition of SDA while SCL is high. SDA however is stuck low. What will work is to send 9 clocks plus a STOP condition. The 9 clock pulses will clear the I²C state machine, thus causing the device to release the bus. This permits the master to send a STOP condition and now the I²C interface of the slave will have been reset. This works for all I²C compatible devices without exception.

According to the I²C specification there exists a so-called general call address. This is for addressing every device connected to the I²C-bus at the same time. The general call address is 00_{HEX}. However, if a device does not need any of the data supplied within the general call structure, it can ignore this address by not issuing an acknowledgement. An I²C device does not have to be designed such that it responds to a general call address. The real time clocks for which this manual is valid do not respond to the general call address.

Sending the 9 clock pulses with SDA low may seem like sending a general call address since data is always zero for every clock pulse. The difference however is that no START condition could be sent first since SDA was already stuck low. Sending the 9 clock pulses is not the same as sending a general call address. If a device does require data from a general call address, it will acknowledge this address and behave as a slave receiver. The master does not actually know how many devices acknowledged if one or more devices respond. The second and following bytes will be acknowledged by every slave-receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not-acknowledging. These RTCs will not respond to a general call.

In short, when the bus is stuck low due to SDA, the sequence to recover the bus is by sending 9 clock pulses plus STOP.

Remark: Only the PCF8593 includes a dedicated $\overline{\text{RESET}}$ input. When reset occurs only the I²C-bus interface is reset. Thus for this device a second option of releasing the I²C-bus is available.

19.4 Wrong time and date, wrong clock speed

When writing into the RTC registers care has to be taken that only valid values are written. For example, seconds only should go to 59, but it is possible to write for example 61 into the seconds register. Care needs to be taken that the software routines convert correctly to the BCD values used in the RTC. If a wrong value is written, at some point the register will return to a valid value, but then still the time indicated will not be correct, since the initial write was wrong.

If the clock is running too fast, usually the cause is spurious signals from other parts of the application that somehow couple into the oscillator signal and are interpreted as additional clock signals. As indicated in the parabolic curve of Fig 7, the crystal frequency will reduce if temperature decreases or increases with respect to the turn over temperature. Assuming that the load capacitance fits the crystal selected, the oscillator will run at 32.768 kHz and can only run slower under influence of temperature.

Refer to Chapter 14 “PCB layout guidelines” to avoid the problem of spurious signals coupling into the oscillator.

If the RTC runs too slow (or it appears to loose time) make sure that read and write operations are finalized within 1 second of initiating them. Refer to Chapter 18 “Timing requirements for I^2C read and write”.

20. References

The documents below provide further useful information.

1. Product data sheets of all real time clocks for which this manual is valid.
2. AN10716_1; Background information and theory related to Real Time Clocks and crystals.
3. AN10652_1; Improved timekeeping accuracy with PCF8563 using external temperature sensor. Rev 1, 2 November 2007.
4. UM10204_3; I^2C-bus specification and user manual. Rev 3, 19 June 2007.
5. Paper “An improved low power crystal oscillator”, Werner Thommen, EESCIR’99, Duisburg, Sept. 1999, pp. 146-149.
6. Epson Toyocom, Crystal Devices Catalogue “The crystal master”, 2007.
7. Micro Crystal, Product Catalog Quartz Crystals 2008.

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22. List of figures

Fig 1. Power-on reset....8
Fig 2. Voltage-low detection....9
Fig 3. Oscillator-stop detection....9
Fig 4. Pierce Oscillator equivalent diagram....10
Fig 5. Oscillator frequency determining components 11
Fig 6. Graph of oscillator frequency as function of load capacitance C_L....12
Fig 7. The deviation in frequency vs. temperature of a typical 32.768 kHz crystal....17
Fig 8. Influences on time accuracy....21
Fig 9. Oscillator tuning....23
Fig 10. Block Diagram PCF8563....26
Fig 11. Alarm function....28
Fig 12. Backup circuit using primary lithium cell....31
Fig 13. Backup circuit using secondary cell (NiCd or NiMH)....32
Fig 14. PCB layout proposal for PCF8563 using leaded components....37
Fig 15. PCB layout proposal for PCF8563 using SMD components and guard ring....38
Fig 16. Protection diodes....39
Fig 17. $R_{p(max)}$ as a function of bus capacitance....41
Fig 18. Application diagram 1, I^2C-bus interface....42
Fig 19. Application diagram 2, SPI interface....42
Fig 20. General countdown timer behaviour....43
Fig 21. Block diagram I^2C interface and Time counters....46
Fig 22. Sequence of events (example READ)....47

23. List of tables

Table 4. Typical values for crystal and surrounding capacitors....14
Table 5. Setting the time and date....27
Table 6. Setting the alarm....27
Table 7. Setting the timer....29
Table 10. Timer delays....43
Table 11. First period delay for timer counter value n....44

24. Contents

1. Introduction 3
2. Features 4
3. Comparison 6
3.1 Event counter mode 6
4. Power-on reset (POR) 8
5. Voltage-low detector 8
6. Oscillator 9
6.1 Oscillation allowance 15
6.2 Using an external oscillator 15
6.2.1 RTC family PCF85x63, PCF8563, PCF8564A, PCA8565, PCF8523 15
6.2.2 PCF2123 16
6.2.3 PCF8583 and PCF8593 16
7. Crystal and crystal selection 16
7.1 Modes which don't work 17
7.2 Effect of temperature 17
8. Capacitors and capacitor selection 19
9. Accuracy 20
10. Oscillator tuning 22
10.1 PCF2123 Offset register 24
11. Century and leap year, Daylight Saving Time . 25
11.1 Century tracking 25
11.2 Year and leap year tracking 25
11.3 Daylight Saving Time (DST) 25
12. Initialization and setting of alarm and timer 26
12.1 Initialization of the RTC and setting the time 26
12.2 Alarm 27
12.3 Setting the timer 29
13. Backup power supply 30
13.1 Lithium Primary cells 30
13.2 NiCd and NiMH secondary batteries 32
13.3 Capacitors 33
13.3.1 Charging the backup capacitor 34
13.3.2 Estimation of backup time with capacitor 34
13.4 Diode selection 35
14. PCB layout guidelines 36
15. Partial circuit switch down 38
16. Hints to keep power consumption low 39
17. First period inaccuracy when using the timer 43
18. Timing requirements for I²C read and write 45
19. Troubleshooting 48
19.1 Oscillator startup time 48
19.2 Checking for oscillation 48
19.3 No communication via I²C-bus 49
19.4 Wrong time and date, wrong clock speed 50
20. References 50
21. Legal information 51
21.1 Definitions 51
21.2 Disclaimers 51
21.3 Trademarks 51
22. List of figures 52
23. List of tables 53
24. Contents 54

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