

HW Getting Started Guide



MPC8568E MDS Processor Board

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About This Document

This document shows how to connect the MPC8568E MDS Processor Board and verify its basic operation, in a step by step format. Settings for switches and jumpers are shown, as well as instructions for connecting peripheral devices. Instructions for connecting the MPC8568E MDS PB to an IDE, such as Freescale's *CodeWarrior*[®] are included, but instructions for working with the IDE are beyond the scope of this document.

Required Reading

The *MPC8568 Reference Manual* has information on the chip, and the *MPC8568E MDS Processor Board User's Guide* has much more detailed information on the processor board. The *Kit Configuration Guide* has instructions on working with the software

Definitions, Acronyms, and Abbreviations

BCSR	Board Register	MDS	Modular Development System
COP	Debug port in PowerPC	PCI	Peripheral component interconnec
DDR2	Double data rate DRAM	PLL	Phase Lock Loop
DIP	Dual In-line Package	QE	Quick Engine, a block in the MPC83xx line of chips
I2C	Philips serial port	SODIMM	Type of memory device
LED	Light Emitting Diode	Tu	Time unit (0.95ns)
		USB	Universal Serial Bus

MPC8568E MDS Processor Board

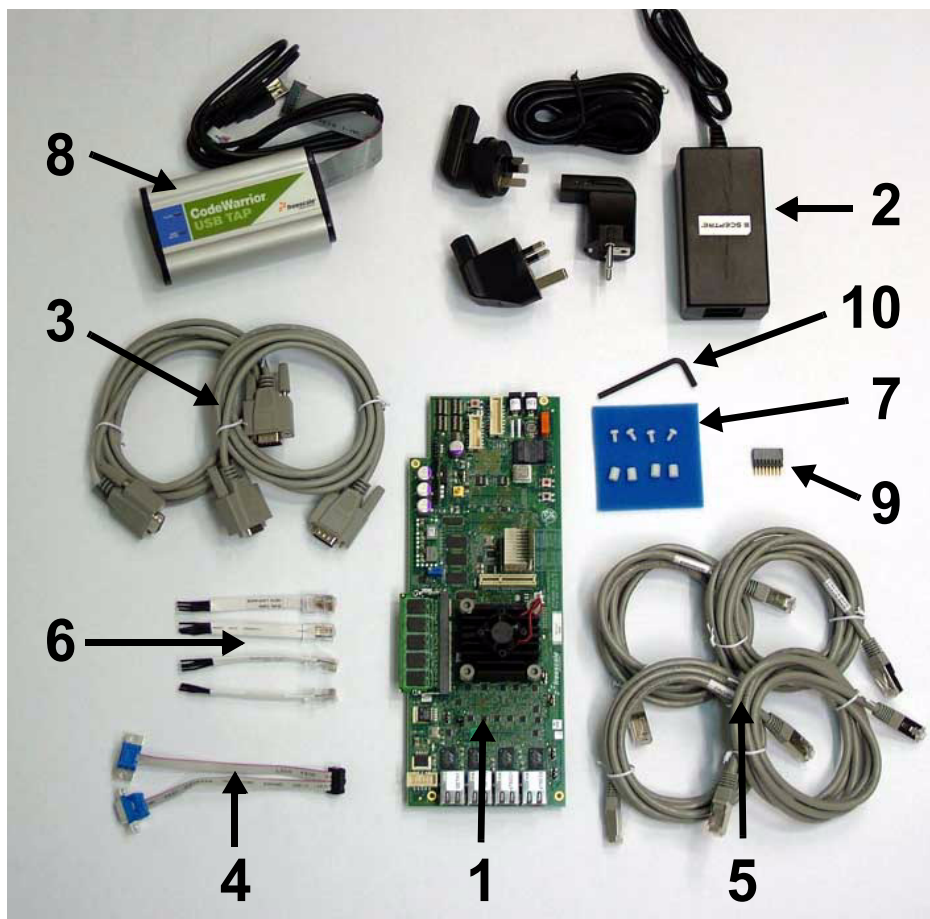
HW Getting Started Guide

Step 1: Check kit contents

1. MPC8568E MDS Processor Board
2. AC/DC 5V/8A universal power supply kit
3. RS232 9-Pin cable (2)
4. Freescale adaptor cable (joined with two RS232 connectors to single IDC 10-pin, for UART1/2)
5. Giga-bit Ethernet cables (4) with RJ45-8 connectors
6. Giga-bit Ethernet loopback cables (4)
7. One set of four plastic spacers
8. CodeWarrior USB Tap
9. Interconnection header (used if programming the BCSRs via the USB Tap (For instructions on using this, see the *MPC8568E MDS User's Guide*.)
10. Allen wrench
11. MPC8568E MDS Processor Board documentation, software and tools (not shown)

Optional (not shown):

- PCI_PCl e adaptor card - required if using the MPC8568E MDS Processor Board as a PCI or PCIe agent. For instructions on using this, see the *MPC8568E MDS User's Guide*.
- PCI Panel - required if using the MPC8568E MDS Processor Board in a PC.



Step 2: Connect plastic spacers

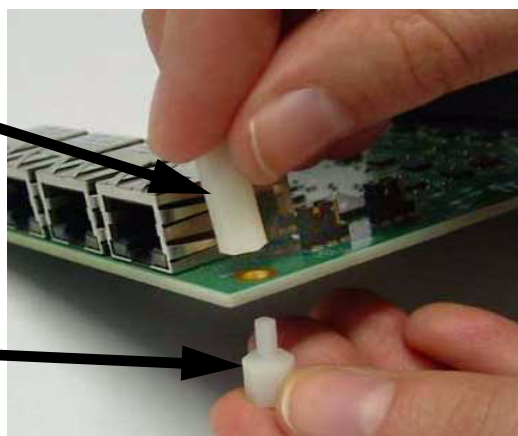
Note: Perform this step only if you are using the processor board in a stand-alone mode.

One set of four plastic spacers screw into holes located at (approximately) the four corners of the board. The spacers raise and stabilize the board.

1. From the lower surface of the board, insert a smaller spacer into one of the board's four spacer holes.
2. Attach a larger spacer (or screw, if included in kit) onto the lower spacer, and screw it on.
3. Repeat for the three remaining spacers.

Large spacer (or screw)

Small spacer

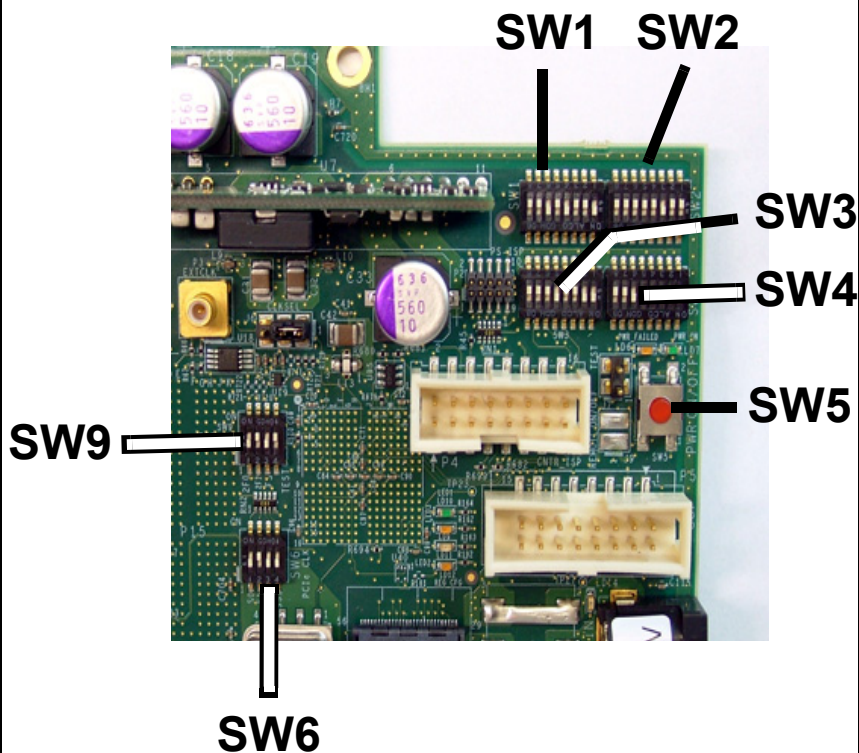


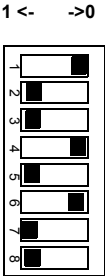
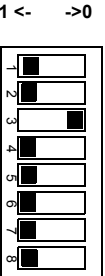

Step 3: Check Switches

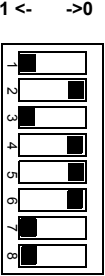
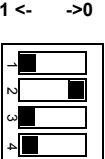
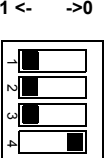
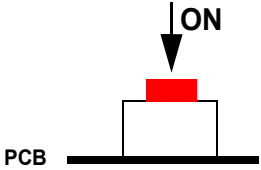
The Dual-In-Line Package (DIP) switches of the MPC8568E MDS PB are shown at right. The default DIP-switch positions set-up the MPC8568E MDS PB clock mode as shown in the table below:

MPC8568E MDS Processor Board Clock Mode
(default values)

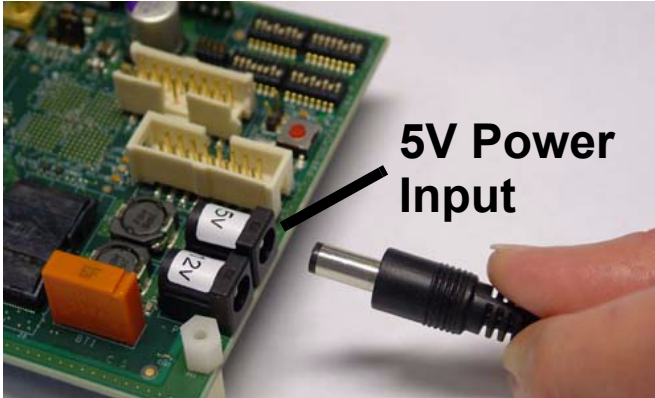
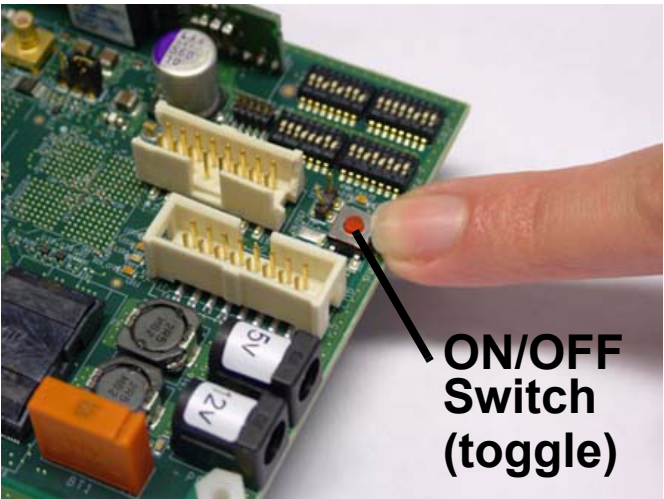
Core Frequency	1000 MHz
CCB	400 MHz
DDR2	200 MHz
Local Bus If LCRR = 0XXXXXXXX2	100 MHz
QE	400 MHz



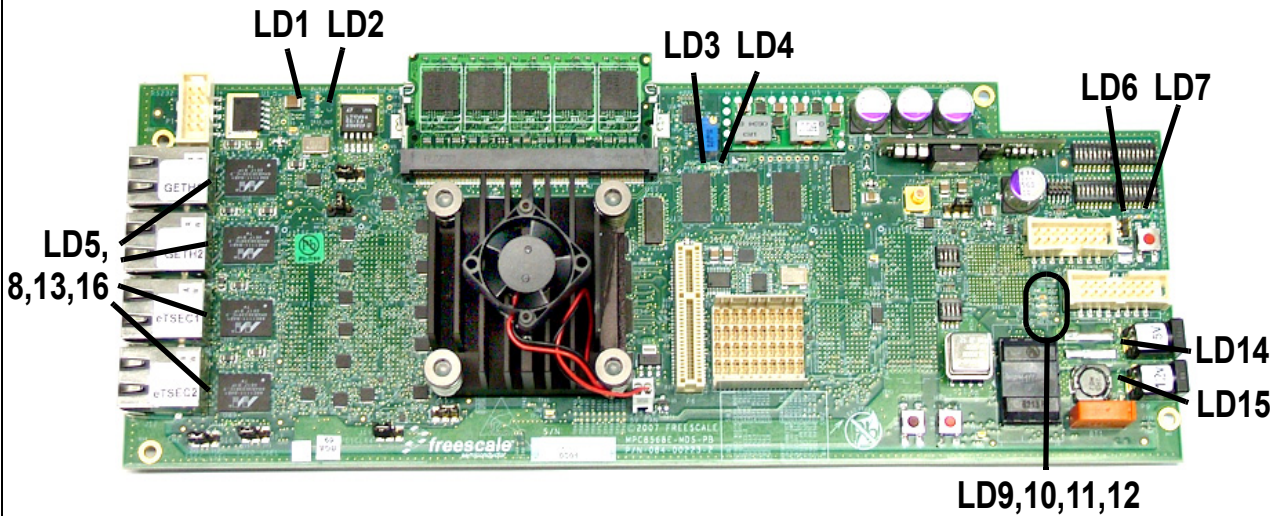
<p>Step 3.a: SW1 Configuration</p> <p>1: SYS PLL0 2: SYS PLL1 3: SYS PLL2 4: SYS PLL3 5: CORE PLL0 6: CORE PLL1 7: CORE PLL2 8: CFG_CPU_BOOT</p>  <p>The "On" DIP Switch position corresponds to a signal value of "zero".</p>	<p>SW1.1-SW1.4: SYS PLL[0:3] Sets the platform frequency (CCB) factory setting: '0110' = 400Mhz.</p> <p>SW1.5 - SW1.7: CORE PLL[0:2] Sets the multiplication factor for COR PLL = CCB * CORE PLL[0:2] factory setting: '101' = 1066Mhz</p> <p>SW1.8 CFG_CPU_BOOT Enables/Disables the e500 core to boot without waiting for configuration by an external host factory setting: '1' = enable the e500 to boot independently</p> <p>Default setting: 01101011</p>
<p>Step 3.b: SW2 Configuration</p> <p>1: ROMLOC0 2: ROMLOC1 3: ROMLOC2 4: Host/Agent0 5: Host/Agent1 6: Host/Agent2 7: BOOTSEQ1 8: CFG_SRDS_EN</p> 	<p>SW2.1-SW2.3: ROMLOC[0:2] Selects the Boot ROM location from one of the following locations: PCI, DDR2, SRIO, PCIe, Local bus factory setting: '110' = Boot from Local Bus 16bit (Flash).</p> <p>SW2.4-SW2.6: Host Agent PCI, PCIe, SRIO selection. [0:2] factory setting: '111' = MPC8568 acts as the host processor/root complex.</p> <p>SW2.7 Boot Sequence1 (Boot sequence[0] tied to '1') it is possible to from Extended I2C or to disable I2C Rom accessed. factory setting: '1' = No I2C ROM is accessed.</p> <p>SW2.8: CFG_SRDS_EN Enables/Disables the SerDes interface factory setting: '1' = enable the SerDes interface</p> <p>Default setting: 11011111</p>
<p>Step 3.c: SW3 Configuration</p> <p>1: QEPLL0 2: QEPLL1 3: QEPLL2 4: QEPLL3 5: QEPLL4 6: QE UCC Volt 7: Tsec1 Width 8: Tsec2 Width</p> 	<p>SW3.1-SW3.5: QE PLL setting [0:4] Sets the multiplication factor that is used to calculate QECLK from the input clock (SYSCLK) . factory setting: '00110' for fcore = 400MHz.</p> <p>SW3.6: QE UCC Voltage Sets the voltage of UCC when it works with GETH factory setting: '1' = UCC voltage = 3.3V</p> <p>SW3.7: Tsec1 Width Set to standard mode. factory setting '1' for GMII.</p> <p>SW3.8: Tsec2 Width Set to standard mode. factory setting '1' for GMII.</p> <p>Default setting: 00110111</p>

<p>Step 3.d: SW4 Configuration</p> <p>1: Tsec1 Prtc0 2: Tsec1 Prtc1 3: Tsec2 Prtc0 4: Tsec2Prtc1 5: RIO SYS SIZE 6: PCI I/O IMPD 7: PCI ARBITER 8: Reserv</p> 	<p>SW4.1: SW4.4 Tsec1,2_Prtc[0:1]. Selects the eTSEC protocol: MII, GMII, or TBI factory setting: '10' (GMII) for both eTSEC1 & eTSEC2.</p> <p>SW4.5: RIO SYS SIZE factory setting: '0' = Small system size up to 256 devices.</p> <p>SW4.6 PCI I/O Impedance: factory setting: '0' = 25Ohm I/O impedance.</p> <p>SW4.7 : PCI Arbiter. factory setting: '1' = The on chip PCI arbiter is enabled.</p> <p>SW4.8 : Reserved. factory setting: '1' = Reserved</p> <p>Default setting: 10100011</p>
<p>Step 3.e: SW6 Configuration</p> <p>1: Clock0 2: Clock1 3: Spread0 4: Spread1</p> 	<p>SW6.1: SW6.2 PCI Express/sRIO Clock[0:1]. Sets the clock value. factory setting: '10' = 100MHz</p> <p>SW6.3: SW6.4 PCI Express/sRIO Clock Spread[0:1]. Sets the spread value. factory setting: '11' = No spread</p> <p>Default setting: 1011</p>
<p>Step 3.f: SW9 Configuration</p> <p>1: 2F0 2: 2F1 3: FS 4: Test</p> 	<p>SW9.1: SW9.2 Skew Control [0:1]. Sets the skew of the PCI clock. factory setting: '11' = No skew If using MPC8568E board as agent, this must be set to '10' on host board</p> <p>SW9.3: PLL Frequency range. Sets the PLL frequency range. factory setting: '1' = 48MHz - 100MHz</p> <p>SW9.4: Test. Disables output if skew = -4Tu (Tu = "time unit" = 0.95ns). factory setting: '0' = disable output if skew = -4Tu</p> <p><i>This switch provides a digitally controlled delay of the PCI_CLK signal in order to provide stable operation of the board when it is a PCI agent</i></p> <p>Default setting: 1110</p>
<p>Step 3.g: SW5 Power Switch</p> 	<p>SW5: power switch (toggle)</p> <ul style="list-style-type: none"> power from an external 5V power supply via the P10 power jack combined mode: powered from +5V on PIB power supply through riser connectors board plugged as a PCI add-in card: PC internal power supply will provide 5V via PCI edge connector

<p>Step 4: Check Jumpers Jumper locations are shown in the figure at right.</p> <p>Check the default positions, as shown in the sub-steps below, and verify that the board is operational before changing any settings.</p>																	
<p>Step 4.a: J2:</p> <p>3 <input checked="" type="checkbox"/> TDMC-RXCLK 2 <input checked="" type="checkbox"/> PD22 (CLK7) 1 <input checked="" type="checkbox"/> UPC2-RXCLKIN</p>	<p>Selects input for CLK7: TDMC_RXCLK or UPC2_RXCLKIN</p> <ul style="list-style-type: none"> • For UPC2-RXCLKIN: Connect 1-2 (default) • For TDMC-RXCLK: Connect 3-2 																
<p>Step 4.b: J4 & J5:</p> <p style="text-align: center;"> <table border="0"> <tr> <td></td> <td></td> <td style="text-align: center;">J5</td> <td></td> </tr> <tr> <td></td> <td></td> <td style="text-align: center;"><input checked="" type="checkbox"/> 3 RMII_RXCLKODD</td> <td></td> </tr> <tr> <td>PB31(CLK16)</td> <td style="text-align: center;"><input checked="" type="checkbox"/> <input checked="" type="checkbox"/></td> <td style="text-align: center;">2 GE125</td> <td style="text-align: center;">J4</td> </tr> <tr> <td></td> <td></td> <td style="text-align: center;"><input checked="" type="checkbox"/> 1 XUPC1_TXCLKO</td> <td></td> </tr> </table> </p>			J5				<input checked="" type="checkbox"/> 3 RMII_RXCLKODD		PB31(CLK16)	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>	2 GE125	J4			<input checked="" type="checkbox"/> 1 XUPC1_TXCLKO		<p>Selects input for CLK16: RMII_RXCLKODD, GE125, or XUPC1_TXCLKO (J5/J4 is a 4-pin combined Jumper, configured as shown at left)</p> <ul style="list-style-type: none"> • For RMII_RXCLKODD: Connect (JP5) 2-3 • For XUPC1_TXCLKO: Connect (JP5) 1-2 • For GE125: Connect JP4 (default) <p>Note: GE125 is the input clock for UCC1 & UCC1 input 125Mhz clock.</p>
		J5															
		<input checked="" type="checkbox"/> 3 RMII_RXCLKODD															
PB31(CLK16)	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>	2 GE125	J4														
		<input checked="" type="checkbox"/> 1 XUPC1_TXCLKO															
<p>Step 4.c: J6:</p> <p>3 <input checked="" type="checkbox"/> External clock 2 <input checked="" type="checkbox"/> Input MPC8568 clock 1 <input checked="" type="checkbox"/> OnBoard clock</p>	<p>Selects input clock for MPC8568E (onboard or external)</p> <ul style="list-style-type: none"> • For external clock: Connect 2-3 • For internal clock: Connect 1-2 (default) 																
<p>Step 4.d: J14:</p> <p>3 <input checked="" type="checkbox"/> RMII_RXCLKEVEN 2 <input checked="" type="checkbox"/> PD23 (CLK8) 1 <input checked="" type="checkbox"/> UPC2_TXCLK</p>	<p>Selects input for CLK8: RMII_RXCLKEVEN or UPC2_TXCLK</p> <ul style="list-style-type: none"> • For RMII_RXCLKEVEN: Connect 2-3 (default) • For UPC2_TXCLK: Connect 1 - 2. 																
<p>Step 4.e: J16:</p> <p>3 <input checked="" type="checkbox"/> 3.3V 2 <input checked="" type="checkbox"/> TSEC VDD 1 <input checked="" type="checkbox"/> 2.5V</p>	<p>Selects input voltage for TSEC_VDD (3.3V or 2.5V)</p> <ul style="list-style-type: none"> • For 3.3V: Connect 2-3 • For 2.5V: Connect 1-2 (default) 																
<p>Step 4.f: J17:</p> <p>3 <input checked="" type="checkbox"/> 3.3V 2 <input checked="" type="checkbox"/> QE UCC1&2 VDD 1 <input checked="" type="checkbox"/> 2.5V</p>	<p>Selects input power for QE UCC1&2 (MPC8568 QE GETH block) - 3.3V or 2.5V</p> <ul style="list-style-type: none"> • For 3.3V: Connect 2-3 • For 2.5V: Connect 1-2 (default) 																

<p>Step 4.g: J19:</p> <p>3 <input checked="" type="checkbox"/> MAC_HW-CP-G-T-SO5 2 <input checked="" type="checkbox"/> XUPC2_RXD9_PCICLK4 1 <input checked="" type="checkbox"/> XPCI_CLK4</p>	<p>Enables PCI clock to be routed to the expansion board of the PIB</p> <ul style="list-style-type: none"> • For normal operation (no re-routing of PCI clock): Connect 1-2 (default) • To route PCI clock to expansion board: Connect 2-3
<p>Step 5: Assemble and connect the power supply kit.</p> <p>Note: Ensure the power is OFF.</p> <p>Assemble the AC/DC power supply kit:</p> <ul style="list-style-type: none"> • power cable with country-specific wall outlet plug • power supply unit and cable with jack (for board connection) <ol style="list-style-type: none"> 1. Connect the AC/DC power supply cable with 5V jack on the board. 2. Plug the power cable into the wall outlet. 	
<p>Step 6: Perform initial board power up, and check LEDs.</p> <p>Caution: To prevent damage to the JTAG connectivity unit connect the unit only after initial board reset.</p> <ol style="list-style-type: none"> 1. Press the power button (SW5). LD1 briefly displays light. 2. Check for completion of the reset sequence-indicated by the LD2 being constantly lit, as well as LD7, indicating power on. 3. Shut off the power by pressing the power button (SW5) again. 	

LED Locations:



LED Indicators meanings:

No.	Name	Color	LED On	LED Off
LD1	ASLEEP	Green	Device in PORESET or in sleep state	Device not in PORESET or sleep state
LD2	TRIG_OUT	Red	Device ready after PORESET	Device not ready
LD3	DDR2	Green	Power supplied to DDR2	No power supplied to DDR2
LD4	DDR1	Green	Power supplied to DDR1	No power supplied to DDR1
LD5	UCC1	Green	GETH connected to UCC1 active	GETH not active
LD6	Power Fail	Red	Power is not properly supplied to device	If board is active, power is properly supplied to device
LD7	Power On	Green	Board power is ON	Board power is OFF
LD8	UCC2	Green	GETH connected to UCC2 active	GETH not active
LD9	BCSR	Red	Connected to BCSR5 for debugging purposes	
LD10	BCSR	Green		
LD11	BCSR	Amber		
LD12	REG-CFG	Red	Configuration from internal registers	Configuration from DIP switches
LD13	eTSEC3	Green	GETH connected to TSEC1 active	GETH not active
LD14	Power 5V	Amber	5V input active	5V input not active
LD15	Power 12V	Green	12V input active	12V input not active
LD16	eTSEC4	Green	GETH connected to TSEC2 active	GETH not active

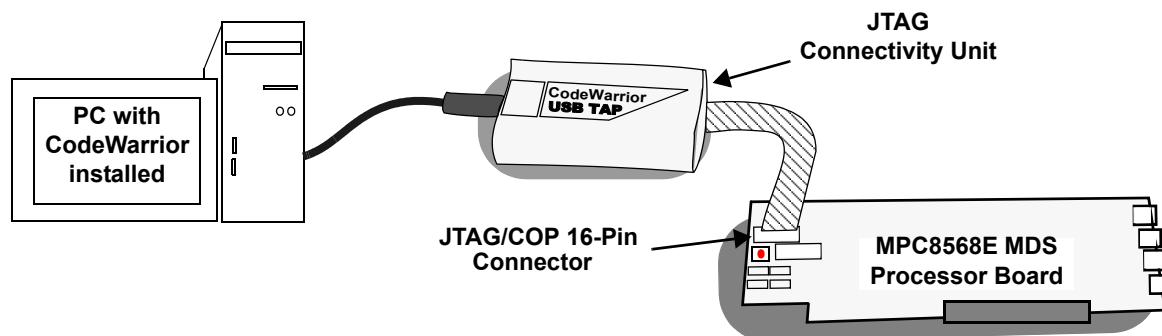
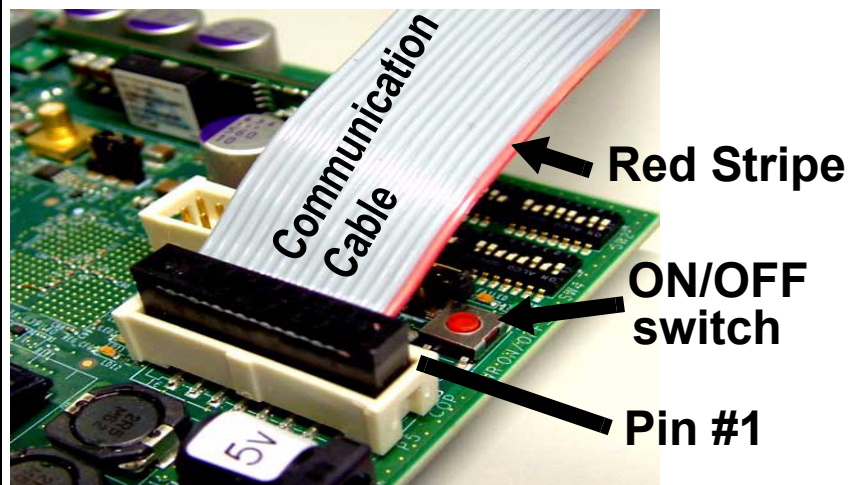
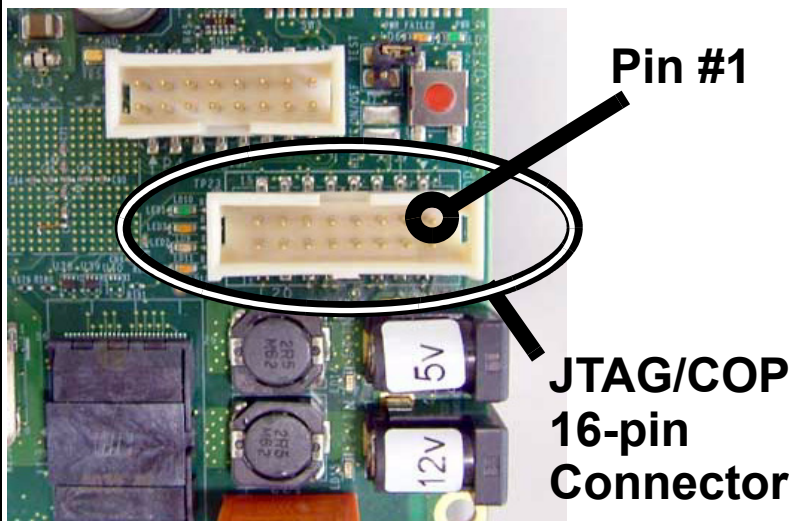
Step 7: Connect the JTAG connectivity unit to the board.

The JTAG connectivity unit ("USB Tap") enables the CodeWarrior software to work with the board.

CAUTION

The "USB-Tap" JTAG connectivity unit must be connected properly to the JTAG/COP 16-pin connector, as shown, otherwise sensitive devices may be damaged.

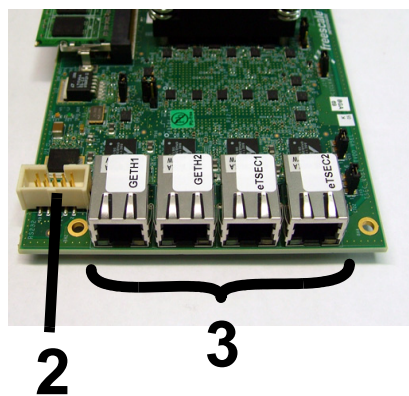
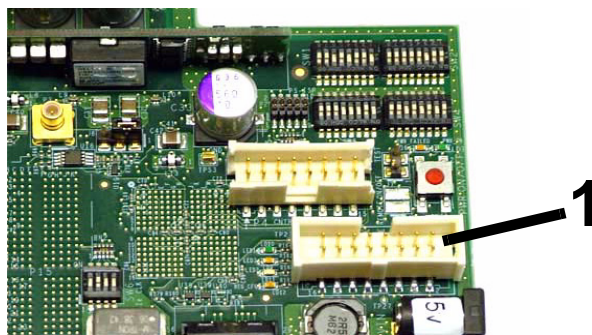
1. Align the red stripe on the communication cable of the USB-Tap JTAG connectivity unit with Pin #1 on the JTAG/COP 16-pin connector.
2. Connect the cable to the JTAG/COP 16-pin connector.
3. Press the ON/OFF switch.
4. Check for completion of the reset sequence (see Step 6 on page 7).



Step 8: Attach remaining cables to the board according to your development needs.

Connect the remaining cables to the board as per user development needs and planned board use:

1. JTAG/COP 16-pin connector for JTAG connectivity unit.
2. Port for the joined Freescale adaptor cable with two RS232 connectors
3. Giga-bit Ethernet ports for the four Ethernet cables with RJ45-8 pin connectors.
4. Continue work according to instructions in the *Kit Configuration Guide*.



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