Freescale Semiconductor
Hardware KIT User Guide

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PowerQUICC MPC8306KIT User's Guide

The MPC8306KIT is a two-board system. The processor board (SOM) features the PowerQUICC processor, MPC8306, and memory interfaces. The other board is called carrier card that comprises external world interfaces terminated on connector/header.

This is a low-cost, high-performance system solution comprising printed circuit board (PCB) assembly plus a software board support package (BSP) distributed in a CD image. This BSP enables the fastest possible time-to-market for development or integration of applications including telecom application, industrial control, networking and low-end embedded application.

This document describes the hardware features of the board including specifications, block diagram, connectors, interfaces, and hardware straps. It also describes the board settings and physical connections needed to boot the MPC8306KIT. Finally, it considers the software shipped with the platform.

Contents

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When you finish reading this document, you should:

- be familiar with the board layout
- understand the default board configuration and your board configuration option
- know how to get started and boot the board
- know about the software and further documentation that supports the board

1 Required Reading

Use this manual in conjunction with following documents:

- *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual (MPC8306RM)*
- *MPC8306 PowerQUICC II Pro Processor Hardware Specifications (MPC8306EC)*
- *Hardware and Layout Design Considerations for DDR Memory Interfaces (AN2582)*

NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used inaccordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

2 Definitions, Acronyms, and Abbreviations

Table 1. Definitions, Acronyms, and Abbreviations

SOM	System on module
PCB	Printed circuit board
BSP	Board support package
POR	Power on reset
GPCM	General-purpose chip-select machine
FCM	Flash control machine
MDIO	Management data Input/Output
COP	Common on-chip processor
RCWLR	Reset configuration word low register
RCWHR	Reset configuration word high register
LTIB	Linux target image builder
USB	Universal serial bus

Table 1. Definitions, Acronyms, and Abbreviations (continued)

FEC	Fast Ethernet controller
UART	Universal asynchronous receiver/transmitter

3 MPC8306KIT Hardware

This section covers the features, block diagram, specifications, and mechanical data of MPC8306KIT (SOM + Carrier) board.

3.1 Features

- CPU: Freescale MPC8306 running at 266/133 MHz; CPU/coherent system bus (CSB)
- Memory subsystem:
  - 128 MByte unbuffered DDR2 SDRAM discrete devices
  - 8 MByte NOR Flash single chip memory
  - 512 MByte NAND Flash memory
  - 256-Kbit serial EEPROM
- Interfaces:
  - 10/100 Base-T Ethernet ports:
    - FEC1 MII and RMII: one 10/100 Base-T RJ-45 interface using Micrel™ KSZ8001 10/100 Base-T PHY
    - FEC2 MII: One 10/100 Base-T interfaced with 5-port switch (PSB6972) on carrier card
    - FEC3 MII: One 10/100 Base-T interfaced using KSZ8001 10/100 Base-T PHY on carrier card
  - USB 2.0 port:
    - USB ULPI signals are interfaced with USB3300 PHY device on carrier card
  - eSDHC Port:
    - One MicroSD card connector
  - Dual UART ports:
    - UART1 supports up to 115200bps (RS232) terminated on 3-pin header on SOM and DB9 connector on carrier card
    - UART2 port converted in to RS-485 and terminated on a DB9 connector on carrier card
  - I^2C
    - I^2C1: Connected to Microchip™ 24LC256 Serial EEPROM
    - I^2C2: Connected to I/O expander PCA9534 on carrier card
  - Flex CAN module
    - CAN: Interfaced with one CAN transceiver (MCZ33902F) on carrier card
- SOM board connectors:
  - 3-Pin power jack connector

  - 3-Pin UART header for console
  - JTAG/COP for debugging
  - 120-pin and 140-pin board-to-board connector
  - 6-pin BDM header for KA2 programming
  - RJ-45 for Ethernet connectivity
  - SD card connector
  - 6-Pin header for boot device (NAND/NOR) selection
- Carrier board connectors:
  - Mini PCIe (x1) card edge connector (not used in MPC8306KIT)
  - PCI card edge connector (not used in MPC8306KIT)
  - Mini PCI card edge connector (not used in MPC8306KIT)
  - Dual stack DB9 connector for RS-232 console and RS-485
  - 2x2 RJ-45 connector for Ethernet switch
  - Unshielded RJ-45 connector for T1/E1
  - MiniAB USB connector
  - Microcontroller UART header
  - Microcontroller BDM header
  - Shielded Rj-45 connector
  - 4-Pin CAN header
  - RJ-11 connector for SLIC/PSTN phone Interface
  - 60-Pin local bus connector on carrier for future expansion
  - 120-Pin and 140-pin board-to-board connector
  - 16-Pin SPI and IEEE 1588 header on carrier for future expansion and measurement
  - 16-Pin GPIO header
- Form factor:
  - SOM: 90 mm X 70 mm
  - Carrier: 170 mm X 170 mm
- 6-Layer PCB(4-layer signals, 2-layer power and ground) routing
- Certification
  - FCC Class-A
  - CE
- Lead free (RoHS)

The following figure shows the MPC8306SOM block diagram.

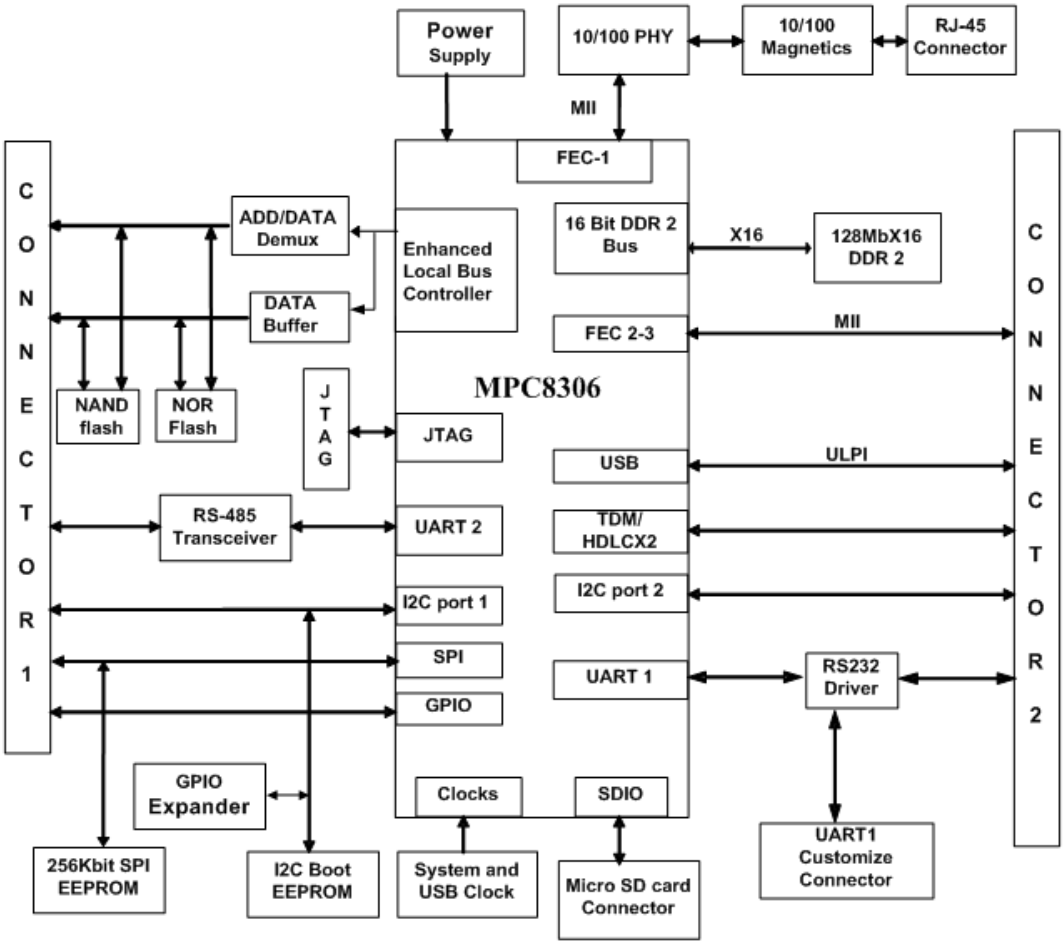

Figure 1. MPC8306SOM Block Diagram

The following figure shows MPC830X carrier block diagram.

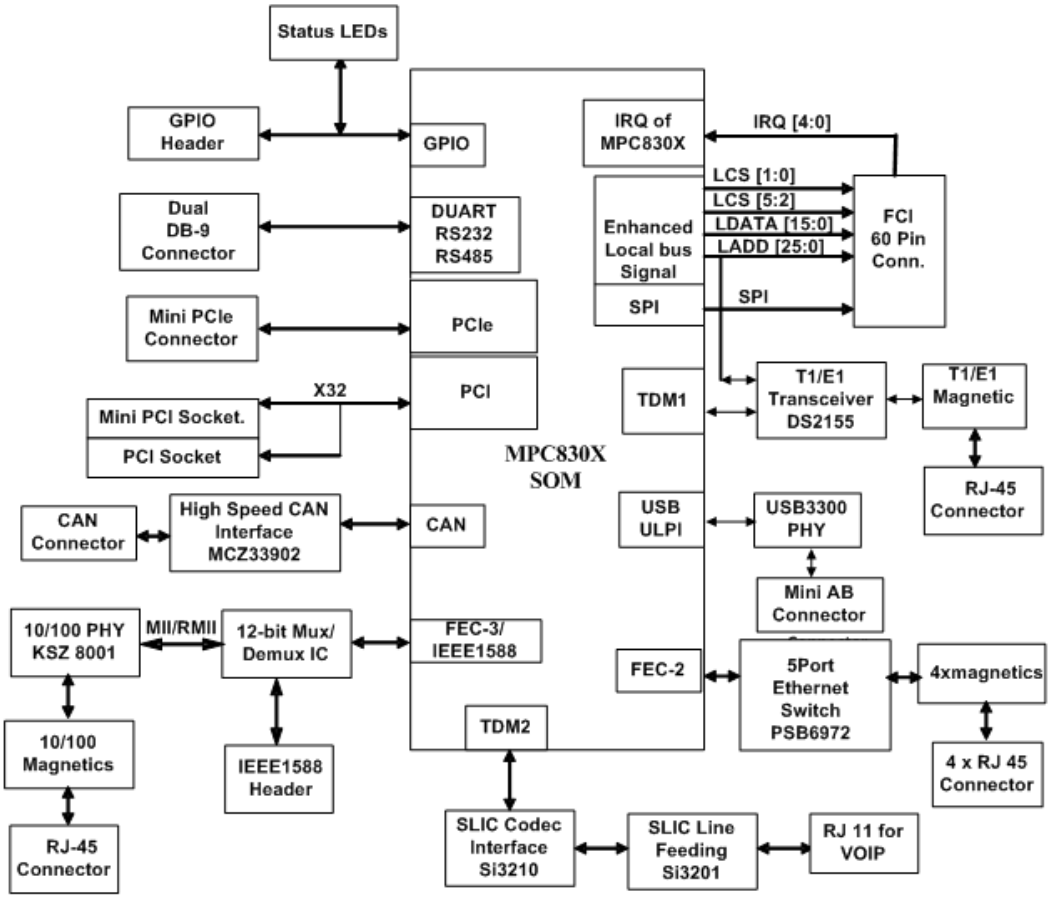

Figure 2. MPC830X Carrier Block diagram

3.2 Specifications

The following table lists the specifications of MPC8306KIT

Table 2. MPC8306KIT Specifications

Characteristics	Specifications
Power Requirement SOM stand-alone MPC8306 KIT	 5 VDC @ 1A 12 VDC @ 2.5A
Communication Processor	MPC8306 running @ 266 MHz
Addressing: Total address range Flash memory (local bus) DDR2 SDRAM	4 GByte (32 address lines) 8 Byte with one chip-select 128 MByte DDR2 SDRAM
Operating temperature MPC8306SOM MPC830X_Carrier	 -40 °C to +85 °C 0 °C to +70 °C

Table 2. MPC8306KIT Specifications (continued)

Characteristics	Specifications
Storage Temperature	-40 °C to +125 °C
Relative Humidity	
PCB dimensions: SOM Board (LxWxT) Carrier Board (LxWxT)	 90 mm x 70 mm x 1.63 mm 170 mm x 170 mm x 1.63 mm

3.3 Mechanical Data

The following figure shows MPC8306LIT dimensions in mm. The MPC8306X carrier board measures 170 mm x 170 mm and MPC8306SOM board measures 90 mm x 70 mm.

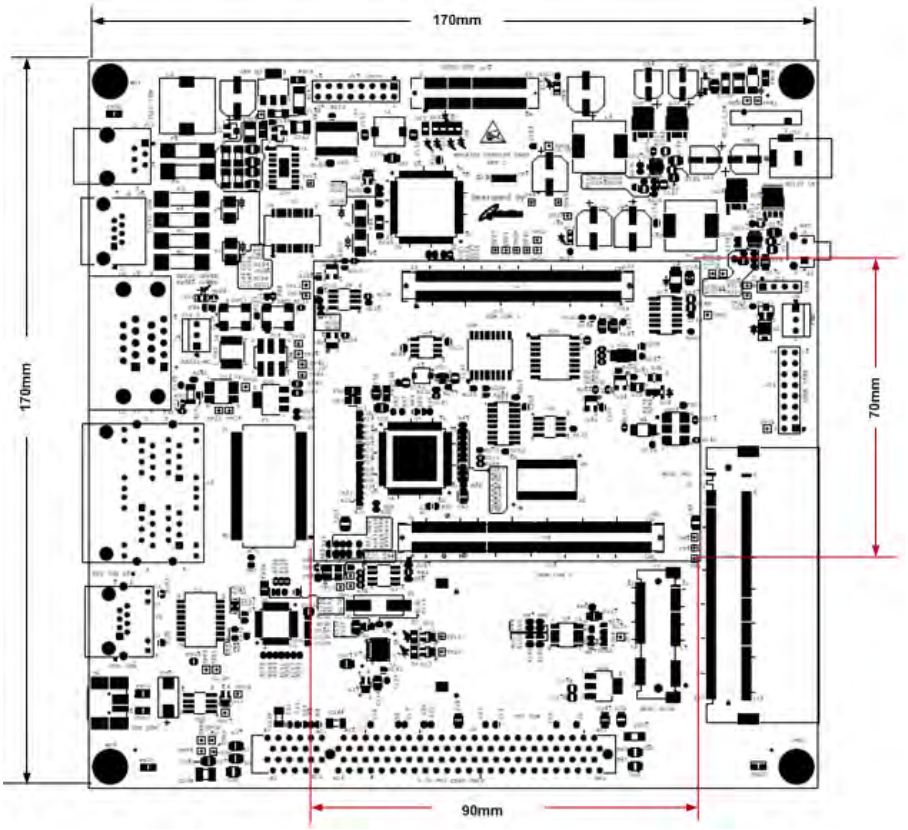

Figure 3. MPC8306KIT dimension

4 Board Level Functions

The board-level functions includes reset, external interrupts, clock distribution, DDR SDRAM controller, local bus controller, I^2C interfaces, SD memory card interface, FEC-1/2/3 interface, CAN interface, RS-232, RS-485, KA2 microcontroller, COP/JTAG interface and USB interface.

4.1 Reset and Reset Configurations

An MPC8306KIT module generates single reset to the MPC8306 and other peripherals on the board. The reset unit provides power-on reset, hard reset, and soft reset signals in compliance with the MPC8306 hardware specification. Figure 4 shows the reset scheme on board.

- MPC8306_POR# (power on reset) input is generated by TI power management IC TPS65023. When MR# (manual reset) is deasserted and 3.3 V is ready, the TPS65023 internal timeout guarantees a minimum reset active time of 100 ms before PORESET# is deasserted. Push button reset interfaces the MR# signal with debounce capability to produce a manual master PORESET#. MPC8306 POR# input is also generated by MC9RS08KA2 microcontroller device by monitoring I^2C-I/O expander GPIO status based on loading of reset configuration word from boot device on SOM board.
- HRESET# (hard reset) is generated either by the MPC8306 or the COP/JTAG port.
- COP/JTAG port reset provides convenient hard-reset capability for a COP/JTAG controller. The HRESET# line is available at the COP/JTAG port connector. The COP/JTAG controller can directly generate the hard-reset signal by asserting this line low. As shown in Figure 4, the COP can independently assert HRESET# or TRST#, while ensuring that the MPC8306 can drive HRESET# as well.
- Carrier_RST# is used to provide power on reset signal to the devices on carrier card. This signal is generated by ANDing Carrier_POR# and HRESET# signal generated by MPC8306.

The following figure shows the reset circuitry of MPC8306KIT.

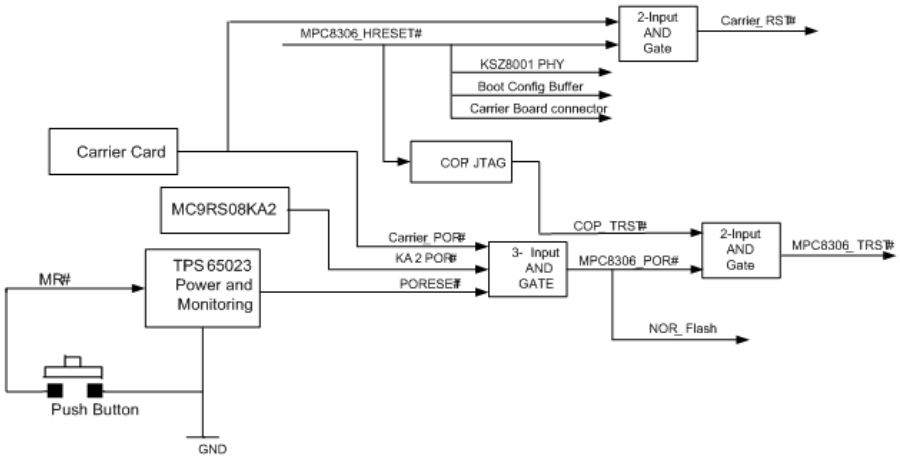

Figure 4. Reset Circuitry of MPC8306KIT

4.2 External Interrupts

The following figure shows the external interrupt circuitry of MPC8306KIT.

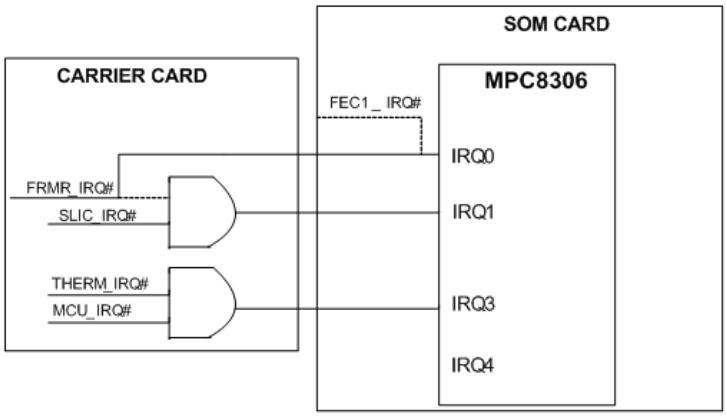

Figure 5. Interrupt Circuitry of MPC8306KIT

- All external interrupt signals are pulled up by 4.7 K resistors.
- Either PHY (KSZ8001) Interrupt (FEC1_IRQ#) or FRMR_IRQ# will be connected to IRQ0# of MPC8306. The selection between FEC1_IRQ# and FRMR_IRQ# can be done through resistor mount/No mount. Default IRQ0 is connected to FRMR_IRQ#.
- Option provided to connect SLIC and framer device interrupt (FRMR_IRQ#) to be ANDed and given to IRQ1# of MPC8306. By default, only SLIC interrupt will be connected to IRQ1.
- MCU Interrupt (MCU_IRQ# and thermal interrupt (THERM_IRQ#) are ANDed and given to IRQ3 of MPC8306.

4.3 Clock Distribution

The following figure shows clock distribution on SOM board.

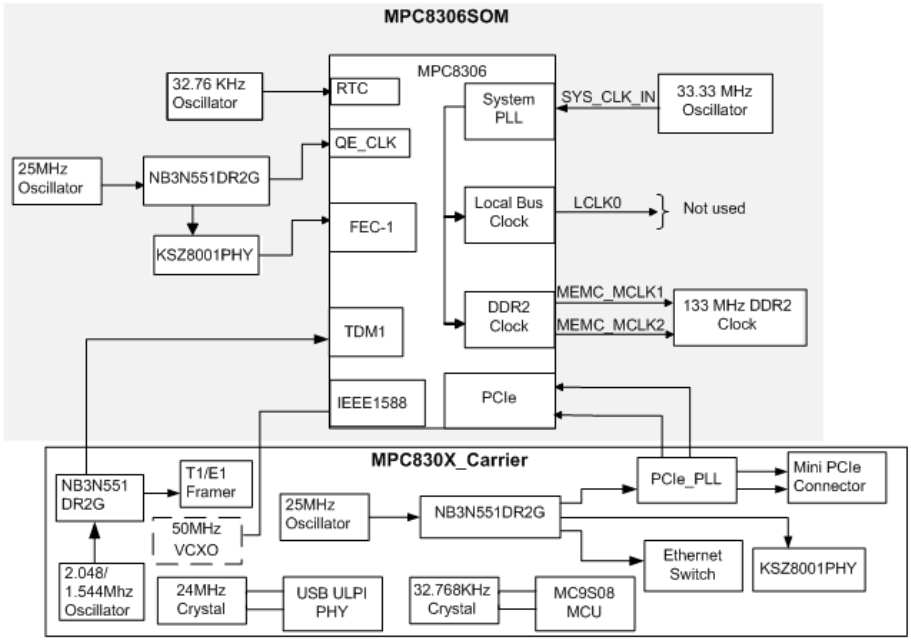

Figure 6. Clock Distribution on MPC8306KIT

The following table shows the clock distribution on MPC8306KIT (SOM + Carrier) board.

Table 3. MPC8306SOM and Carrier Clock distribution

Clock Frequency	Module	Generated by	Description
33.33 MHz	MPC8306 CLKIN	33.33 MHz OSC	The MPC8306 uses CLKIN to generate the internal system PLL. The CSB clock is generated by the internal PLL and is fed to the e300 core PLL for generating the e300 core clock.
133 MHz	DDR2 SDRAM	MPC8306	The DDR memory controller is configured to use the 2:1 mode CSB to DDR for the DDR interface (DDR266). The local bus clock uses 1:1 local to CSB clock, which is configured by hard reset configuration or SPMR register.
32.76 KHz	Real Time Clock	32.76 KHz OSC.	Clock for RTC
25 MHz	MPC QE and FEC1 PHY Clock	25 MHZ OSC and 1:4 Clock buffer	The 25-MHz oscillator provide the clock for MPC8306 QUICC Engine and FEC1 PHY KSZ8001.
2.048/1.544 MHz	T1/E1 Clock	2.048/1.544 MHz OSC and 1:4 Clock buffer	The 2.048/1.544 MHz oscillator provided clock for T1/E1 framer on carrier card and MPC8306TDM section.
24 MHz	ULPI external USB PHY	24 Mhz Crystal	Clock for ULPI USB PHY USB3300
25MHz	4-Port Ethernet Switch and FEC3 PHY	25 MHz OSC	The 25-MHz oscillator provides the clock for the 4-port Ethernet switch.

Table 3. MPC8306SOM and Carrier Clock distribution (continued)

Clock Frequency	Module	Generated by	Description
32.768 KHz	Microcontroller	32.768 KHz Crystal	MC9S08QG8CDT Microcontroller on Carrier.
50 MHz	IEEE 1588 Clock (TMR Clock)	50MHz Oscillator /50MHz VCXO	50 MHz is used by IEEE 1588 Module. It is VCXO controlled by SPI DAC.

4.4 DDR2 SDRAM Controller

The MPC8306 processor uses DDR2 SDRAM as the system memory. The DDR2 interface uses the SSTL2 driver/receiver and 1.8 V power. A Vref 1.8V/2 is needed for all SSTL2 receivers in the DDR2 interface. Since DDR2 SDRAM chip operates at 1.8 V and uses SSTL2 interface, it will directly interface with the MPC8306 without any level translation. The 1.8 V interface supply is provided by an on-board voltage regulator. VREF, which is half the interface voltage (0.9 V), is provided by a voltage divider of the 1.8 V for voltage tracking. SOM board willbe configured to run DDR2 memory @ Max 133MHz, that is, DATA RATE 266 MHz. The following figure shows the DDR2 SDRAM connection.

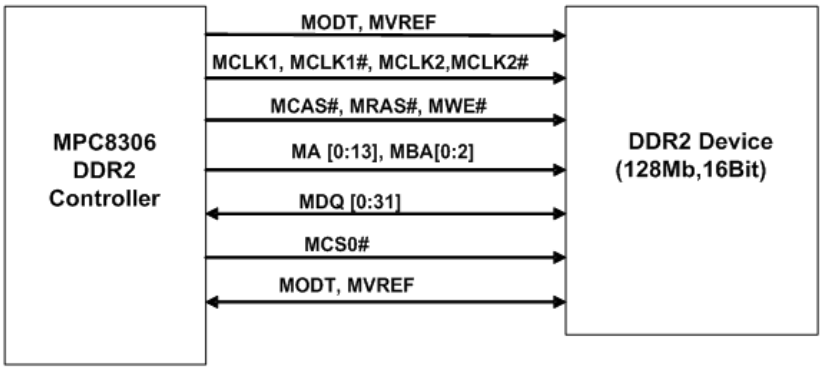

Figure 7. DDR2 SDRAM Connection

4.5 Local Bus Controller

The MPC8306 local bus controller has multiplexed address and data lines LAD[0:15] and non-multiplexed address lines LA[16:25]. Thus, address latch and data buffer need to be used to interface standard memory devices for non-multiplexed address and data bus.

The following modules are connected to the local bus of MPC8306:

- 8 MByte NOR Flash memory
- 512 MByte NAND flash memory
- T1/E1 framer local bus interface
- Local bus signals are terminated in a 60-pin connector on carrier card for future expansion

4.5.1 NOR Flash Memory Interface

This section describes NOR Flash memory interface to MPC8306 local bus. Through the general-purpose chip-select machine (GPCM), the MPC8306 SOM provides an 8 MByte of Flash memory using a

chip-select and local bus control signals. Local bus address and data are multiplexed, so a address latch and a data buffer is used between MPC8306 and NOR Flash interface.

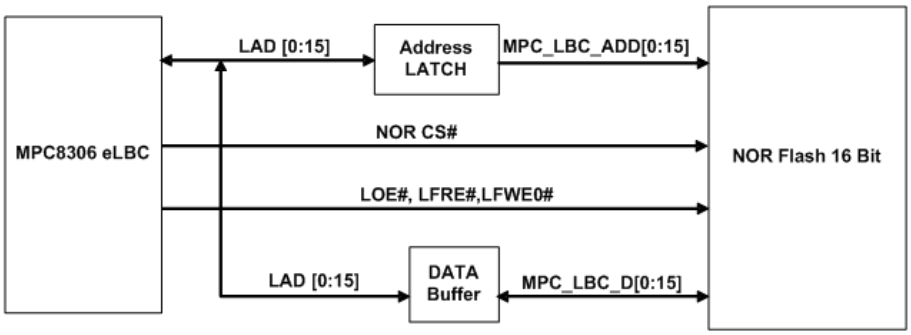

Figure 8. NOR Flash Interface Block Diagram

NOTE

NOR_CS# can be either CS0# or CS1# by J3 header–jumper settings; default is CS0#.

4.5.2 NAND Flash Memory Interface

This section describes NAND Flash memory interface to MPC8306. The MPC8306 has native support for NAND Flash memory through its NAND flash control machine (FCM). eLBC interface of MPC8306 provides glueless interface to NAND Flash memory. MPC8306 supports 16-bit wide eLBC interface. NAND Flash interface of SOM card is 8-bit wide.

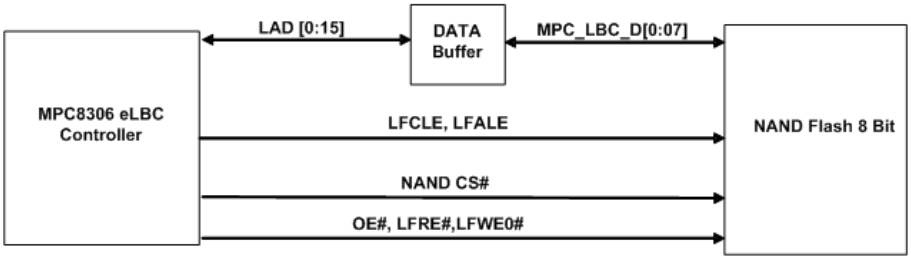

Figure 9. NAND Flash Interface Block Diagram

NOTE

NAND_CS# can be either CS0# or CS1# by J3 header–jumper settings; default is CS1#.

4.5.3 DS2155 Parallel Port Interface

T1/E1 transceiver (DS2155) is having an 8-bit parallel port interface for configuration purpose. DS2155 parallel port is interfaced with MPC8306 local bus controller in GPCM mode as shown in the following figure. DS2155 is interfaced on CS2# of MPC8306.

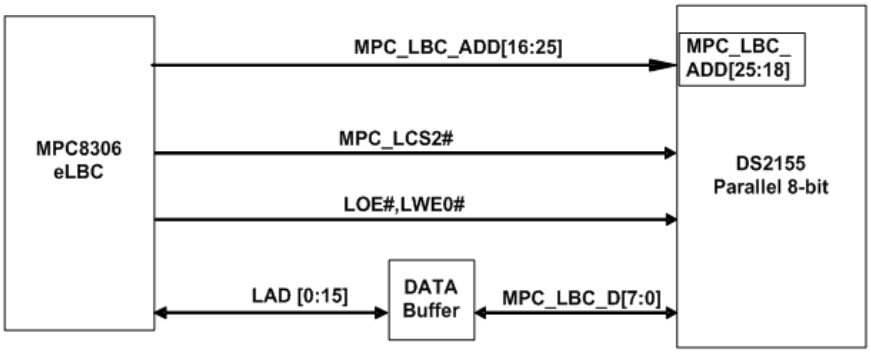

Figure 10. External Cable Connection for the Stand-alone SOM Boot Mode

4.6 I²C Interfaces

The MPC8306 has two I²C interfaces: I²C1 and I²C2. All I²C lines are pulled up with a 4.7-K resister.

4.6.1 I²C1 Interface

AS per MPC8306KIT specification, following components are interfaced on the I²C1:

- Serial EEPROM 24LC256-I/SM at address 0x50
- 4-Bit I²C I/O expander PCA9536 at address 0x41
- MCU MC9S08QG8CDT on carrier card through board-to-board connector
- DAC AD5301BRMZ at address 0x48 on carrier card through board-to-board connector
- Temperature Sensor device LM75 is connected at 0x90 address.

The following figure shows the interface block diagram.

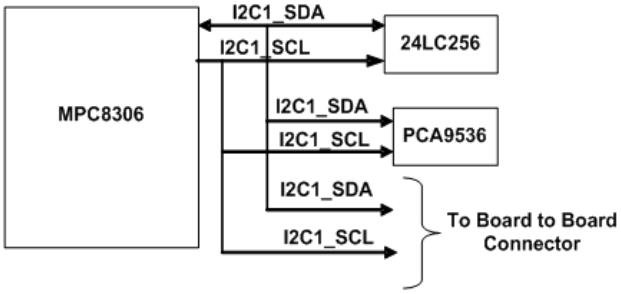

Figure 11. I²C1 Interface Block Diagram

The I²C EEPROM is used to store the configuration registers values and Booting purpose during Boot Sequencer mode. Boot sequencer mode is selected at power-on reset by the BOOTSEQ field of the high-order reset configuration word. If boot sequencer mode is selected, the I²C module communicates with one or more EEPROMs through the I²C interface.

I²C1 is also connected to the MC9S08QG8CDT on carrier card through board-to-board connector. MC9S08QG8CDT Microcontroller unit is used for the fan control.

PCA9536 4-bit I/O expander on I2C1 line is used to provide on-board general purpose I/O for mux/demux control and boot status GPIO.

4.6.2 I2C2 Interfaces

I2C2 is connected to the following devices:

- I/O expander—1 PCA9534DW at address 0x20
- I/O expander—2 PCA9534DW at address 0x21

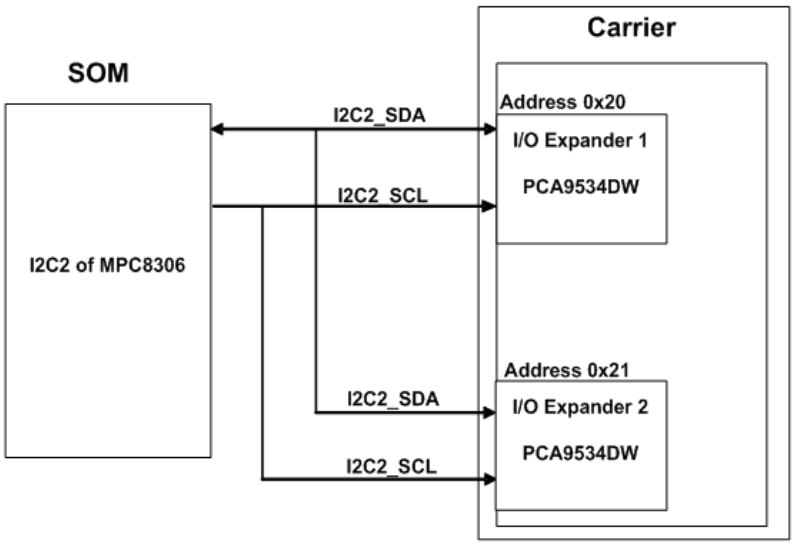

Figure 12. I2C2 Interface Block Diagram

I2C2 is used for an 8-bit I/O expander PCA9534DW on carrier card. PCA9534DW is 8-bit I2C to parallel port expander. PCA9534DW provides GPIO expansion for most microcontroller families via the I2C interface [serial clock (SCL), serial data (SDA)]. There are two I/O expanders on carrier card providing a total 16-bit GPIO.

Table 4. I2C I/O Expander-Based GPIO Signal Assignment on Carrier and SOM Card

I/O Port	Signal Name	Description
SOM Board GPIO		
I/O Expander (PCA9536) U24 GPIO		
IO0	CAN/SD_MUX_CTL	CAN and SDIO signals Mux/demux Selections
IO1	UART / LBC_MUX_CTL	UART and LBC chip select signals mux/demux selections
IO2	BOOT_STAUS_GPIO	GPIO for checking processor boot status
IO3	CARRIER_PRESENT	Detect stand-alone/carrier card availability
Carrier Board GPIO		

Table 4. I2C I/O Expander-Based GPIO Signal Assignment on Carrier and SOM Card (continued)

I/O Port	Signal Name	Description
I/O Expander-1 (U21) GPIO		
P0	MPC_SLIC_SPI_CS#	SLIC SPI chip select
P1	MPC_EEPROM_SPI_CS#	SPI EEPROM chip select (unused)
P2	SPI_MUX_CNTL	SPI EEPROM and MPC8306 SPI mux selection (unused)
P3	FEC3_IEEE1588_MUX_CNTL	FEC3 and IEEE1588 mux/demux control
P4	PCIe_WAKE#	PCIe card wake signal
P5	MPC_GPIO_CAN_EN	CAN transceiver control
P6	MPC_GPIO_CAN_STY#	CAN transceiver control
P7	MPC_GPIO_CAN_ERR#	CAN transceiver control
I/O Expander-2 (U39) GPIO		
P0	SW_UPDATE_RST#	Switch software update signal (unused)
P1	I^2C_EXPND_GPIO1	Terminated on LED D9
P2	I^2C_EXPND_GPIO2	Terminated on LED D10
P3	I^2C_EXPND_GPIO3	Terminated on LED D11
P4	I^2C_EXPND_GPIO4	Terminated on LED D12
P5	I^2C_EXPND_GPIO5	Terminated on LED D8
P6	USB_SLIC SEL	USB and SLIC mux/demux selections
P7	I^2C_EXPND_GPIO7	Terminated on header J17

4.7 SPI Interface

SPI interface is connected to following devices on MPC8306KIT:

- Boot SPI EEPROM Flash on SOM card
- Si3210 SLIC on carrier card

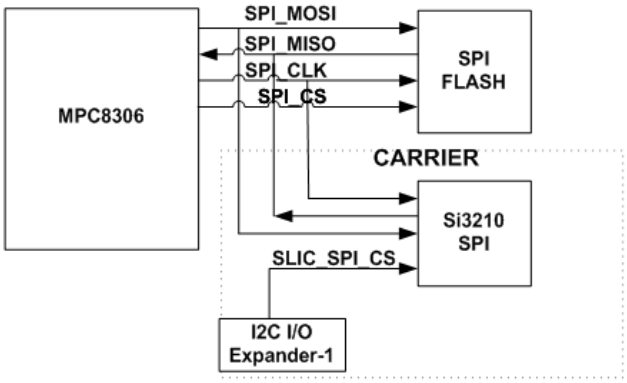

Figure 13. SPI Interface Block in MPC8306KIT

The SPI EEPROM is used to store the configuration registers values for booting purpose. During normal operation, the SPI EEPROM is not used.

Si3210 PROSLIC is being configured through SPI interface of MPC8306. Chip select of SLIC SPI interface is generated through PCA954DW I/O expander on carrier card as shown in Figure 13.

4.8 Micro SD Card Interface

MPC8306 has on-chip SD card controller (eSDHC controller), which provides glueless interface to removable memory storage interfaces such as SDIO and MMC. The SD card can transfer data up to maximum of 33.25 MHz clock speed. The card insertion detect and the write protect signals of connector are mechanical switched signals. These signals are connected to MPC8306 GPIO/WP.

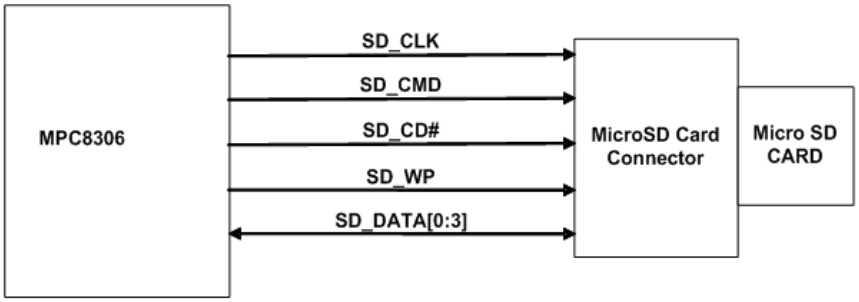

Figure 14. SD Card Interface Block Diagram

NOTE

Power-down board/system while inserting and removing SD card.

4.9 USB Interface

MPC8306 supports USB2.0 host/device/OTG interface through external USB ULPI PHY. As shown in the following figure, USB signals from the MPC8306 SOM go to the carrier card through the board-to-board connector.

The USB connection on MPC8306KIT is shown in the following figure.

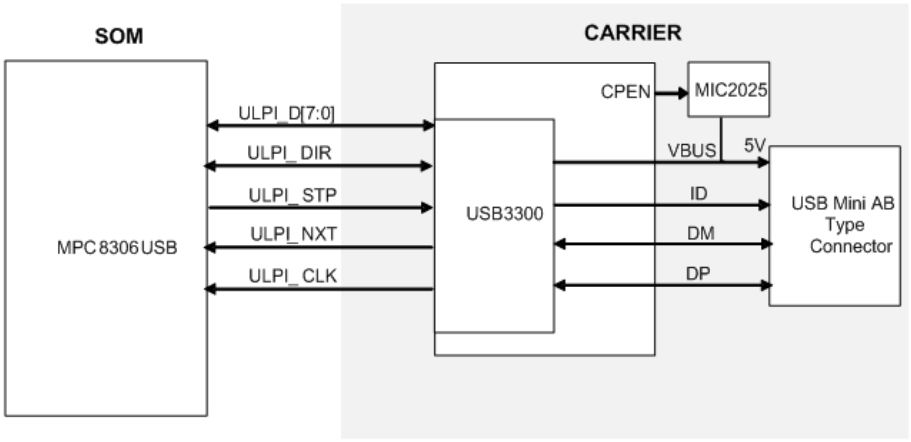

Figure 15. USB Interface Block Diagram

NOTE

USB interface is multiplexed with TDM2 interface. This limitation is due to pin muxing of 8306SoC. So either USB or TDM2 (SLIC) interface can be used at a time. For configuration of either USB or TDM2 (SLIC) interface, see LTIB documentation.

4.10 FEC 10/100 Base-T Interface

MPC8306 have three fast Ethernet controller named as FEC1, FEC2, and FEC3. The details of FEC-1, FEC-2, and FEC-3 port are:

- FEC-1 port is interfaced on SOM board working in MII mode
- FEC-2 port is interfaced to 5-port Ethernet switch on carrier board through board-to-board connector
- FEC-3 port is interfaced to 10/100Mbps PHY (MII Mode) on carrier board through board-to-board connector

4.10.1 FEC1 Interface

The FEC1 port is used to provide network connectivity and allow data transfer over Ethernet on MPC8306SOM board. The external PHY KSZ8001 is connected to MPC8306 FEC1 port through MII interface. FEC1 controls the flow of data packet from the system to external PHY. The MDIO (management data input/output) module controls PHY configuration and status monitoring as shown in the following figure. The PHY address connected to FEC1 is 0x11.

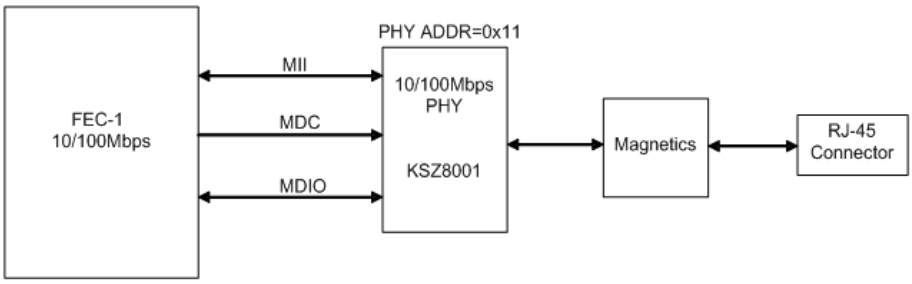

Figure 16. FEC1 Interface Block Diagram

4.10.2 FEC2 Interface

FEC2 port of MPC8306 is connected with 5-Port Ethernet switch (PSB6972) through MII interface. One MII port of switch is connected to FEC2 of MPC8306 on carrier card. The FEC2 signals from the 8306 SoC goes on carrier through carrier–SOM board-to-board connector and interfaced with 5-Port switch as shown in the following figure. The MII port of Ethernet switch is configured to operate in "Reverse MII" mode for MAC-to-MAC connection.

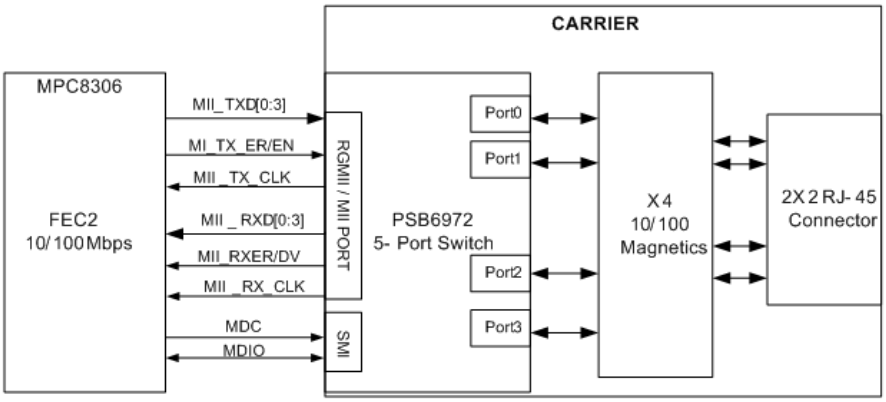

Figure 17. FEC2 Interface Block Diagram

The MDIO modules is used for switch configuration and status monitoring. The downlink of switch is 4 10/100 ports terminated in 2x2 RJ-45 connector on carrier card through magnetic as shown in Figure 17.

NOTE

Switch registers are accessed through SMI interface of switch and MDC/MDIO interface of MPC8306. Becauseof register addressing scheme of Ethernet switch over SMI interface, PHY address range from 0x00 to 0x0F of MDC/MDIO interface is blocked. Hence any external PHY used with this switch need to be addressed from 0x10 to 0x1F.

4.10.3 FEC3 Interface

FEC3 port of MPC8306 is connected to an external PHY KSZ8001 on carrier card over MII interface and terminated to an RJ-45 connector as shown in Figure 18. This provides additional network port

connectivity on carrier card. FEC3MII port of MPC8306 is multiplexed with IEEE 1588 signals, so 12-bit mux/demux IC is used on carrier card for interface selection. By default, MII interface is selected. MII signals travel through board-to-board connector on carrier card. The MDIO module controls PHY configuration and status monitoring.

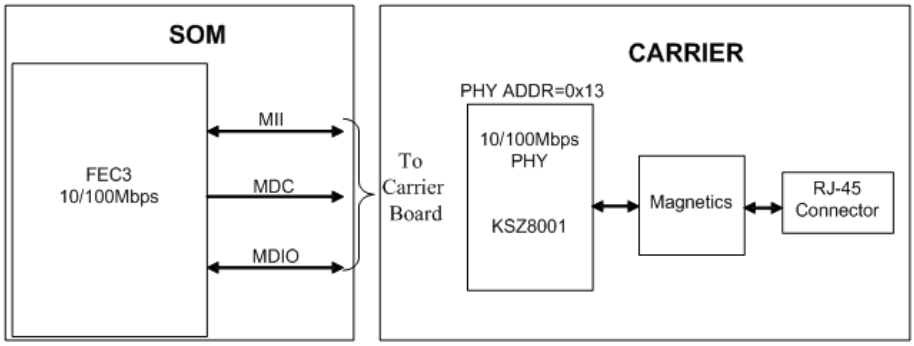

Figure 18. FEC3 Interface Block Diagram

NOTE

Insert SOM card properly on carrier card. Improper insertion of SOM card can result in Ethernet connectivity issue on FEC2 and FEC3.

4.11 DUART Interface

DUART provides support for RS232 and RS485 connectivity. UART1 is used for RS232 signaling and UART2 is for RS485 signaling.

MAX3221, RS232 Transceiver, is used to provide RS232 connectivity on UART-1 port. UART-2 port is used to provide RS485 connectivity through SN65HVD33D—a RS485 driver/receiver. UART2 port is muxed with CS#4 and CS#5 of local bus,so multiplex switch is used for selection of interface. By default, UART-2 port is selected.

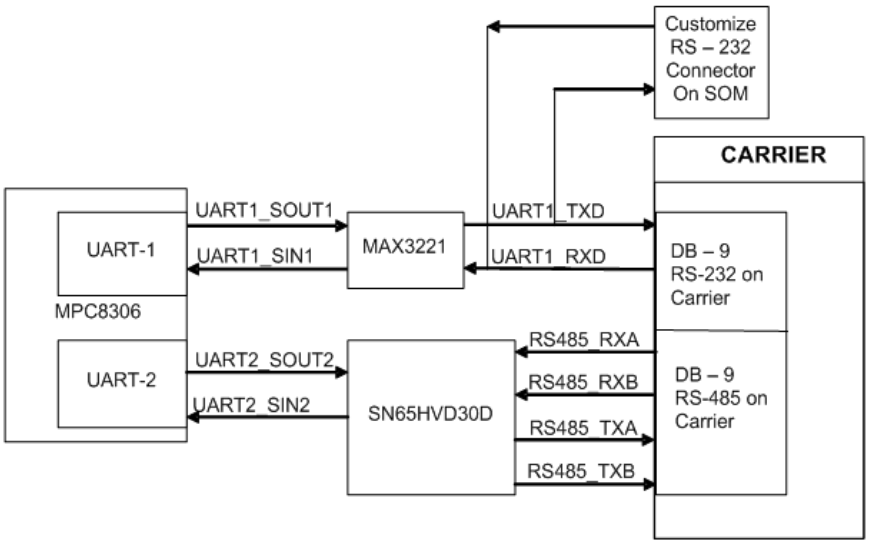

Figure 19. DUART Interface Block Diagram

UART1 (RS232) is terminated on SOM (3-pin header) and carrier card (DB9 connector). RS232 port is used as Debug/Console port for processor and is configured at 115200 baud rate.

Carrier card has dual-stacked DB9 connector. Upper port provides RS232 connectivity and lower port RS485 connectivity.

4.12 Flex CAN Interface

MPC8306 is having four FlexCAN bus controller—CAN0 to CAN3. These CAN signals are brought to carrier card through board-to-board connector.

CAN0 port is connected to CAN PHY (MCZ33902) on carrier card and then terminated on a 4-pin header while other CAN signals are terminated on test points on carrier card.

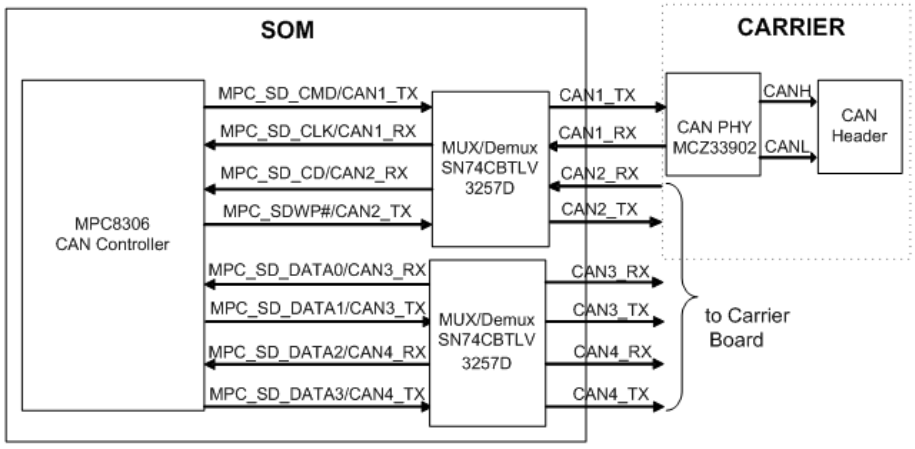

Figure 20. CAN BUS Interface

MPC8306 CAN signals are multiplexed with SDIO interface; so SN74CBTLV3257 - 4:1 mux/demux IC is used for selection of interface. Thus, either CAN or SDIO interface is used at a time through software switch selection.

4.13 TDM Interface

MPC8306 is having two TDM/HDLC ports available. In MPC8306KIT, one TDM port (TDM-1) is interfaced with T1/E1 transceiver (DS2155) and another TDM port (TDM-2) is interfaced with SLIC codec as shown in the following figure.

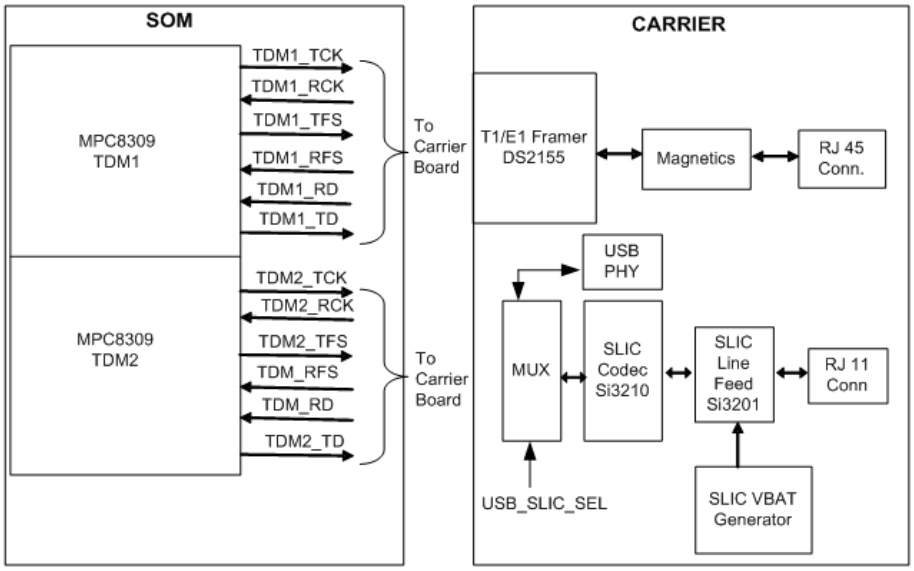

Figure 21. TDM Interface

TDM-1 port of MPC8306 is interfaced with T1/E1 transceiver IC DS2155. It works either in T1 or in E1 mode as per external input clock and configuration. For E1 mode, DS2155 requires 2.048 MHz clock and for T1 mode, a 1.544 MHz clock. Default operation of framer is E1 with input clock to DS2155 at 2.048 MHz.

NOTE

For switching between T1 and E1 mode,that is, input clock change, a small hardware change is required as mentioned in Section 4.13.1, "T1_E1 Clock Change."

TDM-2 port of MPC8306 is interfaced with SLIC Codec IC Si3210. Line feeding IC Si3201 is also required for analog telephone interface.Analog telephone interface requiresa line voltage of –48 V, which is being generated using line interface IC Si3201 and VBAT generator circuit as shown in Figure 21. As shown in the figure, TDM2 interface is multiplexed with USB interface. So either USB or TDM2 (SLIC) interface can be used at a time. The selection of interface can be done by I^2C I/O expander. See LTIB documentation for more information.

4.13.1 T1_E1 Clock Change

As mentioned in Section 4.13, "TDM Interface," T1/E1 framer supports E1 mode by default. For T1 mode configuration, input clock to framer needs to be changed to 1.544 MHz.

For changing framer input clock to 1.544 MHz, following changes need to be done:

- Top side: Make R137 as NU and mount R133

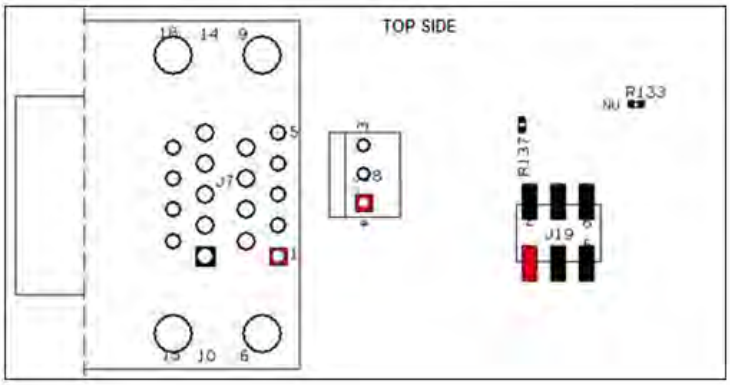

Figure 22. T1_E1 Clock Mode Change Top Side

4.14 COP/JTAG Port

The common on-chip processor (COP) is part of the MPC8306 JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a Freescale JTAG emulator for extensive system debugging.

The setup of USB port JTAG emulator is shown in the following figure.

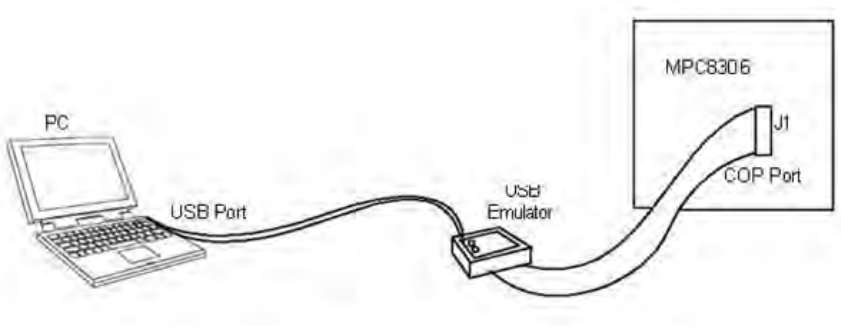

Figure 23. USB Port JTAG Emulator

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. The pinout of this connector is shown in the following figure.

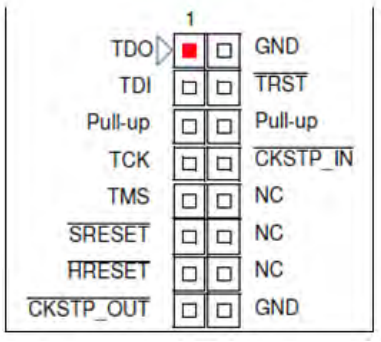

Figure 24. MPC8306SOM COP Connector

5 Connectors, Switches, and LEDs

The following table summarizes the list of connectors, jumpers, switches, and LEDs that are used in MPC8306KIT (SOM + Carrier) board.

Table 5. Connectors

Reference	Description
SOM Board Connectors	
J1	16-Pin JTAG connector
J2	Background debug connector for KA2 programming\
J3	Boot mode selection jumper for NAND and NOR
J4	RJ-45 connector
J5	Micro SD card connector customize RS - 232 connector
J6	Customize RS - 232 connector
J7	120-Pin board-to-board connector
J9	2.5 mm power jack for 5 V supply
J10	140-Pin board-to-board connector
Carrier Board Connectors	
J1	Mini PCI Express connector (not used in MPC8306KIT)
J2	PCI card edge connector (not used in MPC8306KIT)
J3	MiniPCI card edge connector (not used in MPC8306KIT)
J4	2x2 RJ-45 Ethernet switch connector
J5	Unshielded RJ-45 connector for T1/E1 line

Table 5. Connectors (continued)

Reference	Description
J6	USB Mini AB connector
J7	Dual UART connector UART1(top), UART2(bottom)
J9	Shielded RJ-45 connector for FEC-3
J10	4-Pin CAN header
J11	RJ-11 phone jack connector
J12	2.1mm power jack for 12 V supply
J13	120-Pin board-to-board connector
J14	140-Pin board-to-board connector
J15	Local bus connector
J16	IEEE 1588 signal header-optional
J17	GPIO/SPI header

Table 6. Switches

Reference	Description
SOM Board Switches	
SW1	2-Pin Reset switch
Carrier Board Switches	
S3	Reset switch

Table 7. LEDs

Reference	Description
SOM Board LEDs	
D13	5 V indicator LED
D14	3.3 V indicator LED
Carrier Board LEDs	
D14	5 V indicator LED
D15	3.3 V indicator LED
D8	GPIO 5 LED
D9	GPIO 1 LED
D10	GPIO 2LED

Table 7. LEDs (continued)

Reference	Description
D11	GPIO 3LED
D12	GPIO 4LED

5.1 SOM Board Connectors

5.1.1 COP/JTAG Connector

JTAG connector J1 allows user toconnect COP/JTAG–based emulator to MPC8306 for debugging. Pinout detail of the COP/JTAG connector is mentioned in the following table.

Table 8. JTAG Connector Pin Assignment

Pin #	Signal	Pin #	Signal
1	TDO	2	KEY1
3	TDI	4	TRST#
5	QREQ#	6	VDD_SENSE
7	TCK	8	CHKSTP_IN#
9	TMS	10	NC1
11	SRESET#	12	NC2
13	HRESET#	14	KEY2
15	CHKSTP_OUT#	16	GND

5.1.2 Background Debug Connector for KA2

MPC8306 SOM has connector J2 used for KA2 microcontroller programming as shown in the following figure.

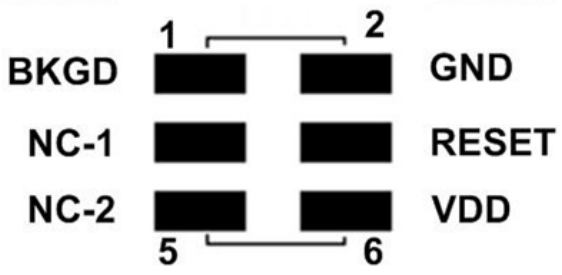

Figure 25. KA2 Programming Header

The following table shows KA2 programming header.

Table 9. Background Debug Connector Pin Detail

Pin#	Name	Pin#	Name
1	BKGD	2	GND
3	NC–1	4	RESET
5	NC–2	6	VDD

5.1.3 Micro SD Card Connector

The microSD card socket (J5) for SD memory card installation is located near to the customized UART connector of the board. The following figure shows how to insert SD card to the board.

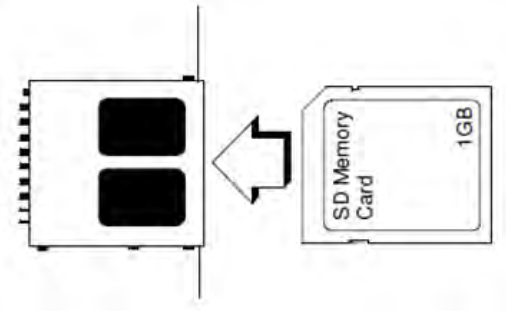

Figure 26. Insertion of SD Memory Card to the Board

5.1.4 Customized RS232 Connector (J6)

MPC8306 SOM board has RS232 customized cable todebug MPC8306 SOM in stand-alone mode. Pinout detail of the customized RS232 connector is mentioned in Table 10.

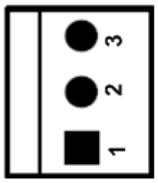

Figure 27. Customized UART Connector

Table 10. Customized UART Serial Connector Pin Assignment

Pin#	Name	Description
1	GND	Ground
2	TX	Transmit

Table 10. Customized UART Serial Connector Pin Assignment (continued)

Pin#	Name	Description
3	RX	Receiver

5.1.5 Ethernet Connector (J4)

MPC8306 SOM has Ethernet connector (J4) to provide network connectivity through FEC1 SOM stand-alone SOM operation mode.

5.1.6 NAND/NOR Chip Select Header (J3)

A six-pin SMD header (J3) is mounted on SOM to select the CS#0:1 for NOR/NAND Flash using two-pin short link jumper.

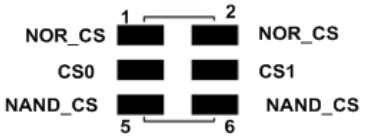

Figure 28. NAND_NOR Chip selects Header

Header J3 is used to select the chip select for NAND and NOR device using two-pin short link jumper as per the following table.

Table 11. Jumper Settings for NAND and NOR Device

Sl. No	Shorting	Description
1	J3.3 and J3.1	8306 CS0 is connected to NOR chip select
2	J3.3 and J3.5	8306 CS0 is connected to NAND chip select
3	J3.4 and J3.2	8306 CS1 is connected to NOR chip select
4	J3.4 and J3.6	8306 CS1 is connected to NAND chip select

NOTE

While configuring NOR on CS0, connect NAND chip select to CS1 and vice versa.

5.2 Carrier Board Connectors

5.2.1 Dual UART Connector (J7)

Carrier board serial interfaces are available at connector J7. It is a dual-stacked DB9 female connector. The upper port is UART1 (RS232) and the lower port is UART2 (RS485). The following figure shows the dual DB9 female connector front view.

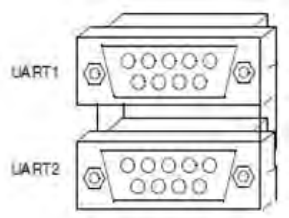

Figure 29. Dual UART Connector

5.2.2 CAN Header J10

A four-pin header (J10) is provided for terminating CAN signal on carrier card as shown in the following figure.

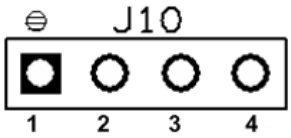

Figure 30. CAN Header

Table 12. CAN Header Pin Assignment

Pin #	Name	Description
1	CANH	CAN High
2	CANL	CAN Low
3	GND	Ground
4	NC	No Connect

5.2.3 RJ-11 (Phone) Connector J11

A six-pin RJ-11 is provided on carrier card to terminate the signal from SLIC line interface IC Si3201 to connect external PSTN phone.

Table 13. RJ-11 Connector Pin Assignment

Pin #	Name	Pin #	Name
1	NC-1	4	TIP
2	NC-2	5	NC-3
3	RING	6	NC-4

5.2.4 T1/E1 Connector J5

Line side interface of T1/E1 framer is terminated on an unshielded 8-pin RJ-45 connector.

Table 14. T1_E1 Connector Pinout

Pin #	Name	Description
1	T1_E1_RXN	T1/E1 Receive Low
2	T1_E1_RXP	T1/E1 Receive High
3	NC-2	No Connect
4	T1_E1_TXN	T1/E1 Transmit Low
5	T1_E1_TXP	T1/E1 Transmit High
6	NC-1	No Connect
5	NC-3	No Connect
6	NC-4	No Connect

5.2.5 FEC-3 Ethernet Connector J9

Carrier RJ-45 connector J9 is used to provide network connectivity to processor through FEC-3 in MCP8306.

5.2.6 Ethernet Connector (J4)

A four-port (2x2) Ethernet connector (J4) is provided on the carrier card for Ethernet connectivity through FEC-2 (5-port Ethernet switch).

5.2.7 IEEE 1588 Connector (J16)—Optional

An optional header (J4) is provided for IEEE 1588 signals connection. It is a dual-row, 16-pin (2 x 8) header connector. The pinout of this connector is shown in the following figure.

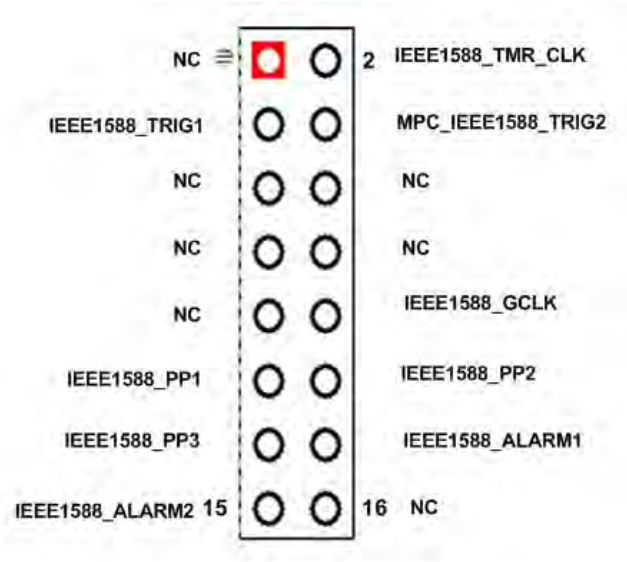

Figure 31. IEEE1588 Header

5.2.8 GPIO/SPI Header (J17)

Header J17 consists of SPI signals for future expansion and some I^2C I/O expander–based GPIO for software verification purpose. The pinout of this connector is shown in the following figure.

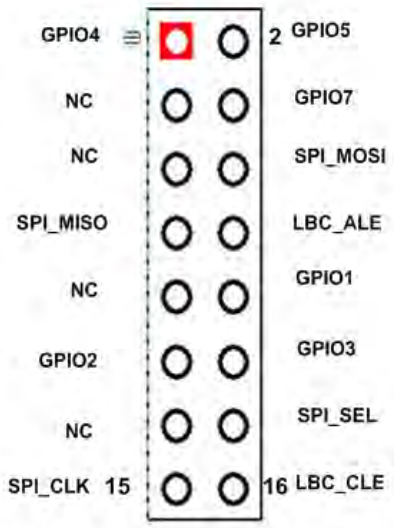

Figure 32. GPIO/SPI Header for expansion

5.2.9 Local Bus Connector (J15)

A 60-pin local bus connector (J15) is provided on the carrier card to terminate all local bus signals for future system expansion purpose.

6 MPC8306KIT Board Configuration

This section describes the operational frequency and configuration options of the MPC8306KIT.

6.1 Reset Configuration Word

The reset configuration words control the clock ratios and other basic device functions such as boot location and endian mode. The reset configuration words are loaded from NOR Flash, NAND Flash, or the I^2C interfaces or from hard-coded values during the power-on or hard reset flows. The reset configuration word is divided intoreset configuration word low register (RCWLR) and reset configuration word high register (RCWHR). The default RCW low bit setting is 0x4404_0008. The default RCW high bit setting is 0x0006_0000. The RCW is located at the lowest 64 bytes of the boot Flash memory, which is 0xFE00_0000 if the default memory map is used.

Table 15. Default RCW in Flash Memory

Address				
FE000000:	44444444	44444444	04040404	04040404
FE000010:	00000000	00000000	08080808	08080808
FE000020:	00000000	00000000	60606060	60606060
FE000030:	00000000	00000000	00000000	000000000

The RCW configurations are shown in the following two figures.

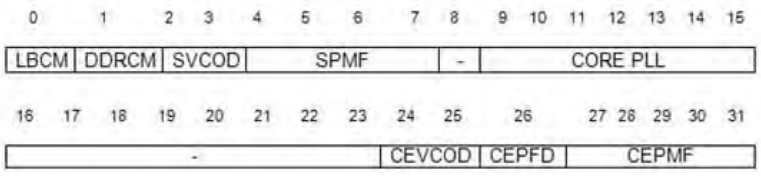

Figure 33. Reset Configuration Word Low Register (RCWLR)

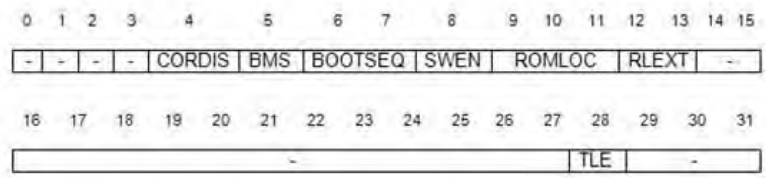

Figure 34. Reset Configuration Word High Register (RCWHR)

Table 16. RCWLR Bit Descriptions

Bits	Name	Meaning	Description	
0	LBCM	Local bus clock mode	Local bus controller clock: CSB_CLK	
			0(Default)	Ratio 1:1
			1	Ratio 2:1
1	DDRCM	DDR SDRAM clock mode	DDR control clock: CSB_CLK	
			0	Ratio 1:1
			1(Default)	Ratio 2:1
2–3	SVCOD	System PLL VCO division	VCO division factor	
			00(Default)	2
			01	4
			10	8
			11	Reserved
4–7	SPMF[0-3]	System PLL multiplication factor	0000	Reserved
			0001	Reserved
			0010	2:1
			0011	3:1
			0100	4:1
			0101	5:1
			0110	6:1
			0110–0000	Reserved
8	—	Reserved	Must be cleared	

Table 16. RCWLR Bit Descriptions (continued)

Bits	Name	Meaning	Description		
9–15	Core PLL[0-6]		Value	coreclk: csb_clk	VCO divider\
			nn 0000 n	PLL Bypasses	PLL Bypasses
			00 0001 0	1:1	2
			01 00010	1:1	4
			10 00010	1:1	8
			11 00010	1:1	8
			00 0001 1	1.5:1	2
			01 0001 1	1.5:1	4
			10 0001 1	1.5:1	8
			11 0001 1	1.5:1	8
			00 0010 0	2:1	2
			01 0010 0	2:1	4
			10 0010 0	2:1	8
			11 0010 0	2:1	8
			00 0010 1	2.5:1	2
			01 0010 1	2.5:1	4
			10 0010 1	2.5:1	8
			11 0010 1	2.5:1	8
			00 0011 0 (Default)	3:1	2
			01 0011 0	3:1	4
			10 0011 0	3:1	8
			11 0011 0	3:1	8
16–23		Reserved	Must be cleared		

Table 16. RCWLR Bit Descriptions (continued)

Bits	Name	Meaning	Description	
24–25	CEVCOD	QUICC Engine PLL VCO division	Establish internal ratio between QUICC Engine PCC VCO point and QUICC Engine PLL output.	
			00	4
			01	Reserved
			10	2
			11	Reserved
26	CEPDF	QUICC Engine PLL division factor	Determine the ce_clk based on RCWHR[CEPMF]	
			0	ce_clk = primary clock input *CEPMF
			1	ce_clk =(primary clock input *CEPMF)/2
27–31	CEPMF	QUICC Engine PLL multiplication factor	Determine the ratio between ce_clk and primary clock input	
			00000	Reserved, should be cleared
			00001	Reserved, should be cleared
			00010	2
			00011	3
			00100	4
			00101	5
			00110	6
			00111	7
			01000	8
			010001-11111	Reserved, should be cleared

Table 17. RCWHR Bit Descriptions

Bits	Name	Meaning	Description	
0–3	—	Reserved	Must be cleared	
4	CORDIS	Core disable mode	0 (Default)	e300 enabled
			1	e300 disabled
5	BMS	Boot memory space	0	0x0000_0000 - 0x007F_FFFF
			1	0xFF80_0000 - 0xFFFF_FFFF

Table 17. RCWHR Bit Descriptions (continued)

Bits	Name	Meaning	Description	
6–7	BOOTSEQ	Boot sequencer configuration	00(Default)	Boot sequencer is disabled
			01	Normal I^2c addressing mode is used. Boot sequencer load configuration from ROM on I^2C interface
			10	Extended I^2c addressing mode is used. Boot sequencer load configuration from ROM on I^2C interface
			11	Reserved
8	SWEN	Switch watchdog enable	0	Disable
			1	Enable
9–11	ROMLOC	Boot ROM interface location	000	DDR2 SDRM(if RCWH[RLEXT=00]) or reserved (if RCWH[RLEXT=01])
			001	Reserved (if RCWH[RLEXT=00]) or local bus NAND Flash - 8 bit small page ROM (if RCWH[RLEXT=01])
			010, 011, 110	Reserved
			101	Local bus GPCM - 8 bit ROM (if RCWH[RLEXT=00]) or Local bus NAND Flash - 8 bit large page ROM (if RCWH[RLEXT=01])
			110 (Default)	Local bus GPCM,16 bits
			111	Reserved
12–13	RLEXT	Boot ROM extension location	00 (Default)	Legacy mode
			01	NAND flash mode
			10, 11	Reserved
14–15	—	Reserved	Must be cleared	
16–27	—	Reserved	Must be cleared	
28	TLE	True little endian	0 (Default)	Big-endian mode
			1	Little-endian mode
29–31	—	Reserved	Must be cleared	

6.2 Power Supply

The MPC8306KIT requires a 12 V power supply from the 3-pin power jack on carrier card. SOM board gets required power at 5 V rail from carrier card. Core voltage, DDR2 voltage, and PHY-specific voltages are generated by either SOM board switching or linear regulated depending on the voltage drop and current consumption requirement.

The MPC8306 does not require the core supply voltage and I/O supply voltages to be applied in any particular order. However, during the power ramp up, before the power supplies are stable, there may be

an interval when the IO pins are actively driven. Afterthe power is stable, as long as PORESET is asserted, most I/O pins are three-stated. To minimize the time that I/O pins are actively driven, apply core voltage before I/O voltage and assert PORESET before the power supplies fully ramp up.

NOTE

In case of MPC8306SOM on stand-alone mode, 5 V needs to be suppplied through 3-pin power jack on SOM card.

6.2.1 MPC8306KIT Power Supply

The following table shows the power supply requirement for MPC8306KIT.

Table 18. Power Supply Requirement Summary of MPC8306KIT

Voltage	Usage	Solution
12V	Input supply to TPS40193DRC	Direct from 2.1 mm power jack
5V	MPC 8306 SOM and CAN interface	TPS40193DRC (3A)
3.3V	T1/E1 framer, Ethernet switch and other devices.	TPS40193DRC (3A)
1.5V	Ethernet switch and Mini PCIe	NCP1117STAT3G LDO(0.5A) and TPS62290DRVT(1A)
1.8V	Ethernet switch magnetics	NCP1117STAT3G LDO(0.5A)
MPC8306SOM Power Supply detail		
5V	MPC8306SOM power supply detail	From carrier card through board-to-board connector
3.3V	MPC8306 and other I/O Voltage	TPS65023RSBT (1.2A)
1.8V	MPC8306 and DDR2 I/O voltage	TPS65023RSBT (1A)
1V	MPC8306 core voltage	TPS65023RSBT (1.5A)

NOTE

In case of MPC8306SOM stand-alone mode of operation, connect external 5 V supply through 3-pin (2.5 mm) power jack on SOM board.

6.3 Chip-Select Assignments and Memory Map

Table 19. Example Memory Map, Local Access Window, and Chip-Select Assignments

Address Range	Target Interface	Chip select Line	Mapping size	Bit width
0x00000000 to 0x08000000	DDR2	MCS0#	128 MB	16 bit
0xe0000000 to 0xe00fffff	Internal bus	Nil	1 MB	—
0xFFF00000 to 0xFFF3FFFF	NAND controller	LCS1#	NAND Flash window 256 Kbyte	8
0xfe000000 to 0xfe7fffff	NOR controller	LCS0#	NOR Flash window 8 MB	16

7 Getting Started

This section describes how to boot the MPC8306 SOM stand-alone and MPC8306 SOM with carrier (MPC8306KIT). Before powering up the board, verify that all the on-board jumpers are set to the defaults according to the settings listed in Section 7.1, "Board Jumper Settings," and make all external connections as described in Section 7.2, "External Cable Connection."

7.1 Board Jumper Settings

This section provides jumper setting of the 8306SOM stand-alone and as a KIT with carrier card.

7.1.1 8306SOM Jumper Settings

Figure 35 and Figure 36 show top/bottom view of MPC8306SOM with each connector Pin-1 marked for reference. There is one jumper setting at the top side and two at bottom side required for functional operation. DIP switches are NOT used on the board.

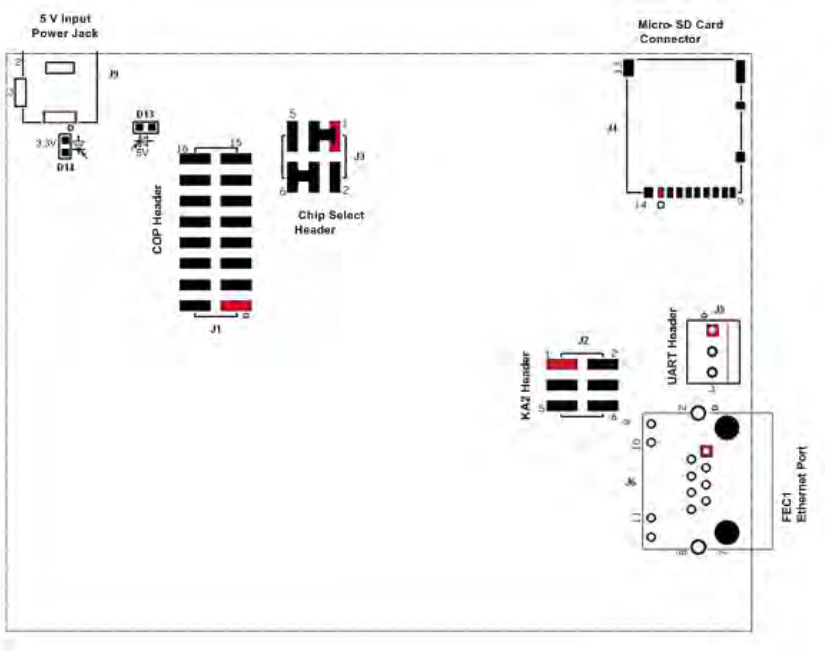

Figure 35. 8306SOM Top View

Table 20. Default Jumper Settings on Top

Reference	Description
J3	Short link jumper between Pin 3-1 and 4-6

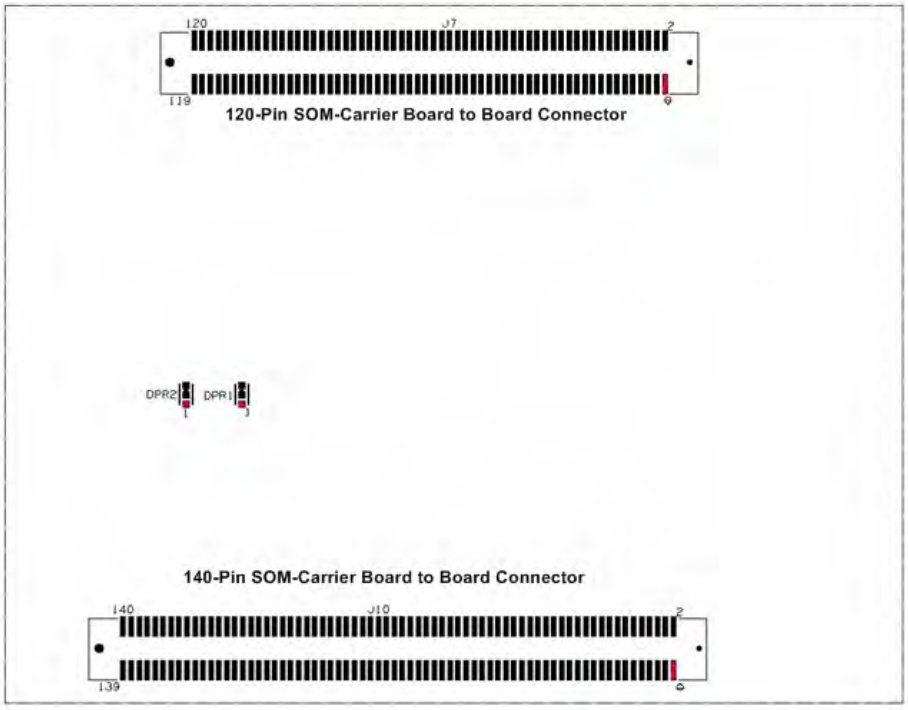

Figure 36. 8306SOM Bottom View

Table 21. Default Jumper Settings on Bottom

Reference	Description
DPR1	Short pin 2-3
DPR2	Short pin 2-3

NOTE

DPR—This is a 3-pad component footprint that provides options to mount/short link jumper on two adjacentpads. By connecting two pads, one of the two options can be selected as shown in the following figure.

Figure 37. DPR1 and DPR2 Settings

7.1.2 MPC8306KIT Top View

The following figure shows top view of MPC8306KIT (SOM + Carrier) with Pin-1 marked for each reference. The jumper setting for MPC8306KIT is same as SOM stand-alone.

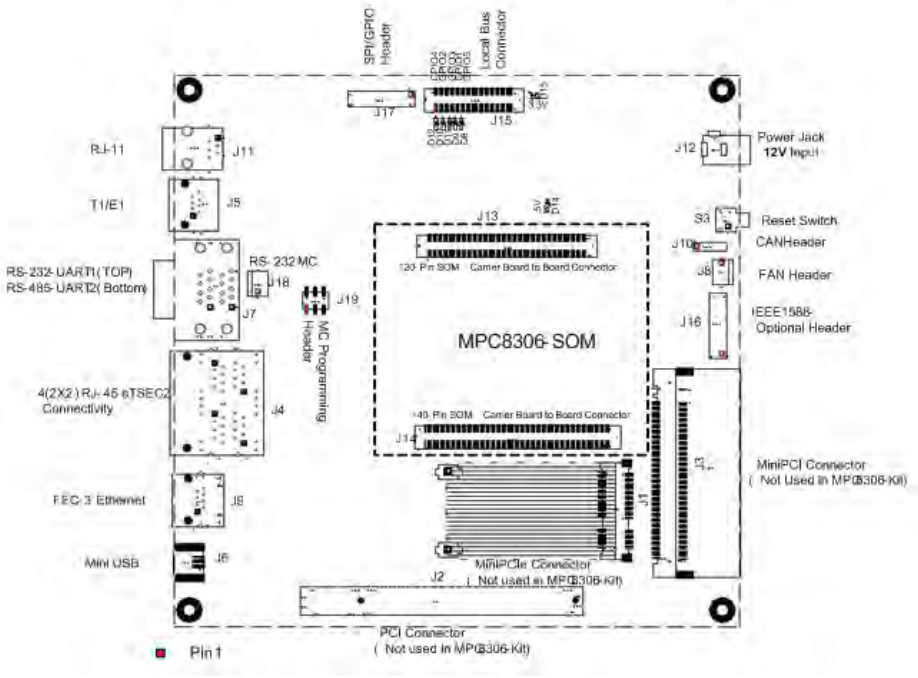

Figure 38. MPC8306KIT Top View

7.2 External Cable Connection

Do not turn on power until all cables are connected and the serial port is configured as described in Section 7.3, “Serial Port Configuration (On PC).” Connect the serial port of the MPC8306_RDB system and the personal computer using an RS-232 cable as shown in Figure 39.

7.2.1 MPC8306KIT (SOM + Carrier) External Cable Connection

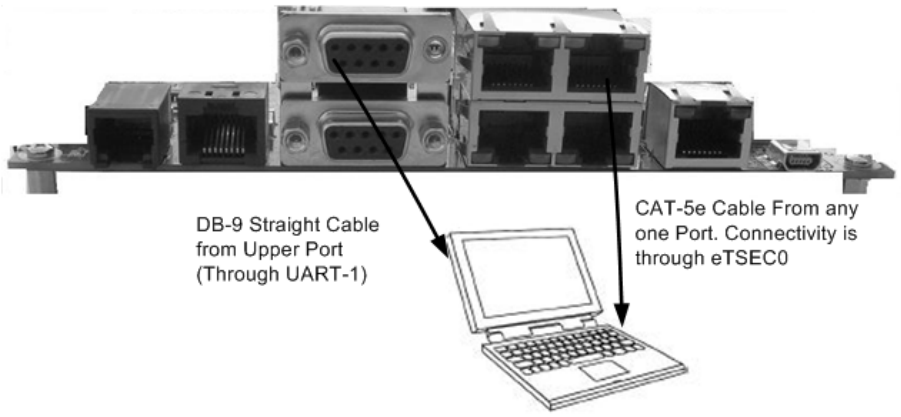

Figure 39. External Cable Connection MPC8306KIT

7.2.2 MPC8306 SOM Stand-alone External Cable Connection

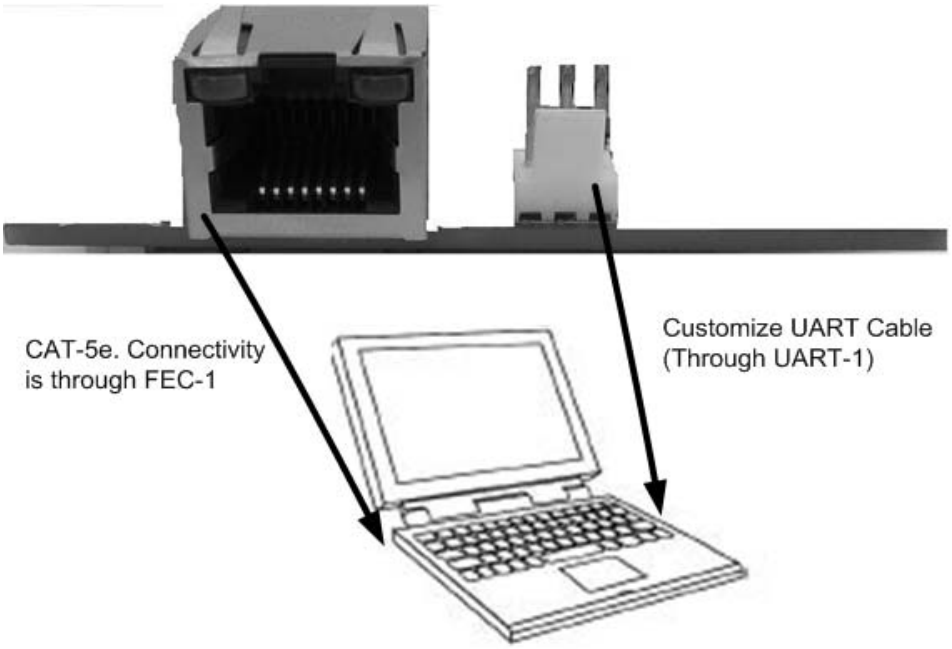

Figure 40. External Cable Connection MPC8306KIT

7.3 Serial Port Configuration (On PC)

Before powering up the MPC8306 board, configure the serial port of the attached computer with the following values:

- Data Rate: 115200 bps
- Number of Data Bits: 8
- Parity: None

- Number of Stop Bits: 1
- Flow Control: None

7.4 Power Up

The three-pin power jack (J12) on carrier card should be used to supply necessary DC power when MPC8306KIT is powered up.

NOTE

The three-pin power jack (J9) should be used to supply power for MPC8306SOM stand-alone operation only. Do not connect power to J9 while using SOM with carrier card.

Example 1.

```
U-Boot 2010.06 (Dec 06 2010 - 10:11:06) MPC83XX
Reset Status:
CPU:   e300c3, MPC8306E, Rev: 1.0 at 266.667 MHz, CSB: 133.333 MHz
QE: 200 MHz
Board: Freescale MPC8306SOM Rev B
I2C:   ready
DRAM:  128 MB
FLASH: 8 MiB
Firmware 'Microcode version 0.0.0 for MPC8306 r1.0' for 8306 V1.0
QE: uploading microcode 'Microcode for MPC8306 r1.0'
NAND:  256 MiB
In:    serial
Out:   serial
Err:   serial
MMC:  FSL_ESDHC: 0
Net:   FSL UEC0, FSL UEC1, FSL UEC2
Hit any key to stop autoboot:  0
```

8 MPC8306KIT Software

A board support package (BSP) is pre-installed on the MPC8306_KIT. This BSP consists of a boot loader (u-boot), a generic PowerPC Linux-based system, and an associated file system. U-boot, the Linux kernel, and the file system reside in the on-board Flash memory. At power up, the Linux system runs on the MPC8306_KIT.

The MPC8306KIT BSP generation takes advantage of a tool called the Linux target image builder (LTIB). LTIB is a suite of tools that leverages existing open source configuration scripts and source code packages and bundles them into a single BSP-generation package. The source code packages include boot loaders and Linux kernel sources as well as many user-space source code packages to build a complete BSP. LTIB also provides compiler packages required to build the BSP. Freescale developers use LTIB to create BSPs

for a multitude of Freescale development targets. LTIB leverages as many BSP elements as possible for all Freescale-supported targets, and it offers the flexibility to customize components that require platform-specific modifications.

The MPC8306KIT BSP release package contains a file named ltib-mpc830xsom-<yyyymmdd>.iso. This file is an ISO image that can be burned to a CD-ROM or mounted directly from your hard disk. Note that <yyyymmdd> is the release creation date. The LTIB installation script that installs all necessary packages on a host Linux PC and allows you to modify the BSP and packages within the BSP is in the ISO image.

This ISO image contains a file called README that describes how to generate and install the BSP on the MPC8306KIT hardware platform. README contains the latest information for each BSP release. To rebuild the BSP package or to add application software, carefully follow the instructions in README. This file contains details on how to build, run, and install the BSPIt guides the user toachieve a successful re-installation of the BSP on the MPC8306_KIT. This ISO image contains the following documents:

- MPC8306-KIT User_Guide.pdf—This user's guide document is in PDF format
- FREESCALE_MPC8306_SOM.pdf and FREESCALE_MPC830X_CARRIER.pdf the platform schematic is in PDF format

For more information on the MPC8306KIT, visit the Freescale web site. To run demonstrations or to acquire details of Freescale third-party applications for this MPC8306KIT, contact your local Freescale sales office.

9 Revision History

The following table provides the revision history for this document.

Table 22. Document Revision History

Revision Number	Date	Substantive Change(s)
0	07/11	Initial Public Release

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