i.MX28 EVK Hardware

User's Guide

Document Number: 924-76415
Rev. 0
7/2011

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Document Number: 924-76415
Rev. 0
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Chapter 1
Introduction

This document provides detailed information on the i.MX28 EVK hardware design. It should be used as a reference for hardware and software design and diagnostics.

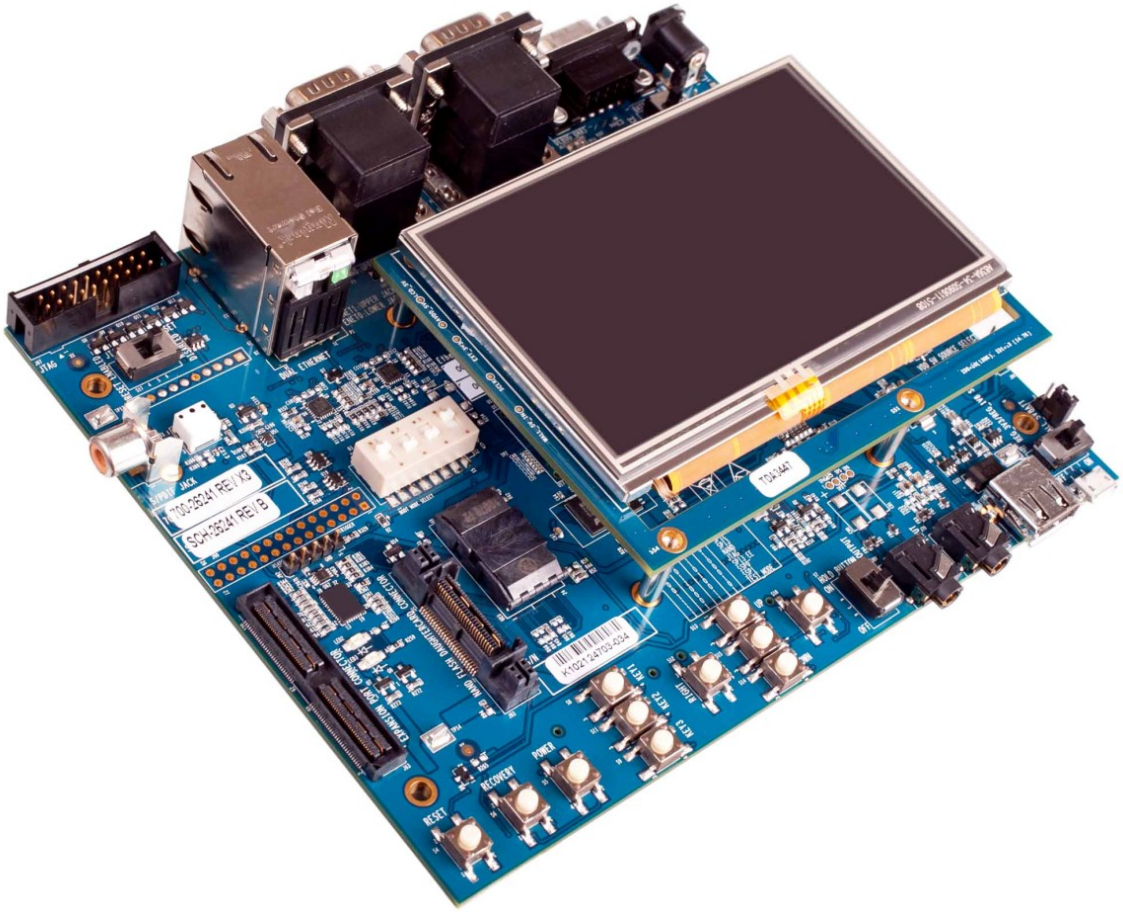

Figure 1-1 i.MX28 EVK System

1.1 Reference Documents

1. i.MX28 Reference Manual (Rev1.0) , Freescale Semiconductor, 2009.06
2. i.MX28 Datasheet, Freescale Semiconductor, 2009
3. LAN8720 Datasheet(Rev 1.0), SMSC, 2009.04
4. SGTL5000 Datasheet(Rev.2), Freescale, 2008.11
5. EDE1116AEBG, 1Gb DDR2 SDRAM Specification(Rev2.0), Elpida, 2008.01
6. TLE6251DS Datasheet(Rev3.1), Infineon, 2007.08
7. SD Memory Card Specifications, SD Group, 2001.04

1.2 Terms and Abbreviations

1. EVK: Evaluation Kit
2. EVB: Evaluation Board
3. SD: Secure Digital Card
4. CAN: Controller Area Network
5. MMC: Multi-Media Card
6. ENET: Ethernet
7. SAIF: Serial Audio Interface
8. LCD: Liquid Crystal Display
9. USB: Universal Serial Bus
10. DNP: Do Not Populate

Chapter 2
i.MX28 EVK Board

2.1 General

The i.MX28 EVK board is a single board solution for customers.

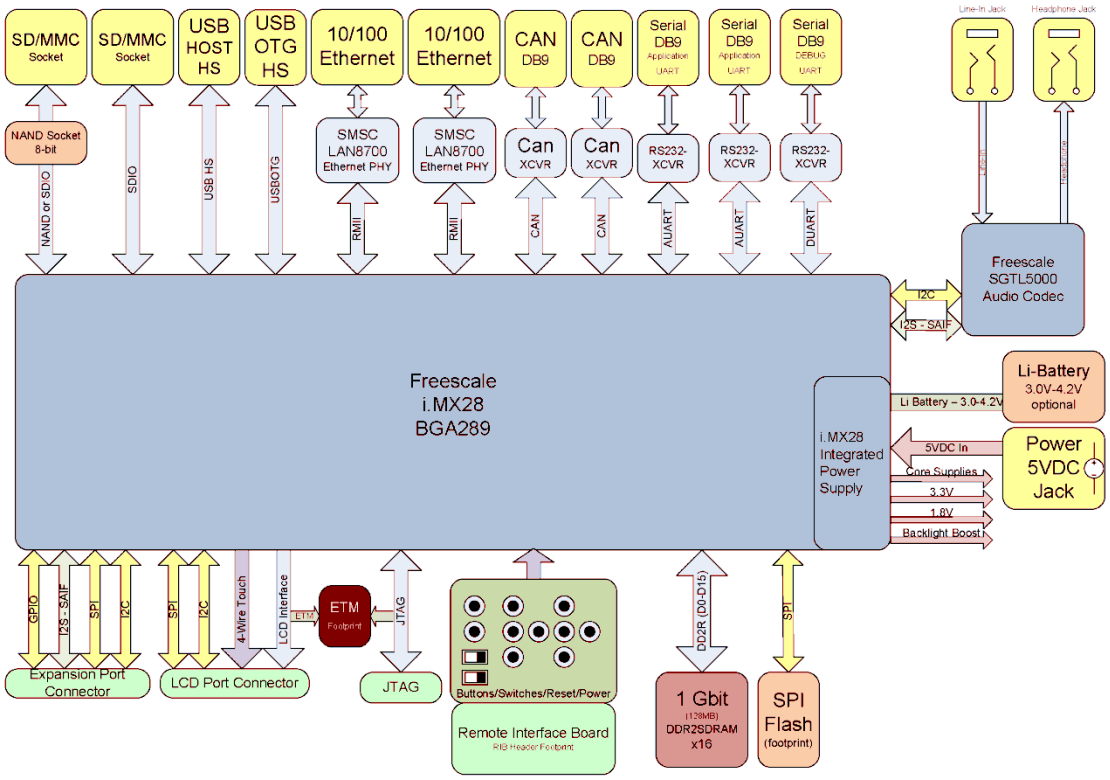

Figure 2-1 i.MX28 EVK System Block Diagram

2.2 i.MX28 Processor

The i.MX28 is a low-power, high performance multimedia application processor ideally suited for the following:

- Human machine interface (HMI) panels: industrial, and home
- Industrial drive, PLC, I/O control display, factory robotics display, and graphical remote
- Handheld scanners and printers
- Electronic point-of-sale (POS) terminals
- Patient-monitoring devices

- Smart energy meters and home energy management systems
- Portable medical, media phones, and VoIP
- Automotive products such as road-tolling monitors, connectivity gateways, car audio accessories and touch screen controlled car radios

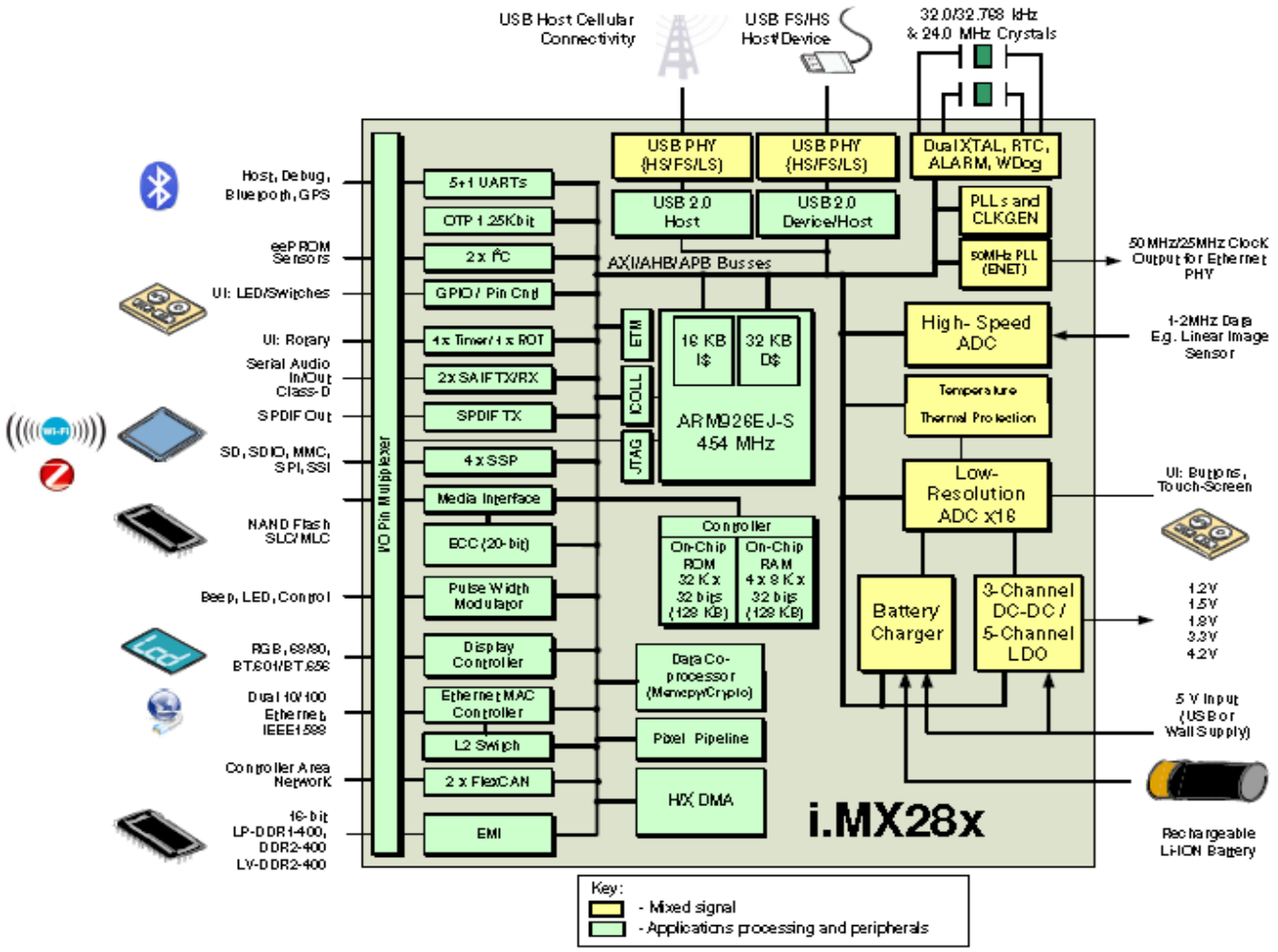

Figure 2-2 i.MX28 Block Diagram

2.3 Boot Mode

Table 2-1 shows details of the boot mode.

Table 2-1 Boot Mode Select

B3	B2	B1	B0	Boot Mode
0	0	0	0	USB0
0	0	0	1	I2C0
0	0	1	0	SPI2
0	0	1	1	SPI3(Flash)
0	1	0	0	GPMI(NAND)
0	1	0	1	Reserve
0	1	1	0	JTAG
0	1	1	1	Reserve
1	0	0	0	SPI3(EEPROM)
1	0	0	1	SSP0(SD0)
1	0	1	0	SSP1(SD1)
1	0	1	1	Reserve
1	1	0	0	Reserve
1	1	0	1	Reserve
1	1	1	0	Reserve
1	1	1	1	Test mode

Notes:

1. EVK board uses switch S2 to select the boot mode. B0, B1, B2, and B3 are labeled next to the pins of switch S2.

2. B3, B2, B1 and B0 can be set to either a 1 or 0 to set the boot mode.
   UP position = 1
   DOWN position = 0

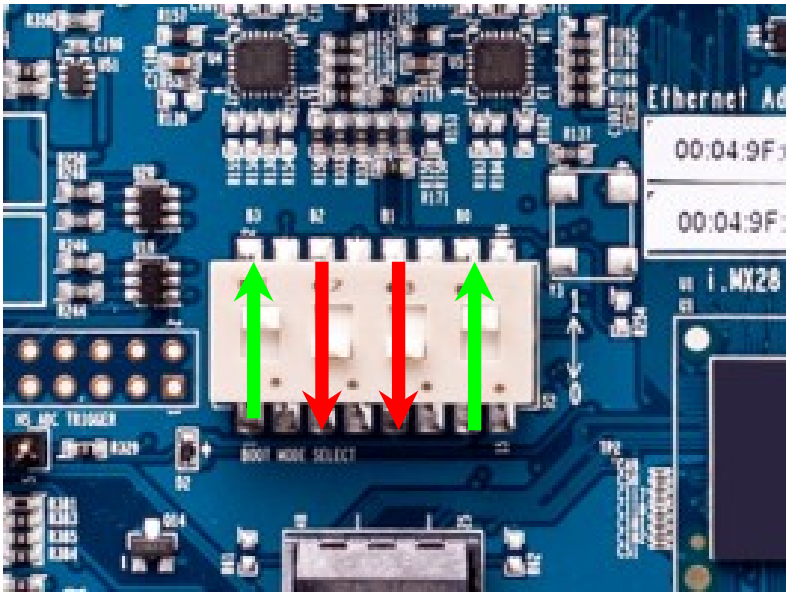

Figure 2-3 Boot Mode Positions

3. SSP0 (SD Card Socket 0) is the default boot mode.
   In this mode, B3, B2, B1, and B0 are set in the positions shown in the diagram below:

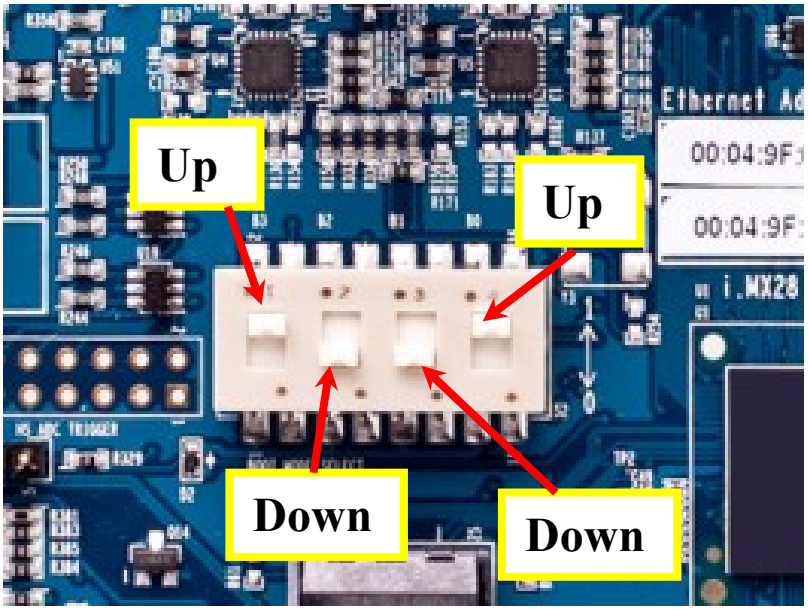

Figure 2-4 Default Boot Mode

2.4 DDR2 SDRAM

There is a single 64MB×16 (128 Mbit) DDR2 SDRAM on the EVK board. The system block diagram is shown in Figure 2-5.

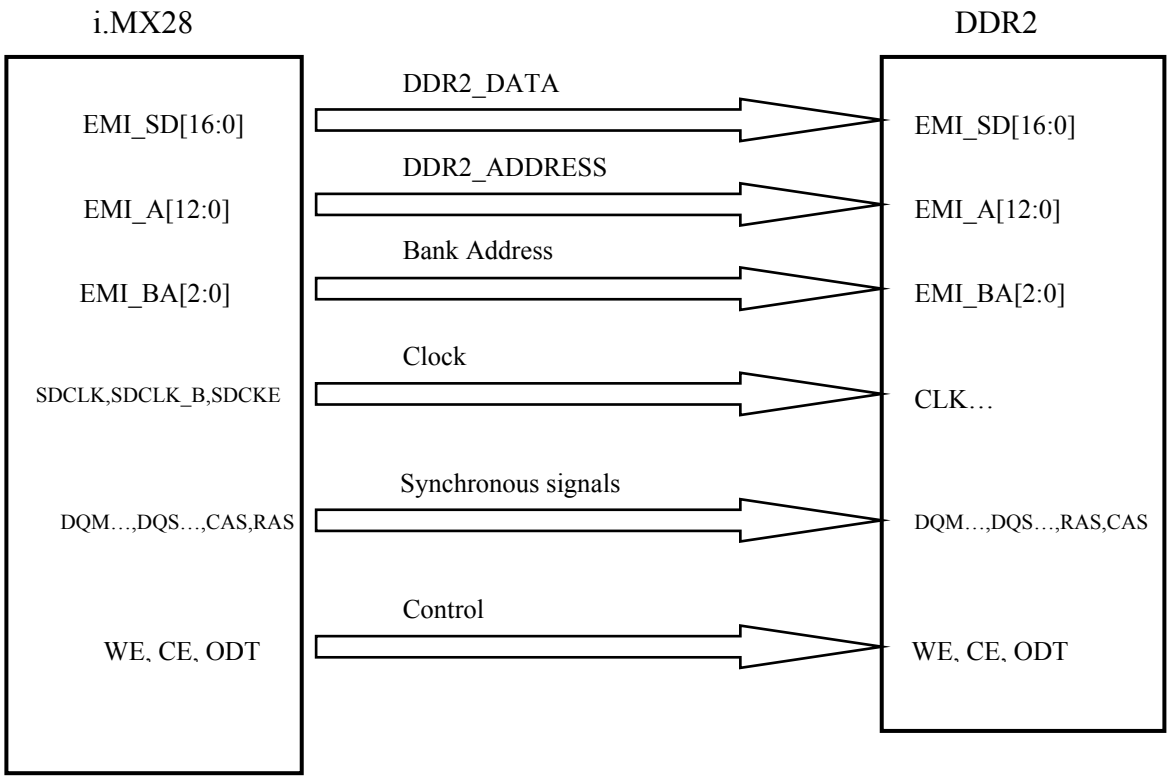

Figure 2-5 DDR2 Memory Block Diagram

2.5 NAND Flash

A NAND Flash Socket is placed on i.MX28 EVK board. It can be used as boot device and a data storage media. There is also a NAND Flash connector on board to support various flash memory daughter-cards. Refer Figure 2-6.

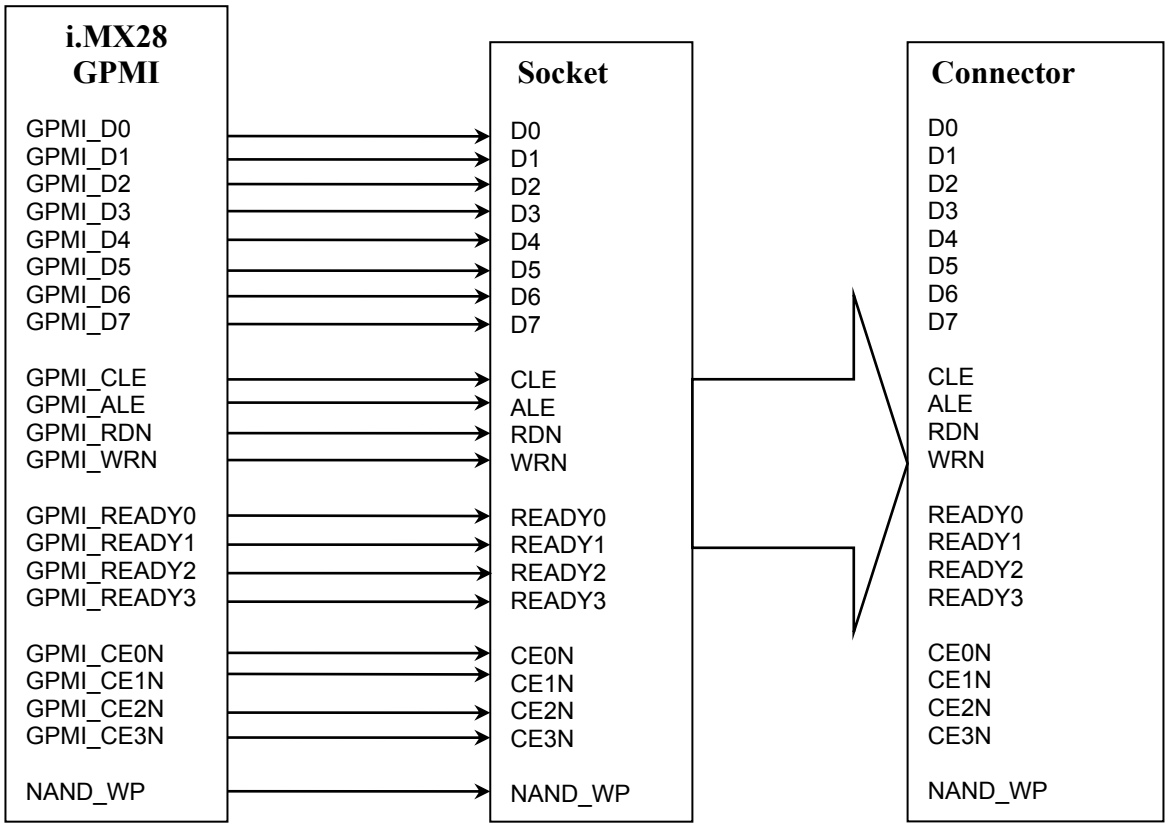

Figure 2-6 NAND Flash Memory System Block Diagram

Notes:

1. The socket and connector share the same signals. A 48 pin TSOP NAND flash can be placed into the socket and/or a flash daughter-card can be placed into the connector.

2. i.MX28 EVK board supports up to 4 NAND flash ICs (CE0, CE1, CE2, and CE3), However, the 0 ohm options for CE2 and CE3 are disconnected by default (they are used for CAN).

3. NAND_WP uses the i.MX28 **GPMI_RESETN** pin.

2.6 EEPROM and SPI Flash

Figure 2-7 shows the EEPROM and SPI Flash block diagram.

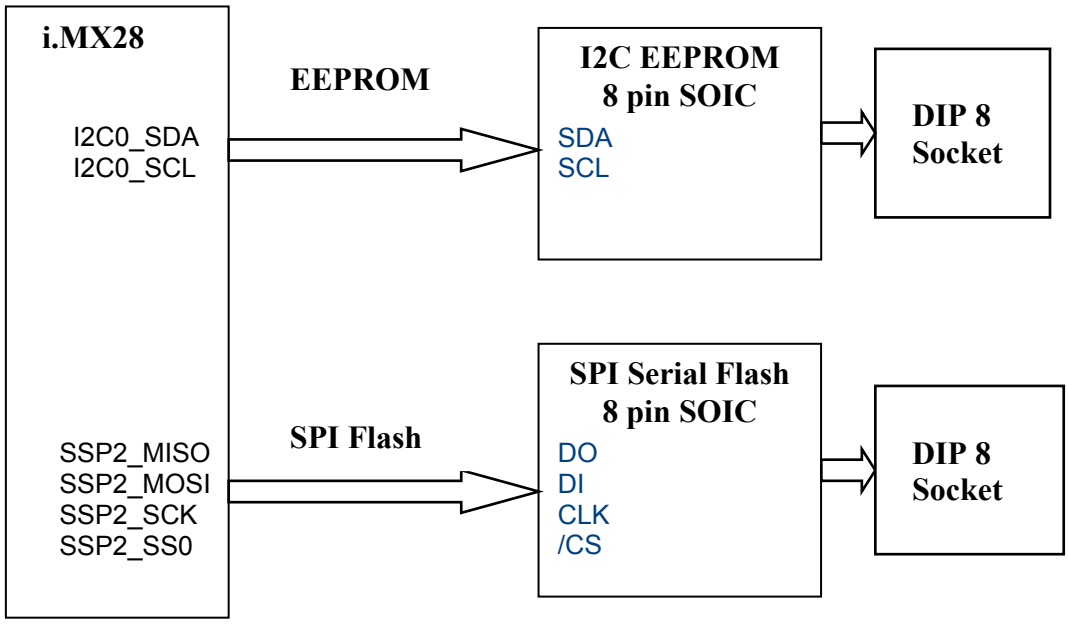

Figure 2-7 Serial Memory Block Diagram

Notes:

1. Default I2C EEPROM IC footprint and socket are DNP.
2. Default SPI Flash IC footprint and socket is DNP.

2.7 Stereo Audio Codec

A stereo audio codec is integrated on i.MX28 EVK board, the part number is SGTL5000.

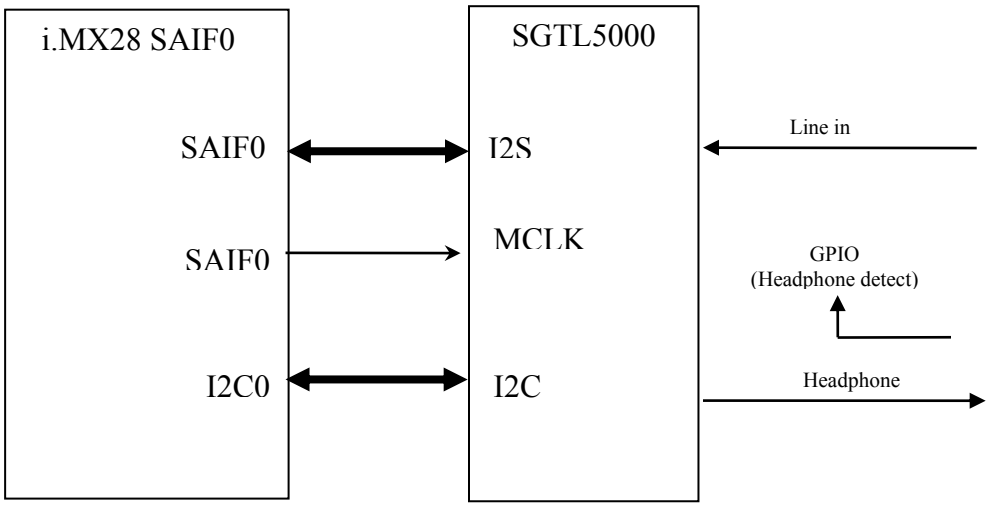

Figure 2-8 Audio Codec Block Diagram

Notes:

1. Line in and headphone out are supported on the EVK board. The additional features of the SGTL5000 are not supported.
2. SGTL5000 uses the clock from the i.MX28 SAIF0 MCLK.
3. Capless headphone mode is used for the headphone output so the appropriate SGTL5000 register bit(s) should be set to enable capless headphone mode.

2.8 LCD Daughter-Card Connector

There is a 4.3” WVGA (800 x 480) RGB TFT with Touch-Panel. Figure 2-9 shows the LCD circuit block diagram.

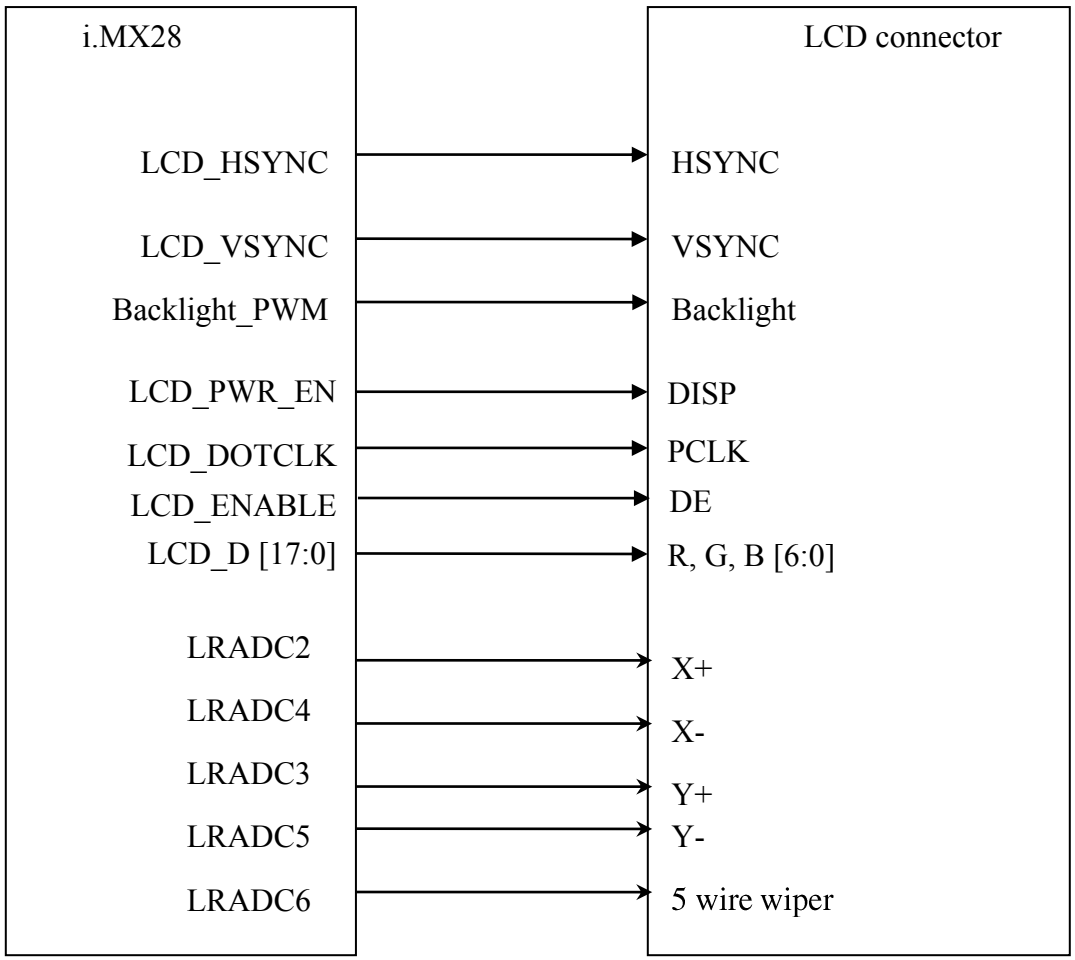

Figure 2-9 LCD Circuit Block Diagram

Notes:

1. LCD_PWR_EN is connected to i.MX28 LCD_RESET(GPIO3_30)
2. Backlight_PWM is connected to PWM2.
3. The i.MX28 has an integrated resistive touch controller, which uses the LRADC signals.

2.9 USB OTG and HOST

Figure 2-10 shows the USB circuit block diagram.

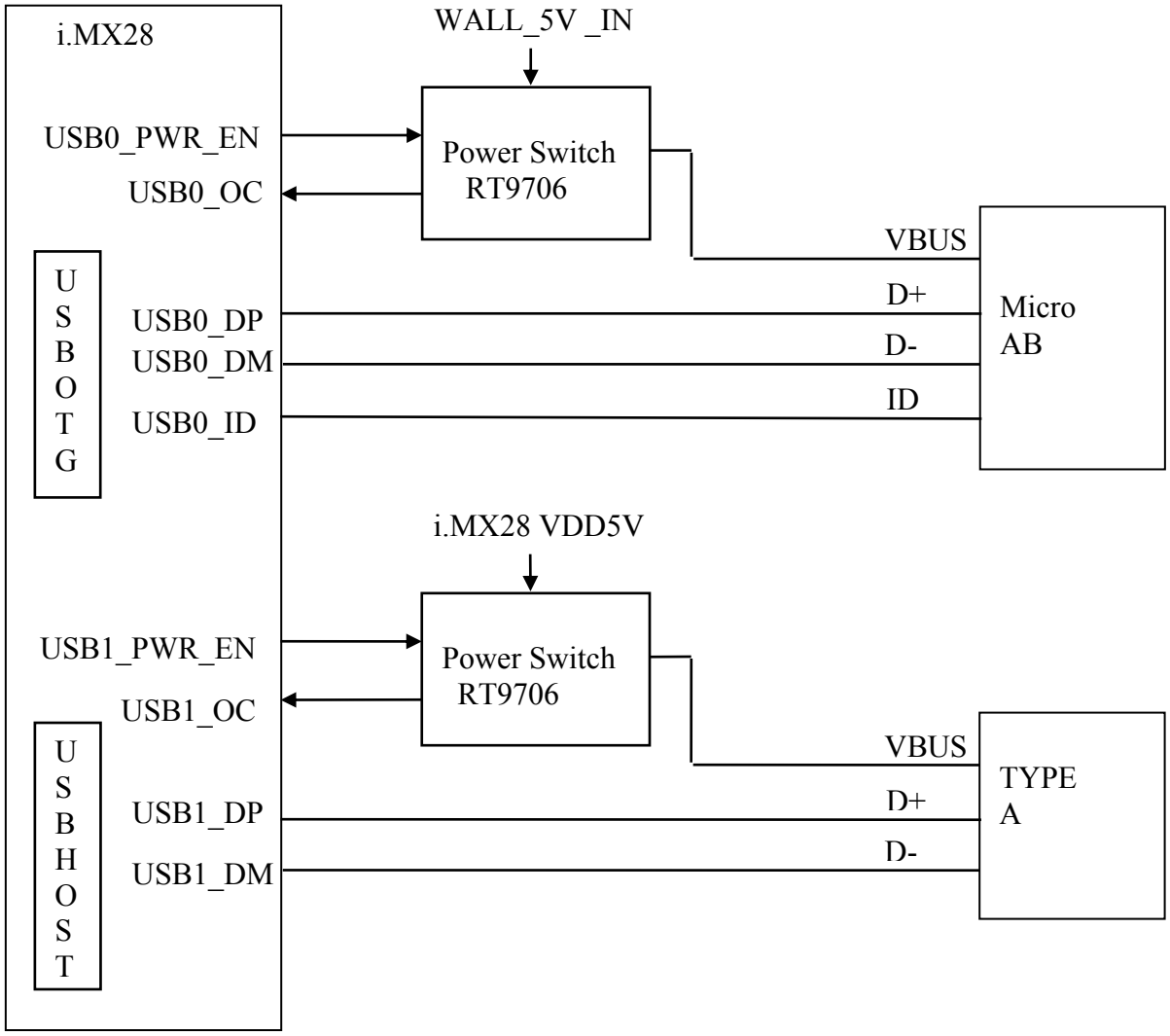

Figure 2-10 USB Circuit Block Diagram

2.10 MMC/SD Interface

There are two SD card slots on the i.MX28 EVK board. Refer Figure 2-11.

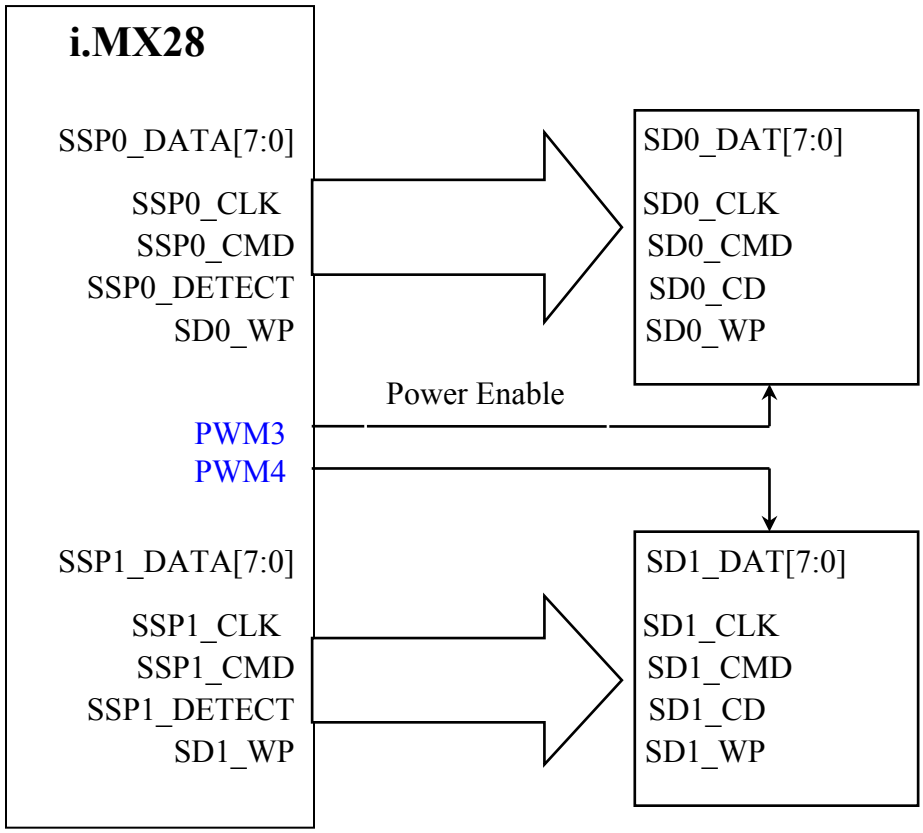

Figure 2-11 SD/MMC Block Diagram

Notes:

1. SD0 and SD1 can both be used as a boot device.
2. The default SD0 power supply is VDDIO33 and the default SD1 power supply is REG_3V3. SD0 and SD1 both have a power supply option for using either VDDIO33 or REG_3V3. REG_3V3 can support large current applications like a WIFI SD card.
3. PWM3 is used as the default power enable for SD0. PWM4 can be used instead by removing resistor R96 and populating R102.
4. PWM4 is used as the default power enable for SD1. PWM3 can be used instead by removing resistor R99 and populating R114.

2.11 10/100 Ethernet

Figure 2-12 shows the i.MX28 EVK Ethernet system block diagram.

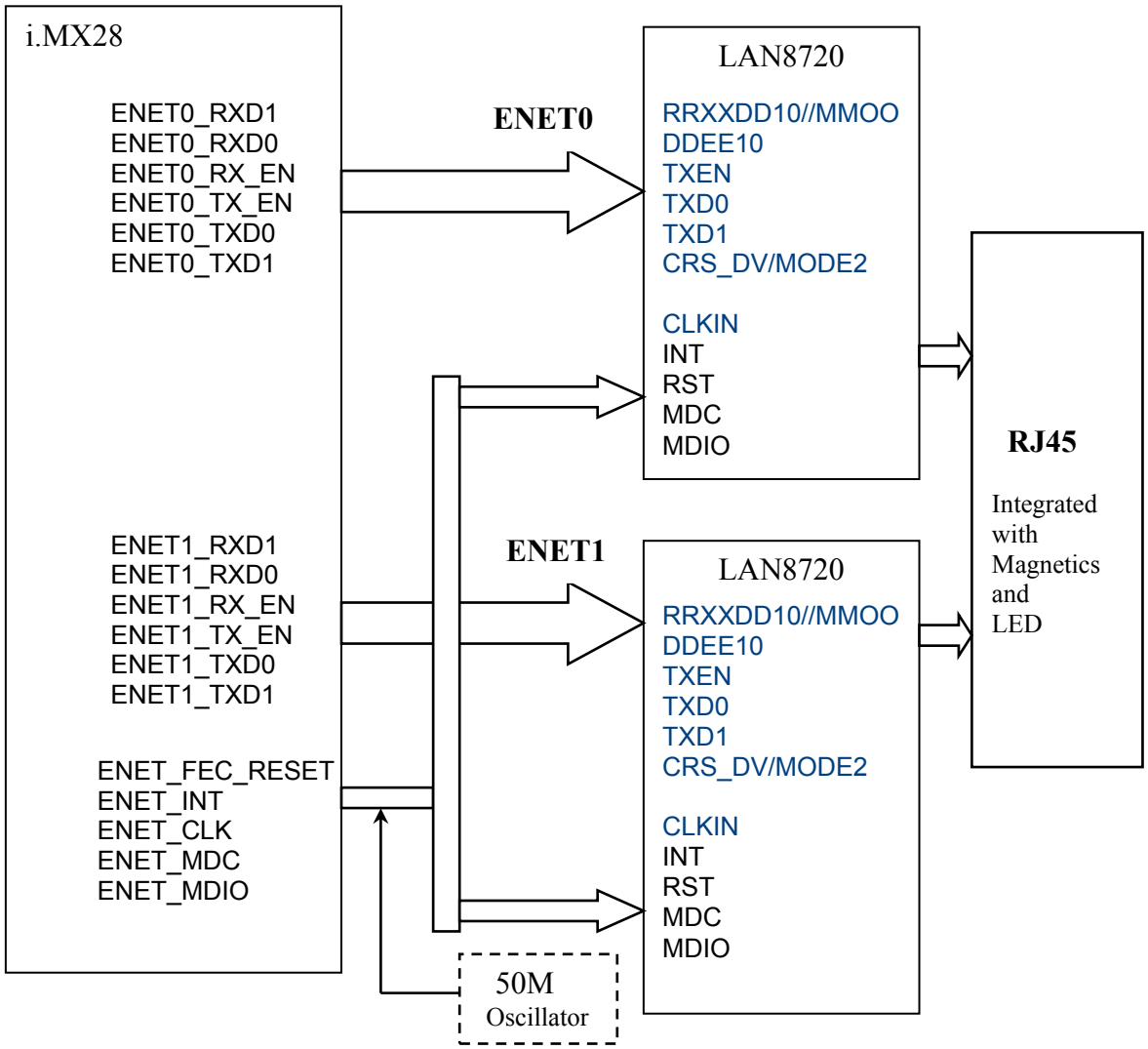

Figure 2-12 Ethernet Block Diagram

Notes:

1. i.MX28 provides the 50 MHz clock to both Ethernet PHYs. The default external 50 MHz oscillator is DNP.
2. The MDC, MDIO, ENET_FEC_RESET, ENET_INT, and ENET_CLK signals are shared by both LAN8720 PHYs.
3. A dual stack RJ45 connector is used for the ENET interface.
   The upper jack is ENET1.
   The lower jack is ENET0.

2.12 CAN

Figure 2-13 shows the i.MX28 CAN circuit block diagram.

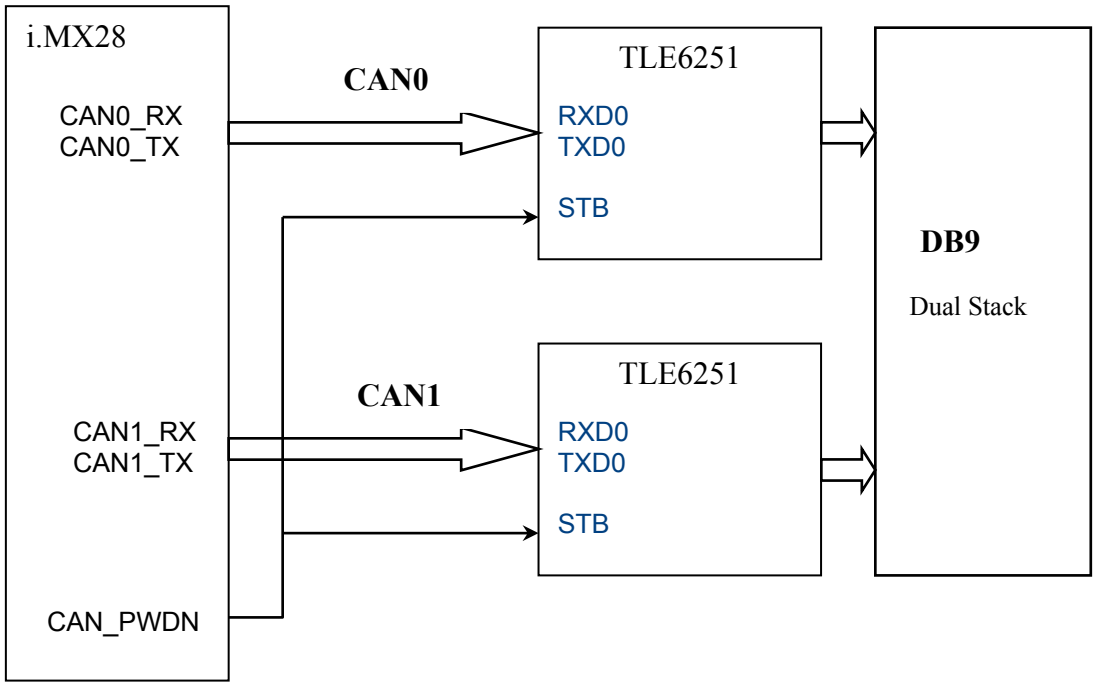

Figure 2-13 CAN Circuit Block Diagram

Notes:

1. CAN_PWDN is shared by both TLE6251 CAN transceivers, which use the MX28 SSP1_CMD pin as a GPIO.
   0 = standby mode
   1 = power on mode

2. A dual stack male DB9 connector is used for the CAN interface.
   The upper jack is CAN0.
   The lower jack is CAN1.

2.13 UART

Figure 2-14 shows the i.MX28 UART system block diagram.

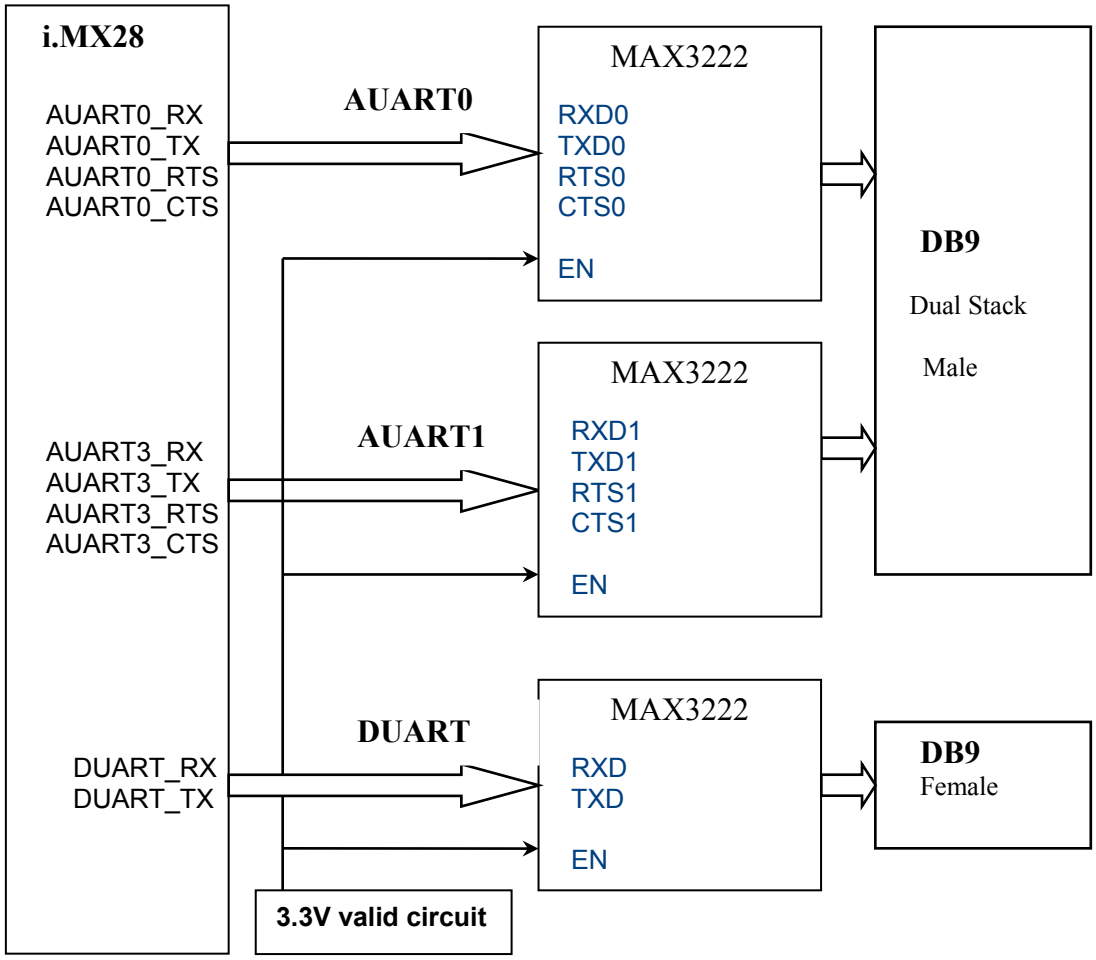

Figure 2-14 UART System Block Diagram

Notes:

1. The AUART interface uses a dual stack male DB9.
   The upper jack is UART0.
   The lower jack is UART1.

2. The DUART is used for debugging and is typically connected to a computer communications terminal.

2.14 Board HW Identification

Figure 2-15 shows the i.MX28 Board HW identification block diagram.

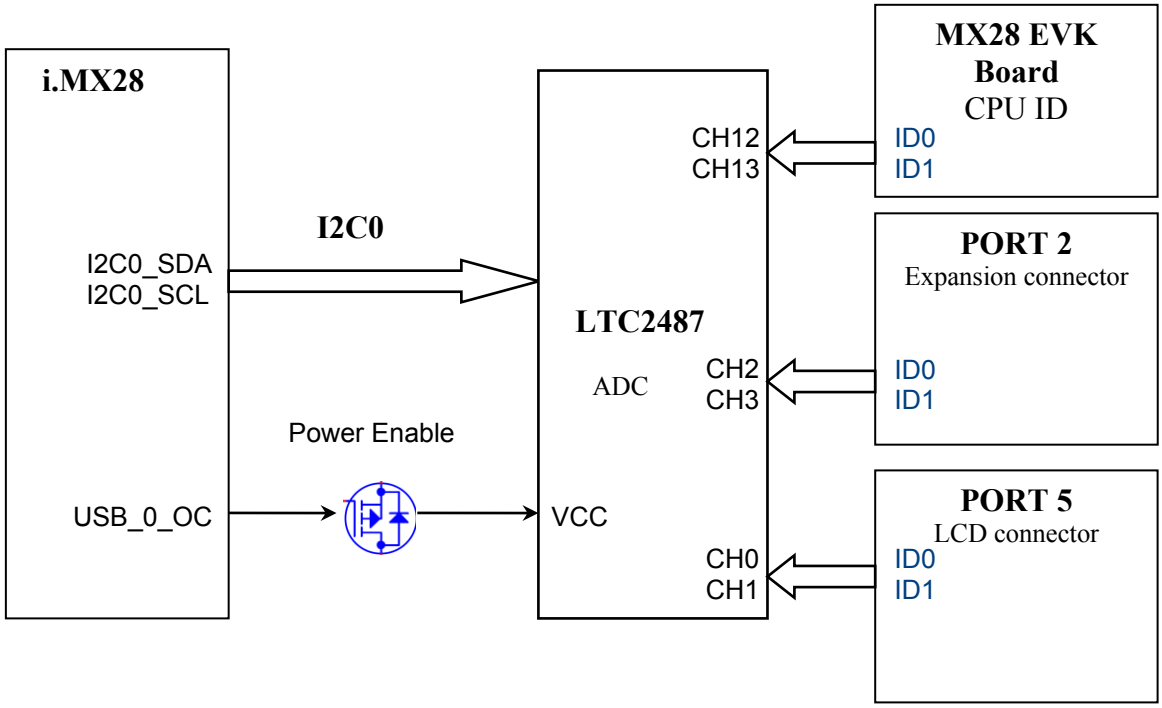

Figure 2-15 Board HW Identification Block Diagram

Notes:

1. The LTC2487 uses the MX28 USB_0_OC signal as a GPIO pin for power gating Q14. This will power up / power down the board identification feature.
   0 = power up
   1 = power down

2. The board identification circuit allows the firmware to identify the type of board hardware that is being used.
   a. The type and version of the LCD/display card being used.
   b. The type and version of the expansion port card being used
   c. The version of the MX28 EVK board the firmware is running on.

2.15 User Button Interface

Figure 2-16 shows the user button interface block diagram.

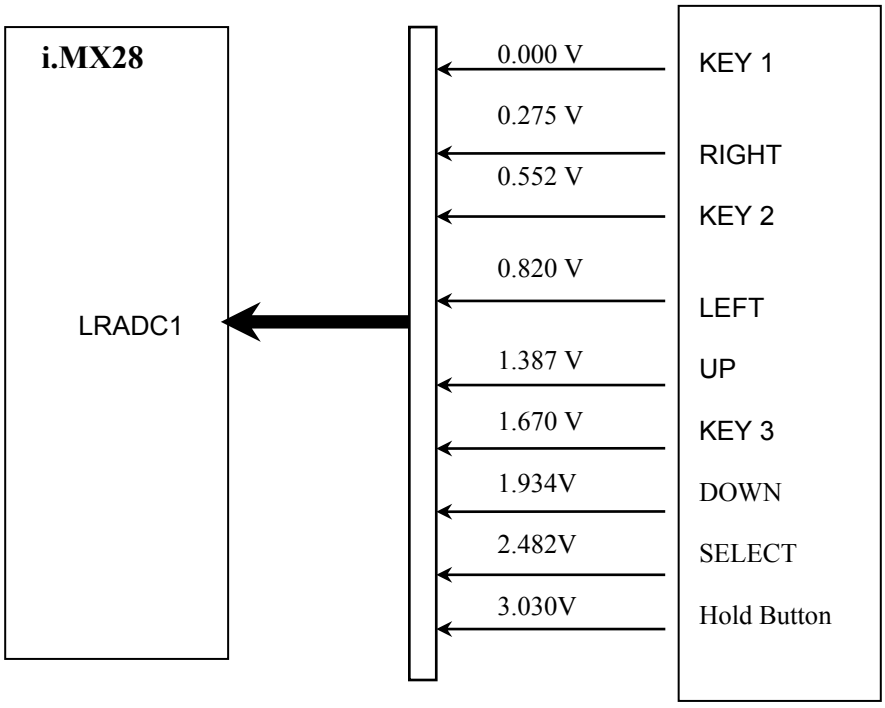

Figure 2-16 Block Diagram of the User Buttons

Notes:

1. An analog resistive ladder/divider is used for the button array. Pressing a button will generate a different analog voltage level, which can be read using the MX28 LRADC input to distinguish between button presses.
2. There are 8 buttons and 1 switch (HOLD) on the EVK board.
3. Example target reference voltage values are shown above for each button press given a VDDIO voltage of 3.3V.

Other Buttons:

1. POWER button – this button will engage the MX28 PSWITCH pin, which will startup the processor and the MX28 DCDC converter.
2. RESET button – this button will reset the MX28 processor.
3. RECOVERY button – holding this button down for >5 seconds will cause the MX28 to perform a USB boot.

2.16 Power Supply

2.16.1 Power Block

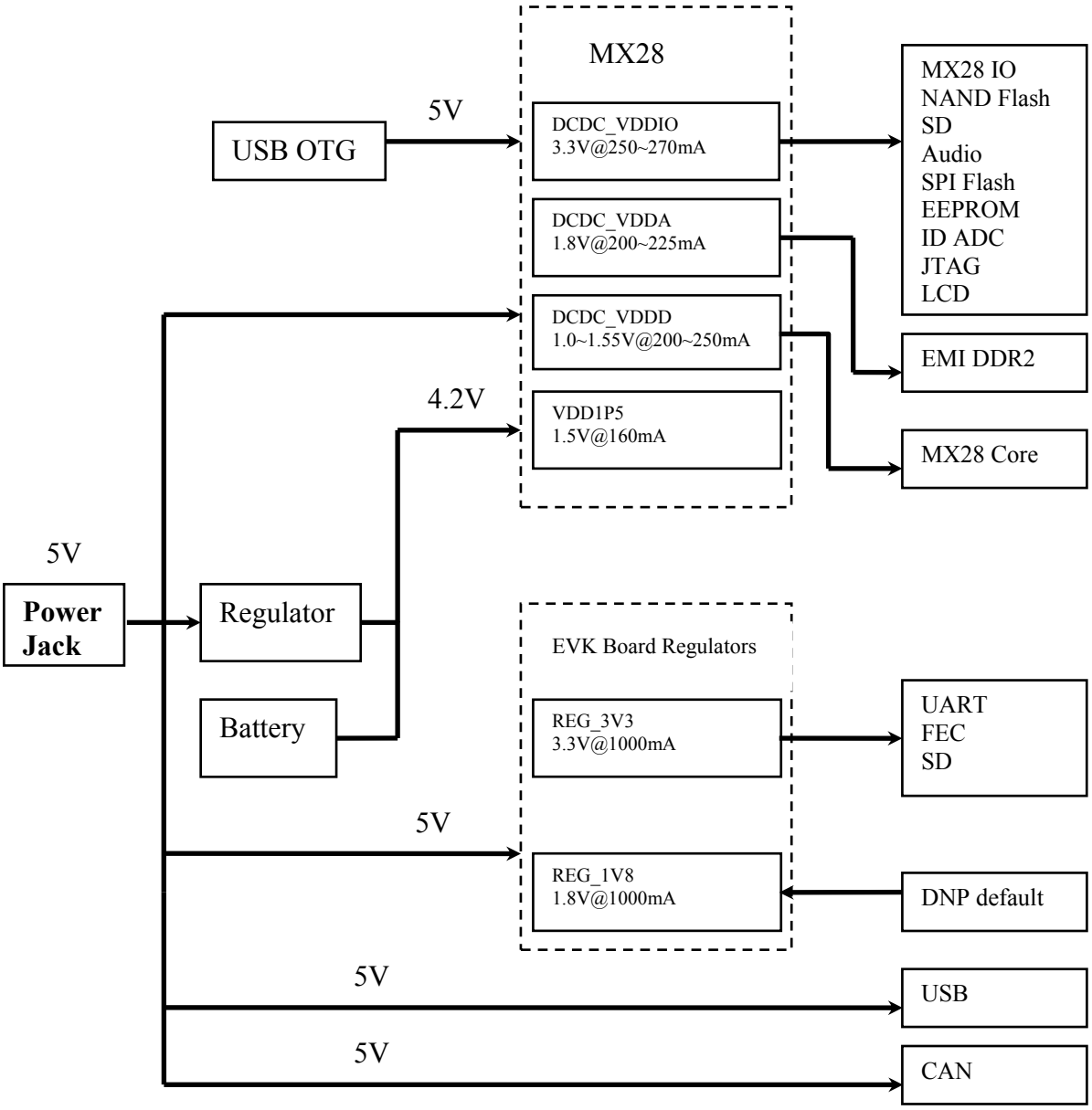

Figure 2-17 i.MX28 EVK Power Supply Diagram

2.16.2 i.MX28 Power Allocation

Table 2-2 i.MX28 Power Allocation List

Power net	Voltage Level	Module
DCDC_VDDA	1.8V	EMI DDR2
DCDC_VDDIO	3.3V	GPMI
DCDC_VDDIO	3.3V	SSP
DCDC_VDDIO	3.3V	UART
DCDC_VDDIO	3.3V	ADC
DCDC_VDDIO	3.3V	USB
DCDC_VDDIO	3.3V	CAN
DCDC_VDDIO	3.3V	ENET
DCDC_VDDIO	3.3V	LCD
DCDC_VDDIO	3.3V	SAIF
DCDC_VDDIO	3.3V	JTAG

2.16.3 Power Measurement Points

Table 2-3 Power measurement points on the EVK board

Power supply Group	Voltage level	Probe Component
REG_4V2	4.2V	Sense resistor R253
Battery	4.2V	Sense resistor R242
DCDC_VDDIO	3.3V	Sense resistor R7 and R8
DCDC_VDDA	1.8V	Sense resistor R1 ,R2,and R9
DCDC_VDDD	1.0~1.5V	Sense resistor R3
REG_3V3	3.3V	Sense resistor R230
REG_1V8	1.8V	Sense resistor R239

2.17 JTAG

Figure **2-18** shows the JTAG circuitry on the i.MX28 EVK board:

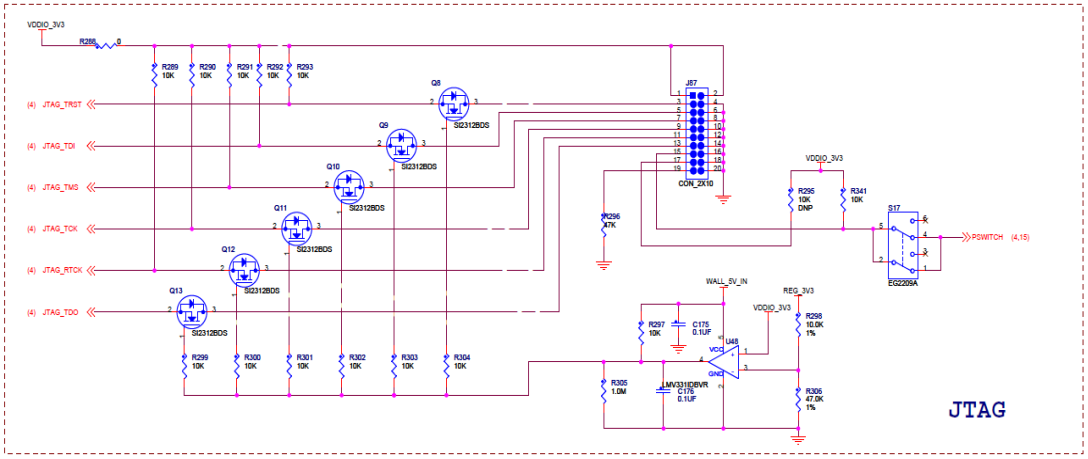

Figure 2-18 JTAG Schematic Drawing

The JTAG disconnected circuit uses FETs Q8-Q13 to disconnect the JTAG signals between the JTAG connector, J87, and the i.MX28 processor. The signal lines are disconnected when the i.MX28 shuts down to prevent back powering from the JTAG tool into the i.MX28 processor. The disconnect circuit is triggered by the falling edge of the VDDIO_3V3 supply via comparator U48 when the i.MX28 processor shuts down.

A standard 20 pin JTAG connector is used. There is also a switch (S17) that can be used to disconnect the JTAG system reset (SRST) signal from the i.MX28 processor PSWITCH pin. When the SRST signal is disconnected, this will prevent a fast falling edge on the i.MX28 PSWITCH pin when a reset command is issued (using the debugger), thereby preventing the i.MX28 processor from resetting and shutting down.

2.18 I/O MUX

Table 2-4 shows the i.MX28 pin connections to the various peripheral signal pins and the MUX position used by the BSP software.

Table 2-4 I/O MUX

PAD Name	Port	MUX Position	MUX 0	MUX 1	MUX 2
AUART0_RX	AUART0	0	AUART0_RX	I2C0_SCL	DUART_CTS
AUART0_TX	AUART0	0	AUART0_TX	I2C0_SDA	DUART_RTS
AUART0_RTS	AUART0	0	AUART0_RTS	AUART4_TX	DUART_TX
AUART0_CTS	AUART0	0	AUART0_CTS	AUART4_RX	DUART_RX
AUART1_RX	LED0 (PWM0)	GPIO	AUART1_RX	SSP2_CARD_DETECT	PWM_0
AUART1_TX	LED0 (PWM1) or Touch Reset	GPIO	AUART1_TX	SSP3_CARD_DETECT	PWM_1

Table 2-4 I/O MUX

PAD Name	Port	MUX Position	MUX 0	MUX 1	MUX 2
AUART1_RTS	USB0_ID	1	AUART1_RTS	USB0_ID	TIMROT_ROTARYB
AUART1_CTS	USB0_OC or ID ADC power gating	1 or GPIO	AUART1_CTS	USB0_OVERCURRENT	TIMROT_ROTARYA
AUART2_RX	USB1_PWR_EN	GPIO	AUART2_RX	SSP3_D1	SSP3_D4
AUART2_TX	USB0_PWR_EN	GPIO	AUART2_TX	SSP3_D2	SSP3_D5
AUART2_RTS	SAIF1_LRCLK or I2C1(SDA)	1 or 2	AUART2_RTS	I2C1_SDA	SAIF1_LRCLK
AUART2_CTS	SAIF1_BITCLK or I2C1(SCL)	1 or 2	AUART2_CTS	I2C1_SCL	SAIF1_BITCLK
AUART3_RX	AUART3	0	AUART3_RX	CAN0_TX	ENET0_1588_EVENT0_OUT
AUART3_TX	AUART3	0	AUART3_TX	CAN0_RX	ENET0_1588_EVENT0_IN
AUART3_RTS	AUART3	0	AUART3_RTS	CAN1_RX	ENET0_1588_EVENT1_IN
AUART3_CTS	AUART3	0	AUART3_CTS	CAN1_TX	ENET0_1588_EVENT1_OUT
ENET0_TX_CLK	Ethernet Interrupt (0+1)	GPIO	ENET0_TX_CLK	HSADC_TRIGGER	ENET0_1588_EVENT2_OUT
ENET0_RX_CLK	Ethernet Reset(0+1)	GPIO	ENET0_RX_CLK	ENET0_RX_ER	ENET0_1588_EVENT2_IN
ENET0_TXD1	ENET0	0	ENET0_TXD1	GPMI_READY7	
ENET0_TXD0	ENET0	0	ENET0_TXD0	GPMI_READY6	
ENET0_RX_EN	ENET0	0	ENET0_RX_EN	GPMI_CE6N	SAIF1_SDATA1
ENET0_RXD1	ENET0	0	ENET0_RXD1	GPMI_READY4	
ENET0_RXD0	ENET0	0	ENET0_RXD0	GPMI_CE7N	SAIF1_SDATA2
ENET0_TX_EN	ENET0	0	ENET0_TX_EN	GPMI_READY5	
ENET0_MDC	ENET 0+1	0	ENET0_MDC	GPMI_CE4N	SAIF0_SDATA1
ENET0_MDIO	ENET 0+1	0	ENET0_MDIO	GPMI_CE5N	SAIF0_SDATA2
ENET0_RXD2	ENET1_RXD0	1	ENET0_RXD2	ENET1_RXD0	ENET0_1588_EVENT0_OUT
ENET0_RXD3	ENET1_RXD1	1	ENET0_RXD3	ENET1_RXD1	ENET0_1588_EVENT0_IN
ENET0_CRS	ENET1_RX_EN	1	ENET0_CRS	ENET1_RX_EN	ENET0_1588_EVENT3_IN
ENET0_TXD3	ENET1_TXD1	1	ENET0_TXD3	ENET1_TXD1	ENET0_1588_EVENT1_IN
ENET0_TXD2	ENET1_TXD0	1	ENET0_TXD2	ENET1_TXD0	ENET0_1588_EVENT1_OUT
ENET0_COL	ENET1_TX_EN	1	ENET0_COL	ENET1_TX_EN	ENET0_1588_EVENT3_OUT
ENET_CLK	ENET 0+1	0	CLKCTRL_ENET		
GPMI_D00	NAND + SD	0 or 1	GPMI_D0	SSP1_D0	
GPMI_D01	NAND + SD	0 or 1	GPMI_D1	SSP1_D1	
GPMI_D02	NAND + SD	0 or 1	GPMI_D2	SSP1_D2	
GPMI_D03	NAND + SD	0 or 1	GPMI_D3	SSP1_D3	
GPMI_D04	NAND + SD	0 or 1	GPMI_D4	SSP1_D4	
GPMI_D05	NAND + SD	0 or 1	GPMI_D5	SSP1_D5	
GPMI_D06	NAND + SD	0 or 1	GPMI_D6	SSP1_D6	
GPMI_D07	NAND + SD	0 or 1	GPMI_D7	SSP1_D7	
GPMI_ALE	NAND	0	GPMI_ALE	SSP3_D1	SSP3_D4
GPMI_RESETN	NAND+ SD1 (WP)	0 or 1	GPMI_RESETN	SSP3_CMD	
GPMI_RDN	NAND	0	GPMI_RDN	SSP3_SCK	
GPMI_WRN	NAND + SD	0 or 1	GPMI_WRN	SSP1_SCK	
GPMI_CLE	NAND	0	GPMI_CLE	SSP3_D2	SSP3_D5
GPMI_RDY0	NAND + SD	0 or 1	GPMI_READY0	SSP1_CARD_DETECT	USB0_ID
GPMI_RDY1	NAND + SD	0 or 1	GPMI_READY1	SSP1_CMD	

Table 2-4 I/O MUX

PAD Name	Port	MUX Position	MUX 0	MUX 1	MUX 2
GPMI_CE0N	NAND + SD	0 or 1	GPMI_CE0N	SSP3_D0	
GPMI_CE1N	NAND + SD	0 or 1	GPMI_CE1N	SSP3_D3	
GPMI_RDY2	CAN0_TX	1	GPMI_READY2	CAN0_TX	ENET0_TX_ER
GPMI_RDY3	CAN0_RX or HSADC_TRIGGER	1 or 2	GPMI_READY3	CAN0_RX	HSADC_TRIGGER
GPMI_CE2N	CAN1_TX	1	GPMI_CE2N	CAN1_TX	ENET0_RX_ER
GPMI_CE3N	CAN1_RX	1	GPMI_CE3N	CAN1_RX	SAIF1_MCLK
I2C0_SCL	I2C0	0	I2C0_SCL	TIMROT_ROTARYA	DUART_RX
I2C0_SDA	I2C0	0	I2C0_SDA	TIMROT_ROTARYB	DUART_TX
LCD_D00	LCD	0	LCD_D0		ETM_DA0
LCD_D01	LCD	0	LCD_D1		ETM_DA1
LCD_D02	LCD	0	LCD_D2		ETM_DA2
LCD_D03	LCD	0	LCD_D3	ETM_DA8	ETM_DA3
LCD_D04	LCD	0	LCD_D4	ETM_DA9	ETM_DA4
LCD_D05	LCD	0	LCD_D5		ETM_DA5
LCD_D06	LCD	0	LCD_D6		ETM_DA6
LCD_D07	LCD	0	LCD_D7		ETM_DA7
LCD_D08	LCD	0	LCD_D8	ETM_DA3	ETM_DA8
LCD_D09	LCD	0	LCD_D9	ETM_DA4	ETM_DA9
LCD_D10	LCD	0	LCD_D10		ETM_DA10
LCD_D11	LCD	0	LCD_D11		ETM_DA11
LCD_D12	LCD	0	LCD_D12		ETM_DA12
LCD_D13	LCD	0	LCD_D13		ETM_DA13
LCD_D14	LCD	0	LCD_D14		ETM_DA14
LCD_D15	LCD	0	LCD_D15		ETM_DA15
LCD_D16	LCD	0	LCD_D16		ETM_DA7
LCD_D17	LCD	0	LCD_D17		ETM_DA6
LCD_D18	LCD	0	LCD_D18		ETM_DA5
LCD_D19	LCD	0	LCD_D19		ETM_DA4
LCD_D20	LCD	0	LCD_D20	ENET1_1588_EVENT2_OUT	ETM_DA3
LCD_D21	LCD	0	LCD_D21	ENET1_1588_EVENT2_IN	ETM_DA2
LCD_D22	LCD	0	LCD_D22	ENET1_1588_EVENT3_OUT	ETM_DA1
LCD_D23	LCD	0	LCD_D23	ENET1_1588_EVENT3_IN	ETM_DA0
LCD_VSYNC	SAIF1_SDATA0	1	LCD_VSYNC	SAIF1_SDATA0	
LCD_HSYNC	SAIF1_SDATA1	1	LCD_HSYNC	SAIF1_SDATA1	ETM_TCTL
LCD_DOTCLK	SAIF1_MCLK	1	LCD_DOTCLK	SAIF1_MCLK	ETM_TCLK
LCD_ENABLE	Touch I2C Interrupt - LCD	GPIO	LCD_ENABLE		
LCD_RS	LCD_DOTCLK	1	LCD_RS	LCD_DOTCLK	
LCD_RESET	LCD_PWR_EN	0	LCD_RESET	LCD_VSYNC	
LCD_CS	LCD_ENABLE	1	LCD_CS	LCD_ENABLE	
LCD_RD_E	LCD_VSYNC	1	LCD_RD_E	LCD_VSYNC	ETM_TCTL
LCD_WR_RWN	LCD_HSYNC	1	LCD_WR_RWN	LCD_HSYNC	ETM_TCLK
PWM0	DUART_RX	2	PWM_0	I2C1_SCL	DUART_RX
PWM1	DUART_TX	2	PWM_1	I2C1_SDA	DUART_TX

Table 2-4 I/O MUX

PAD Name	Port	MUX Position	MUX 0	MUX 1	MUX 2
PWM2	BACKLIGHT_PWM	0	PWM_2	USB0_ID	USB1_OVERCURRENT
PWM3	SSP0 Power Gating	0	PWM_3		
PWM4	SSP1 Power Gating	0	PWM_4		
SAIF0_SDATA0	SAIF0	0	SAIF0_SDATA0	PWM_6	AUART4_TX
SAIF0_MCLK	SAIF0	0	SAIF0_MCLK	PWM_3	AUART4_CTS
SAIF0_BITCLK	SAIF0	0	SAIF0_BITCLK	PWM_5	AUART4_RX
SAIF0_LRCLK	SAIF0	0	SAIF0_LRCLK	PWM_4	AUART4_RTS
SAIF1_SDATA0	SAIF0_SDATA1	0	SAIF1_SDATA0	PWM_7	SAIF0_SDATA1
SPDIF	SPDIF	0	SPDIF_TX		ENET1_RX_ER
SSP0_CMD	SSP0	0	SSP0_CMD		
SSP0_SCK	SSP0	0	SSP0_SCK		
SSP0_DATA0	SSP0	0	SSP0_D0		
SSP0_DATA1	SSP0	0	SSP0_D1		
SSP0_DATA2	SSP0	0	SSP0_D2		
SSP0_DATA3	SSP0	0	SSP0_D3		
SSP0_DATA4	SSP0	0	SSP0_D4	SSP2_D0	
SSP0_DATA5	SSP0	0	SSP0_D5	SSP2_D3	
SSP0_DATA6	SSP0	0	SSP0_D6	SSP2_CMD	
SSP0_DATA7	SSP0	0	SSP0_D7	SSP2_SCK	
SSP0_DETECT	SSP0	0	SSP0_CARD_DETECT		
SSP1_SCK	SSP0 WP	GPIO	SSP1_SCK	SSP2_D1	ENET0_1588_EVENT2_OUT
SSP1_CMD	CAN Power down	GPIO	SSP1_CMD	SSP2_D2	ENET0_1588_EVENT2_IN
SSP1_DATA0	Headphone Detect	GPIO	SSP1_D0	SSP2_D6	ENET0_1588_EVENT3_OUT
SSP1_DATA3	Ethernet PWR_EN	GPIO	SSP1_D3	SSP2_D7	ENET0_1588_EVENT3_IN
SSP2_MOSI	SPI2	0	SSP2_CMD	AUART2_TX	SAIF0_SDATA2
SSP2_MISO	SPI2	0	SSP2_D0	AUART3_RX	SAIF1_SDATA1
SSP2_SCK	SPI2	0	SSP2_SCK	AUART2_RX	SAIF0_SDATA1
SSP2_SS0	SPI2	0	SSP2_D3	AUART3_TX	SAIF1_SDATA2
SSP2_SS1	USB1_OVERCURRENT	2	SSP2_D4	SSP2_D1	USB1_OVERCURRENT
SSP2_SS2	SPI2(ss2)	0	SSP2_D5	SSP2_D2	USB0_OVERCURRENT
SSP3_MOSI	GPIO2_25	GPIO	SSP3_CMD	AUART4_RX	ENET1_1588_EVENT0_IN
SSP3_MISO	GPIO2_26	GPIO	SSP3_D0	AUART4_RTS	ENET1_1588_EVENT1_OUT
SSP3_SS0	GPIO2_27	GPIO	SSP3_D3	AUART4_CTS	ENET1_1588_EVENT1_IN
SSP3_SCK	wall_5v_insert_detect(GPIO2_24)	GPIO	SSP3_SCK	AUART4_TX	ENET1_1588_EVENT0_OUT

2.19 Interface, Switches, and Jumpers

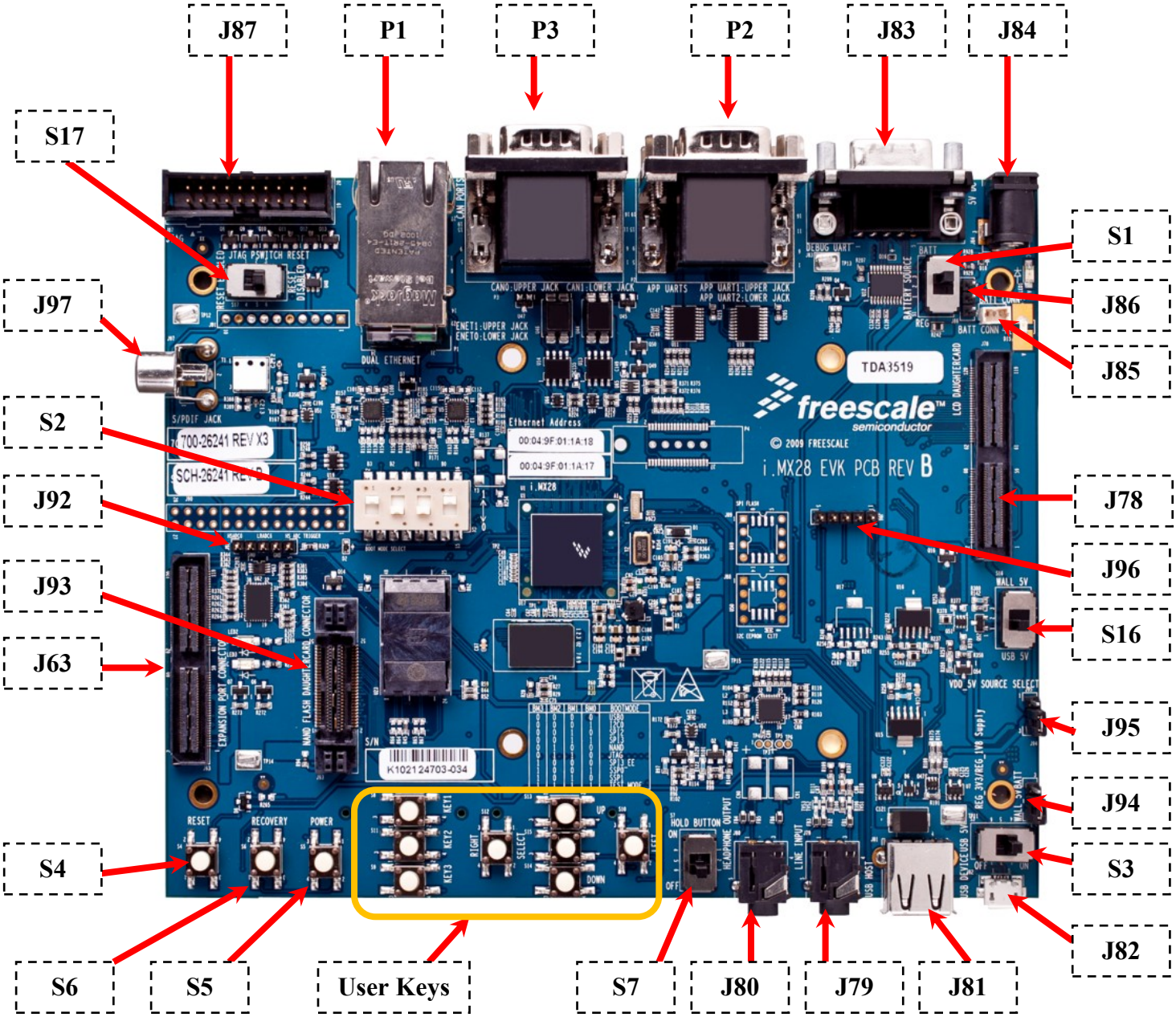

Figure 2-19 Interface, Switches, and Jumpers

Figure 2-19 shows the following:

1. **Switches:**

   S1: Battery source selection switch
   Upper position: real 4.2V Li-ion battery using J85/J86.
   Lower position: simulated 4.2V battery with on-board EVK 4.2V regulator.

   S2: Boot mode select switch
   Please refer to Chapter 5 (Boot Mode) in this document for details.

   S3: USB 5V Power switch
   Left position: USB 5V “OFF” / disconnected
   Right position: USB 5V “ON” / connected

   S7: HOLD switch
   Upper position: The user keys are locked.
   Lower position: The user keys are unlocked.

   S16: I.MX28 VDD5V supply selection switch
   Upper position: power source is Wall 5V
   Lower position: power source is USB 5V

   S17: JTAG reset switch
   Left position--- JTAG Reset “Enabled”
   Right position--- JTAG Reset “Disabled”

2. **Buttons:**

   S4: “Reset” button
   S5: “Power” button
   S6: “Recovery” button

3. **User Keys:**

   S8: KEY1
   S9: KEY3
   S10: RIGHT
   S11: KEY2
   S12: LEFT
   S13: UP
   S14: DOWN
   S15: SELECT

4. **Jumpers:**

J94: Selects the power source of the EVK board 3.3V regulator and 1.8V regulator.
Upper two pins shorted: regulator power source is WALL 5V.
Lower two pins shorted: regulator power source is the battery supply (via battery connector or 4.2V regulator).

J95: Selects the power source of the LCD backlight
Upper two pins shorted: power source is WALL 5V.
Lower two pins shorted: power source is the i.MX28 VDD4P2 output.

5. **Interface Connectors:**

P1: Dual Ethernet RJ45 connector
The upper jack is ENET1.
The lower jack is ENET0.

P2: Application UART dual stack DB9 connector
The upper jack is UART1.
The lower jack is UART2.

P3: CAN (Controller Area Network) dual stack DB9 connector
The upper jack is CAN0.
The lower jack is CAN1.

J63: Expansion port connector
J78: LCD port connector
J79: LINE INPUT
J80: Headphone / Line Output
J81: USB HOST jack
J82: USB OTG jack
J83: Debug UART DB9 connector
J84: WALL 5V Power Jack
J85: 2mm (4.2V Li-ion) battery connector
J86: 2.5mm (4.2V (Li-ion) battery header
J87: JTAG connector (20 pin standard)
J92: HSADC header
J93: NAND Flash daughter-card connector
J96: LRADC / touch screen header
J97: S/PDIF RCA connector

Figure 2-20 shows the following connectors:

U42: SD Card socket 0

U43: SD Card socket 1

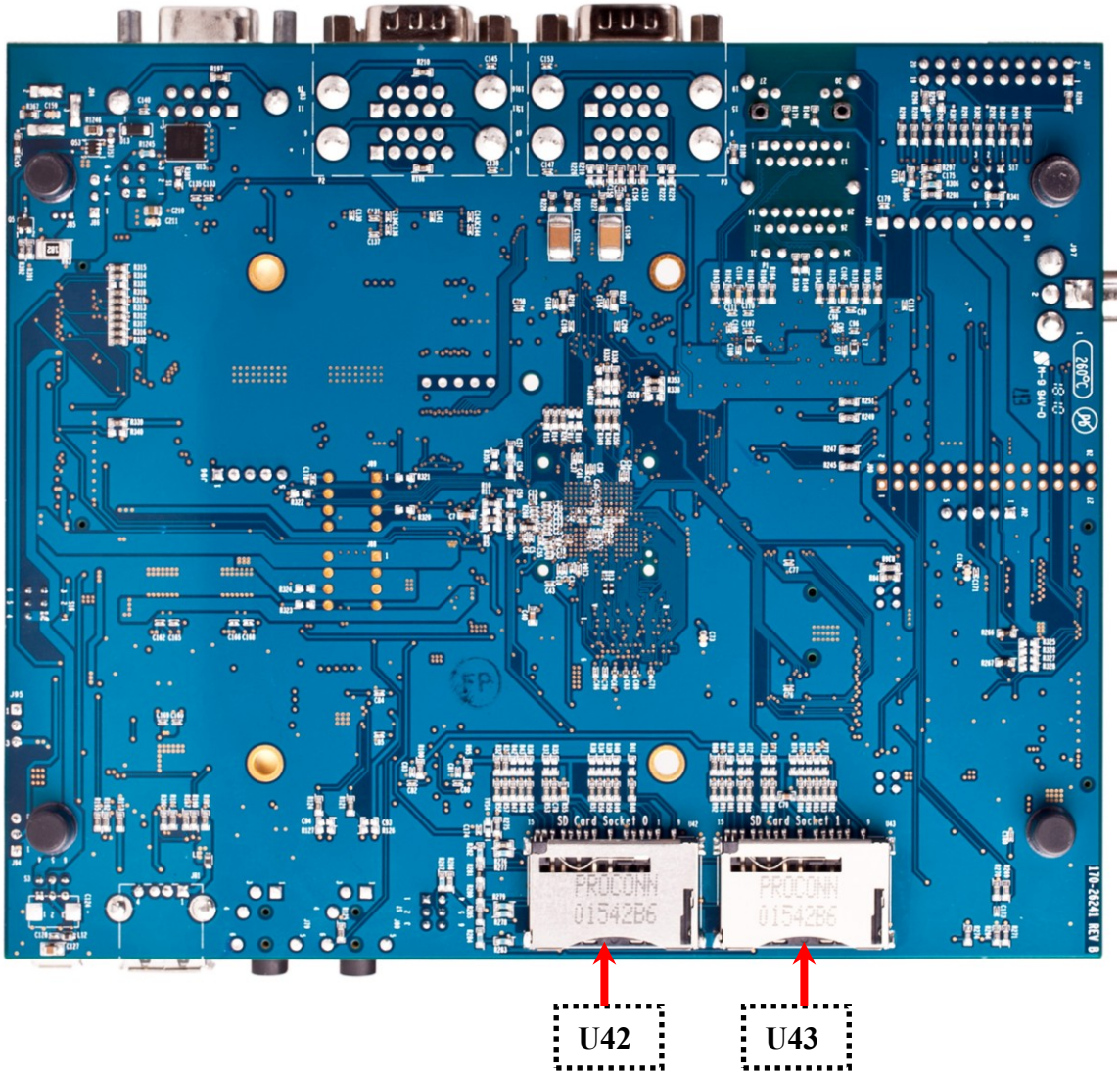

Figure 2-20 Interface Connectors

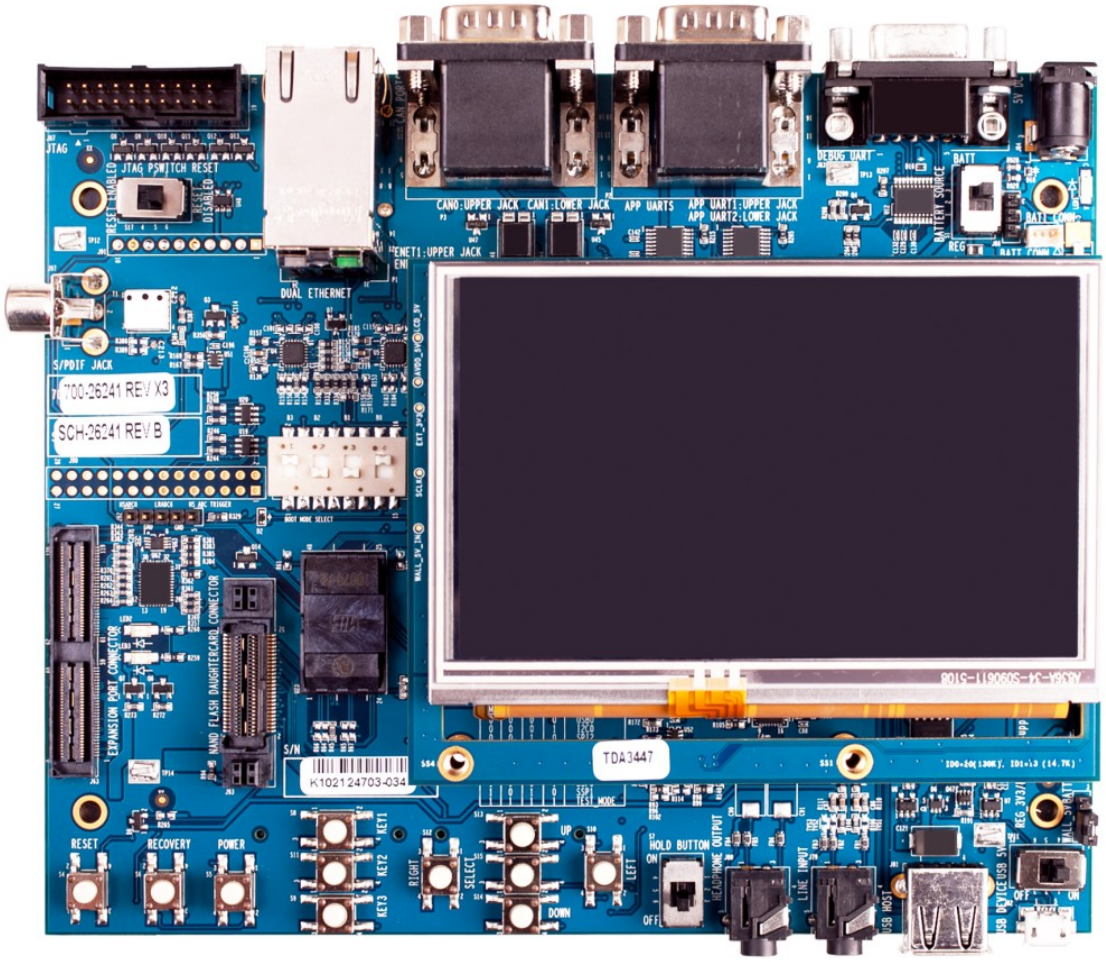

Figure 2-21 i.MX28 EVK Board with 4.3" WVGA Display Installed

Appendix A
Revision History

Table A-1 Revision History provides a revision history for this user's guide.

Table A-1 Revision History

Rev. Number	Date	Substantive Change(s)
Rev 0	07/2011	Initial release.

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