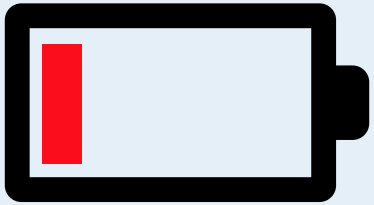
IMPROVING BATTERY-LIFE WITH ULTRA LOW-POWER PROCESSORS

NIK JEDRZEJEWSKI

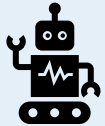
PRODUCT MANAGER

SECURE CONNECTIONS FOR A SMARTER WORLD

Why Do My Batteries Drain So Fast?



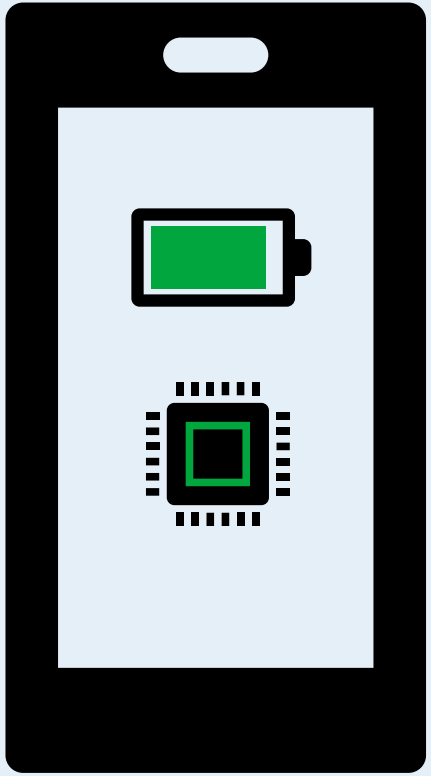
FOMO



What Can Be Done?

Make the Battery bigger?

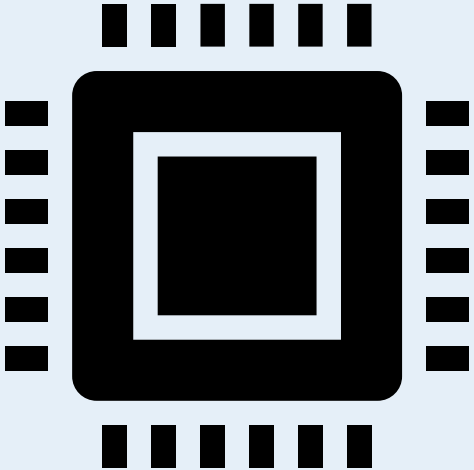
Cost, Weight ⬆



Make the Processor & SW more efficient?

Cost, Weight ⬇

Processor and SW Need to Be More Efficient



Process Technology

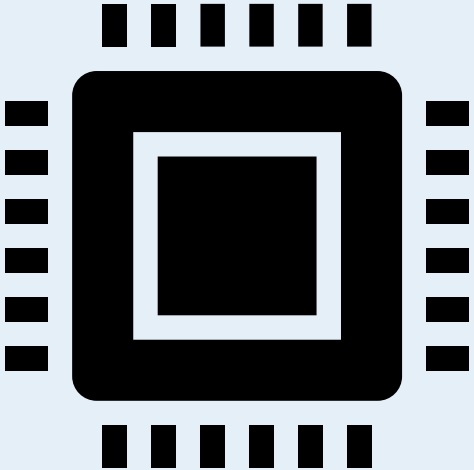
Power Domain Architecture

Software Enablement

IP choices

MPU Process Technology

60nm



40nm

28nm

Dynamic Power = I^2 x R

Longer internal traces increase Resistance

- Decreasing trace dimensions decreases
  - ✓ Trace Length
  - ✓ Resistance
  - ✓ Power

Dynamic Power = V^2/R

Lower voltages reduce power

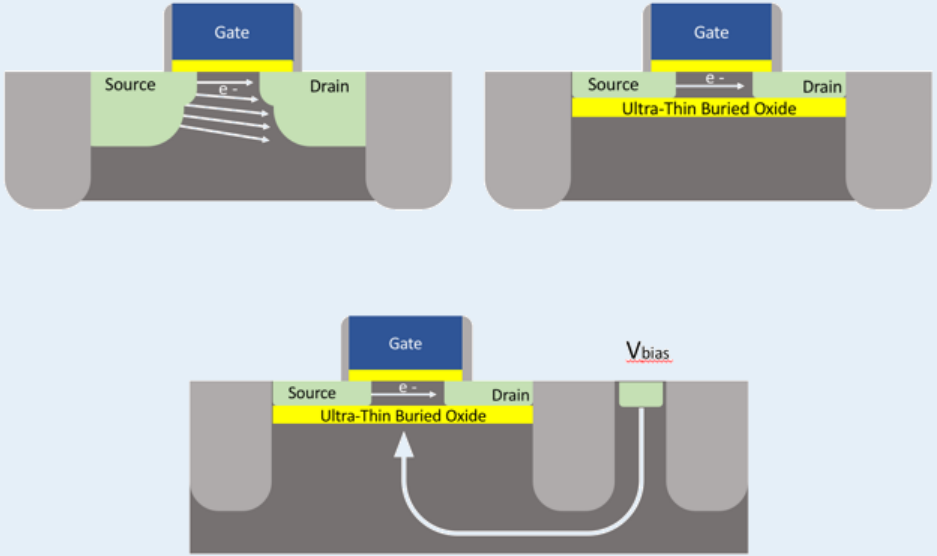
Static Power = Leakage

Transistor design is key as Leakage increases at smaller transistor dimensions.

- Limit electron flow in a transistor

Benefits of 28nm FDSOI

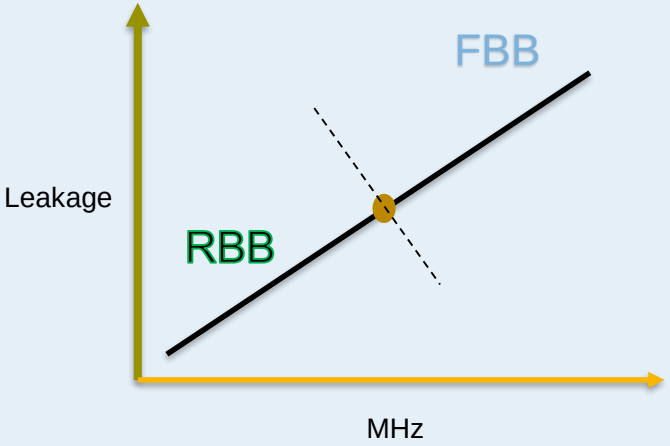
- **Power – Performance Benefits**
  - Improved electrostatics enables **shorter gate lengths**
  - Reduced device parasitics
  - Device back bias allows for **lower Vdd** while maintaining performance
  - **Device tuning** with back biasing to compensate process variation
- **Analog Integration and Performance Benefits**
  - Higher gain, better matching and lower 1/f noise
- **Better SER and Latchup Immunity**
  - **10-100x better** SER performance versus 28nm bulk alternatives
  - Thin buried oxide layer makes device immune to latch-up

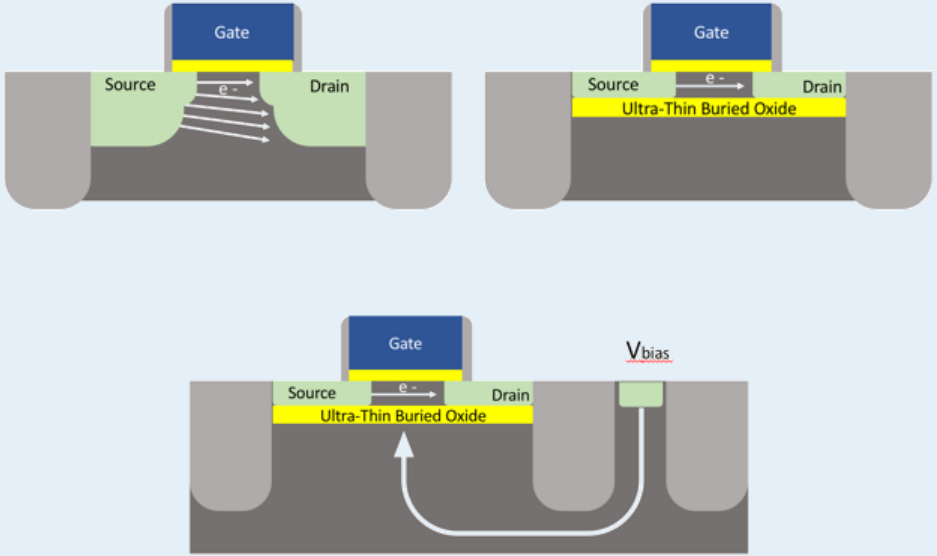


***Body Biasing**: Faster when required and more energy efficient when performance isn't as critical*

Benefits of 28nm FDSOI

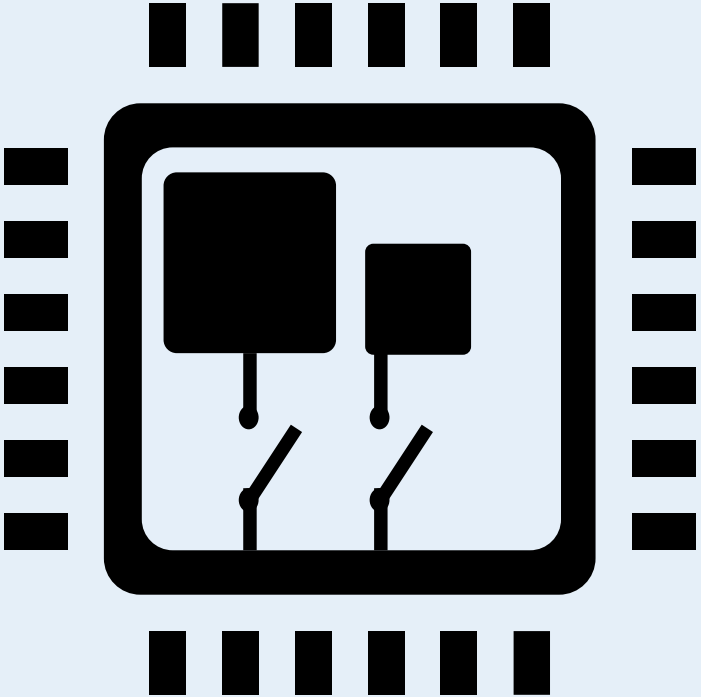
Allows user to tune transistors for a given use case





***Body Biasing**: Faster when required and more energy efficient when performance isn't as critical*

MPU Power Domain Architecture?

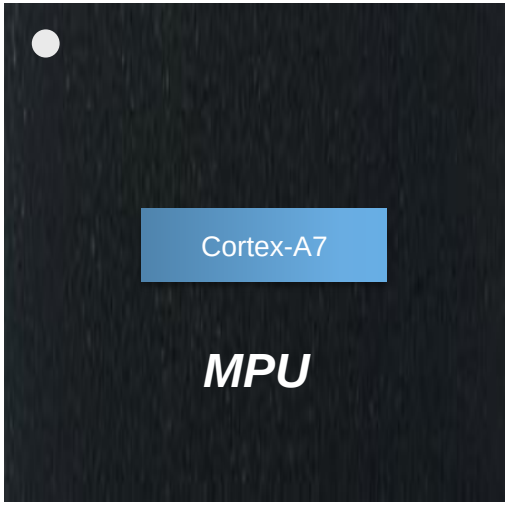


Heterogeneous Computing

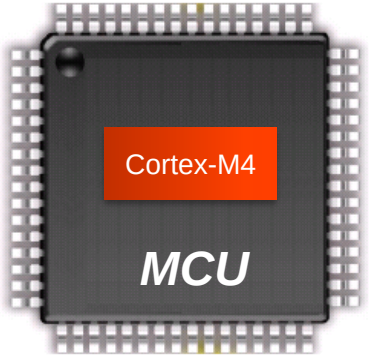
Cortex®-A domain

Cortex®-M domain

Maximizing Power Gated Silicon to Limit Leakage



vs.

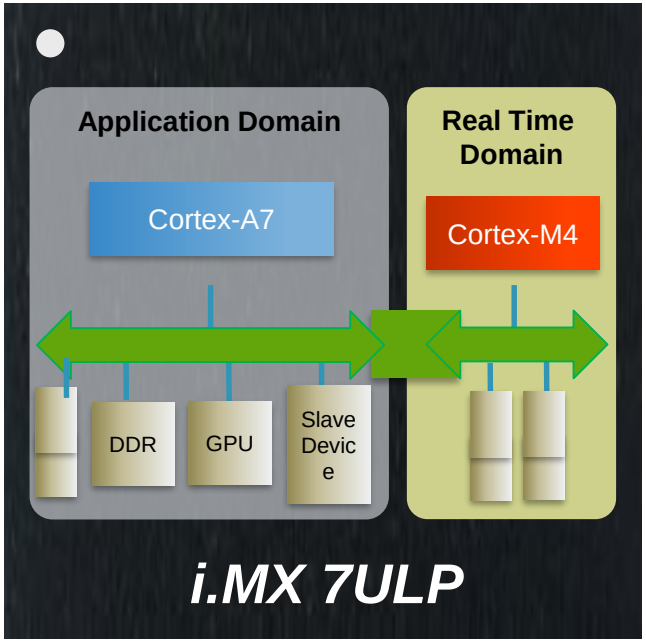


- High Core Processing Performance
- Rich OS support
- NEON Acceleration
- High Bandwidth
- MMU

- Real Time Performance
- Right Sized Processing
- Extreme Low Power Modes

Leveraging MPU & MCU in one device

Performance Peripherals

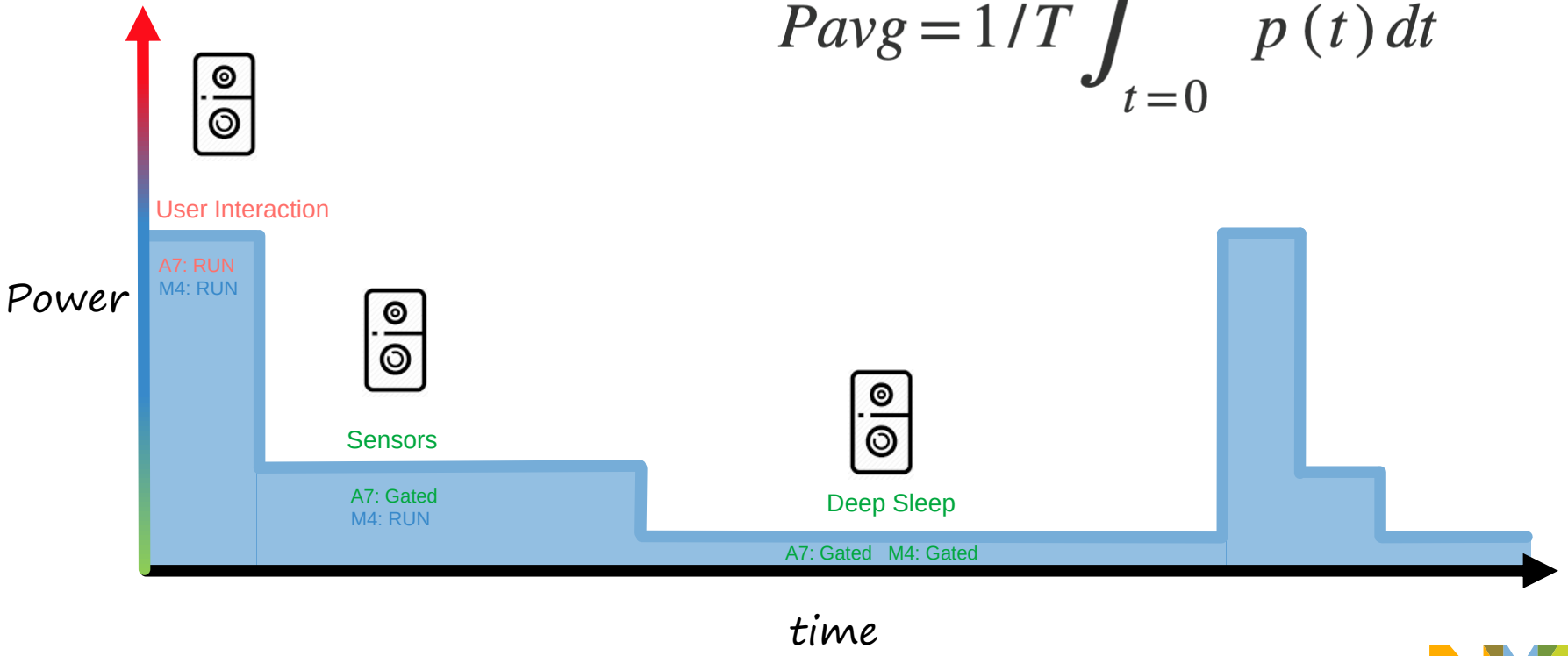


Low Power Peripherals

Heterogeneous Domain Based Computing

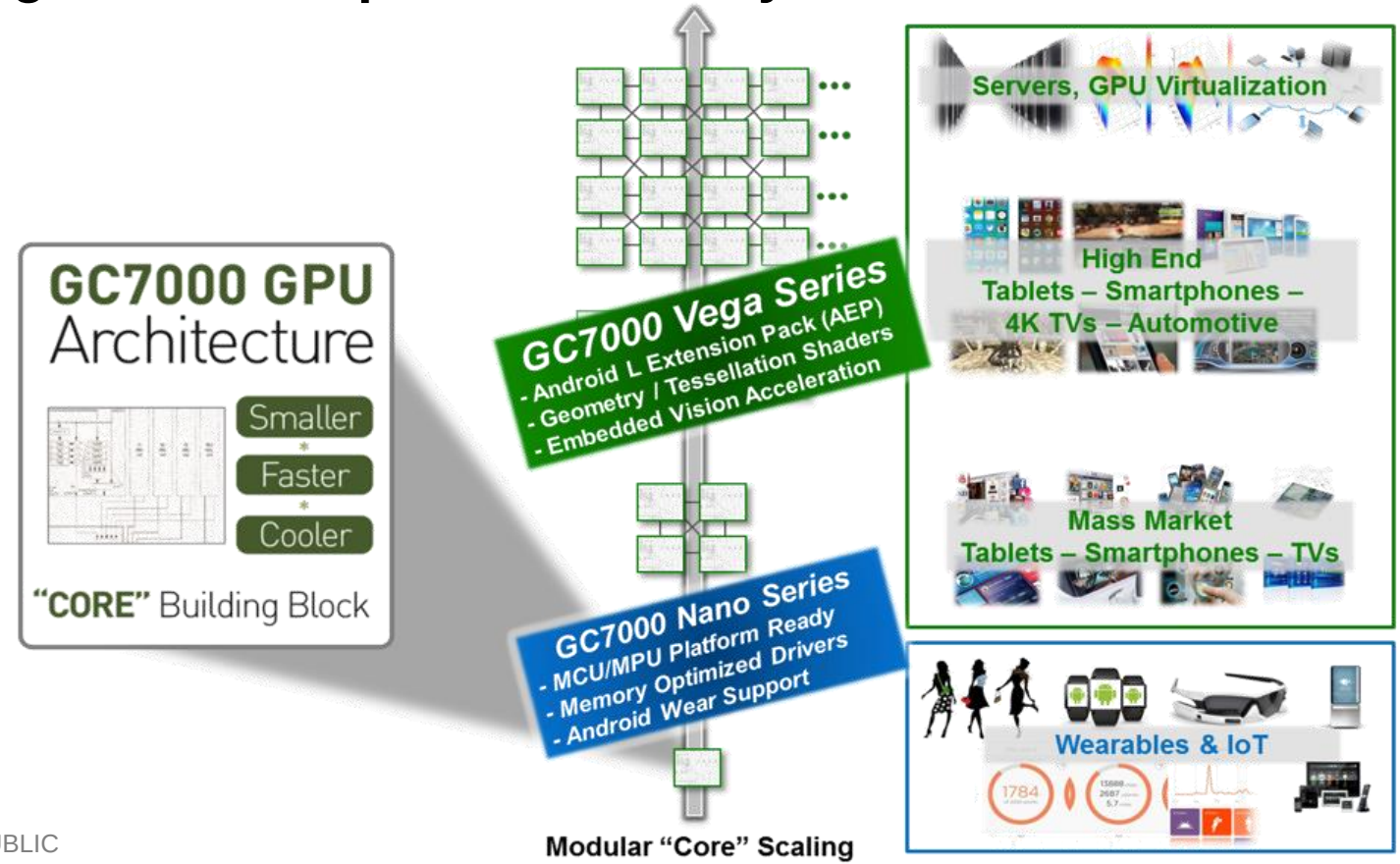
All Power Modes Add Up

$$Pavg = 1/T \int_{t=0}^{t=T} p(t)\,dt$$

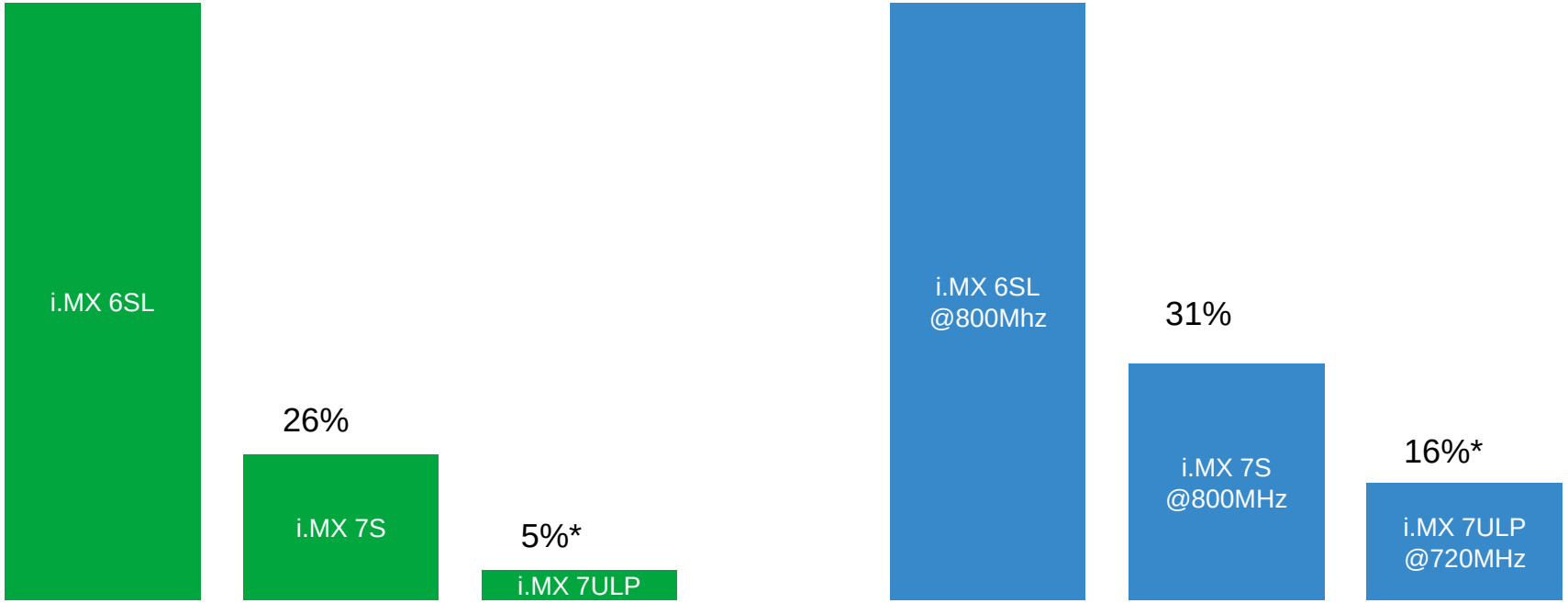


Vivante GPU Nano Series:

Right-sized for power efficiency

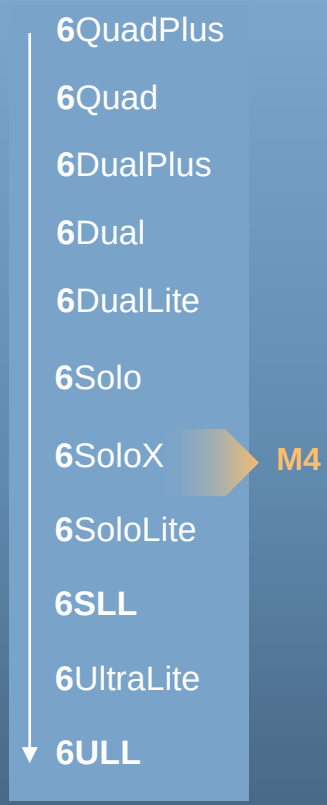


Progress in Power Consumption



* Preliminary measurements on early silicon
** Linux retained in LPDDR self refresh

ULP Family: Market Opportunity in Power Efficiency



i.MX 8 series M4
Advanced Graphics and Performance

i.MX 8M series M4
Advanced Audio and Video

i.MX 8X series M4
BOM and Energy Efficiency

Arm® v8-A
(32-Bit / 64-Bit)

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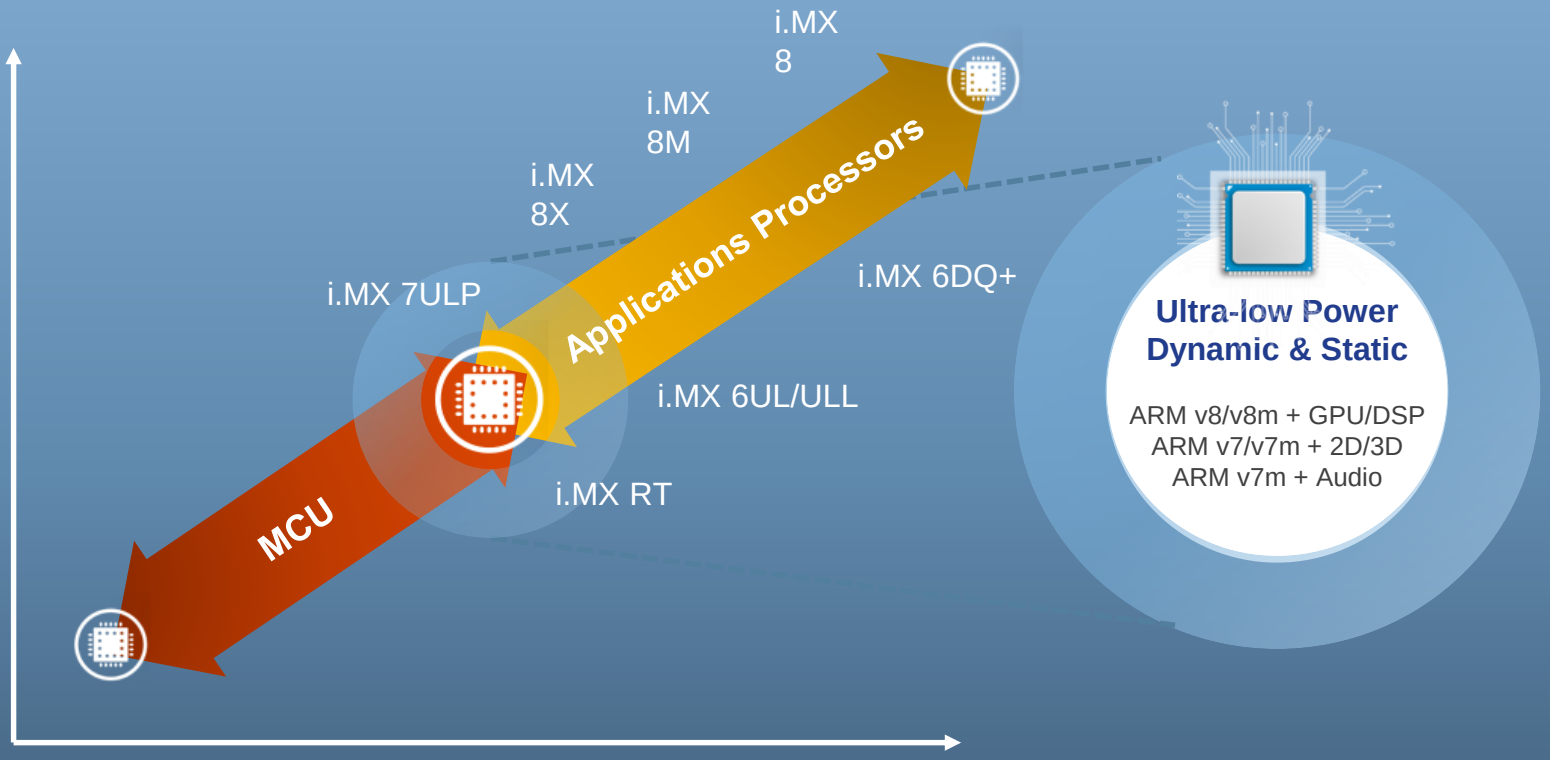
i.MX 7 M4
Flexible Efficient Connectivity

Arm® v7-A
(32-Bit)

i.MX 7ULP M4
Ultra Low Power with Graphics

The Best of Both Worlds



i.MX 7ULP

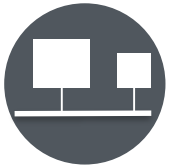
Bringing together **Apps Processor performance** and **MCU Low Power**

Ultra Low Power

- **FDSOI**
  - Effective control of the transistor channel through biasing
- **High Performance/mW** extending battery life for portable devices.
- **Performance on Demand** with fast wake up times

Efficient 3D & 2D Graphics

- **GC7000 nanoULTRA**
  - OpenGL ES 2.0/1.1
  - OpenVG 1.1
- **GC320 2D** Composition
  - Offloads tasks from 3D GPU
  - Stretch/Shrinking, rotation, GUI processing



Heterogeneous Computing

- **Multiple software execution**:
  - Powerful processing using **Cortex-A7** and Neon co-processor
  - Real-time performance through **Cortex-M4**
- **System integrity and security**
  - Resource Domain Controller
  - Fast Low Power Boot
  - Safe Recovery of Application domain

i.MX 7ULP Applications Processor

Specifications:

CPU:

- Cortex-A7 @ 720MHz
- Cortex-M4 @200MHz

Process: 28nm FD-SOI

Package:

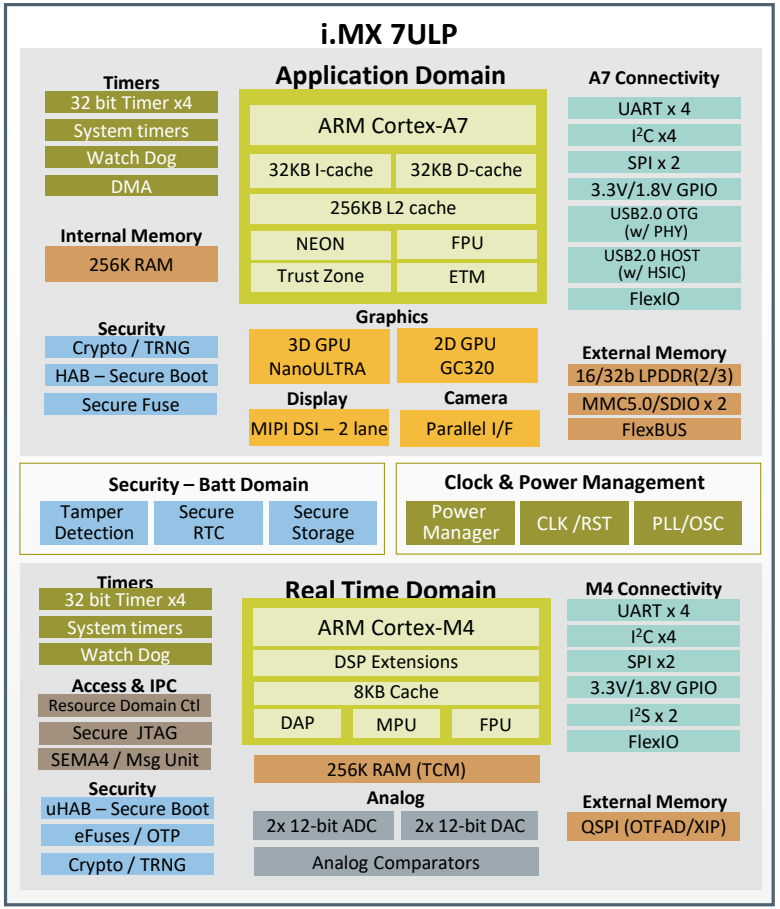
- 14x14 393BGA, 0.5mm pitch: **Consumer & Industrial**
- 10x10 361BGA, 0.5mm pitch: **Consumer Only**

Temp Range (junction):

Industrial: -40C to +105C
Consumer: 0C to +95C

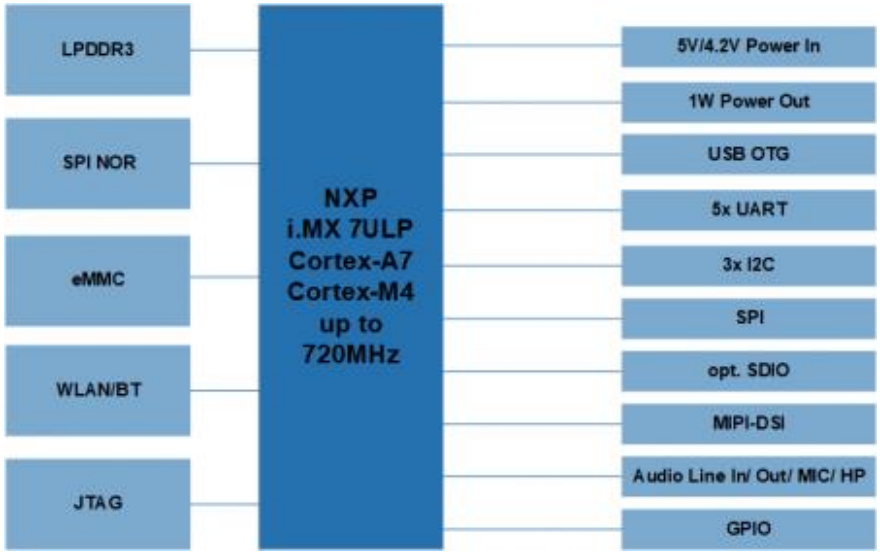
Key Features:

- Graphics
  - GC7000 nanoULTRA GPU: OpenGL 2.0 / OpenVG
  - GC320 Composition Engine
- Ultra Low Power
  - Independent Real-time domain
  - Ultra Low Run Current
- Memory options
  - QSPI (on the fly decryption)
  - 32-bit LPDDR2/3 @400MHz
  - eMMC 5.0 /SD3.0
- Connectivity
  - USB HS OTG with PHY
  - USB HS HOST HSIC
  - I2C X 8, SPI X 4, UART X 8, SDIO X 2, I2S X 2
- Security
  - High Assurance Boot
  - Crypto Acceleration: AES-128/256, SHA-1, SHA-224, SHA-256
  - RNG and Tamper Detection



*Application and Real Time Domain separately shown with respective peripherals
** Production frequencies are TBD until launch

PicoCore™MX7ULP



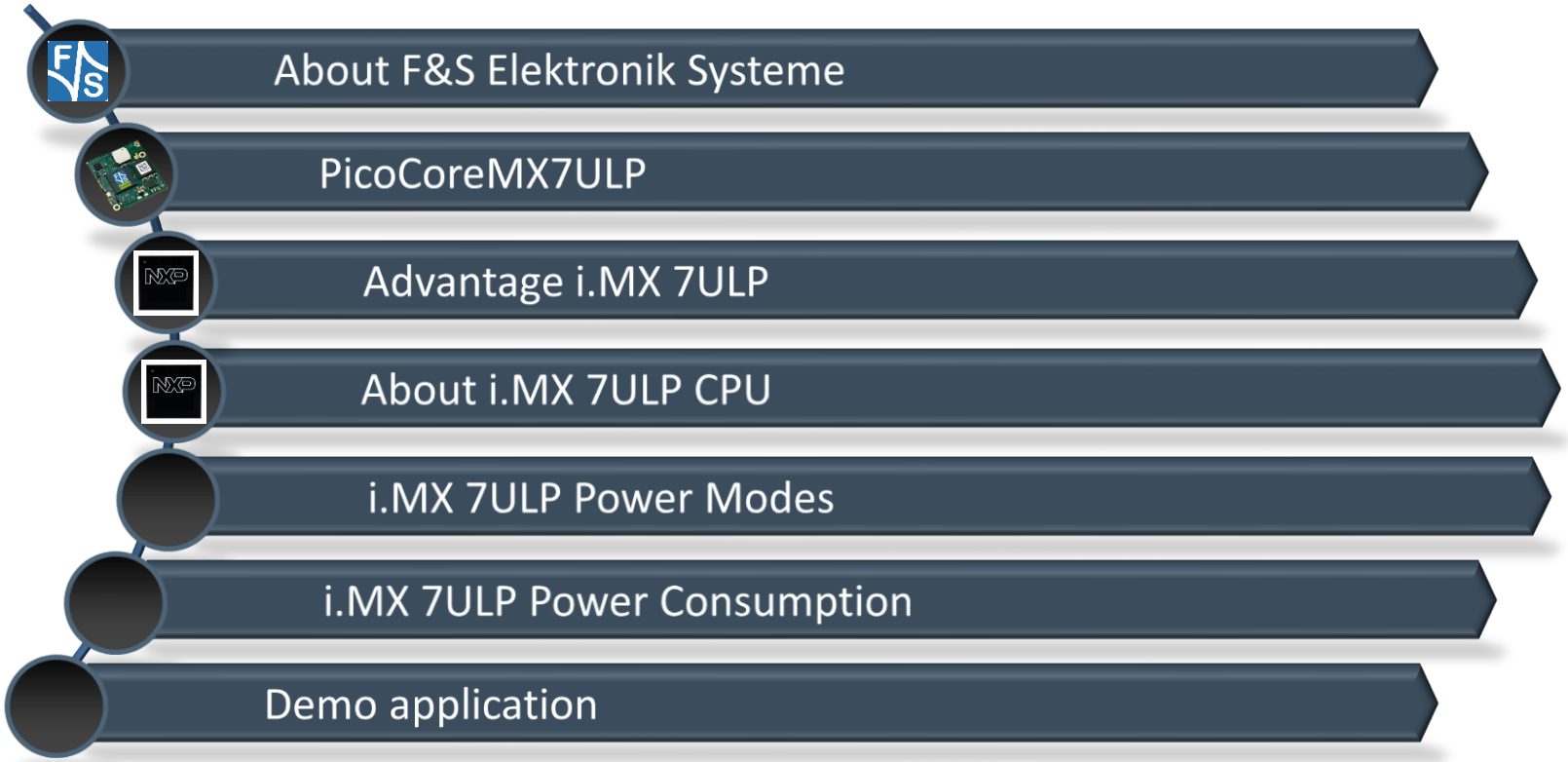
- Fast Evaluation, Implementation and Launch

The Embedded Solution Company

Power saving on portable devices with i.MX 7ULP

F & S Elektronik Systeme GmbH | Untere Waldplätze 23, D-70569 Stuttgart | T +49-711 123722-0 | F +49-711 123722-99 | http://www.fs-net.de

Agenda



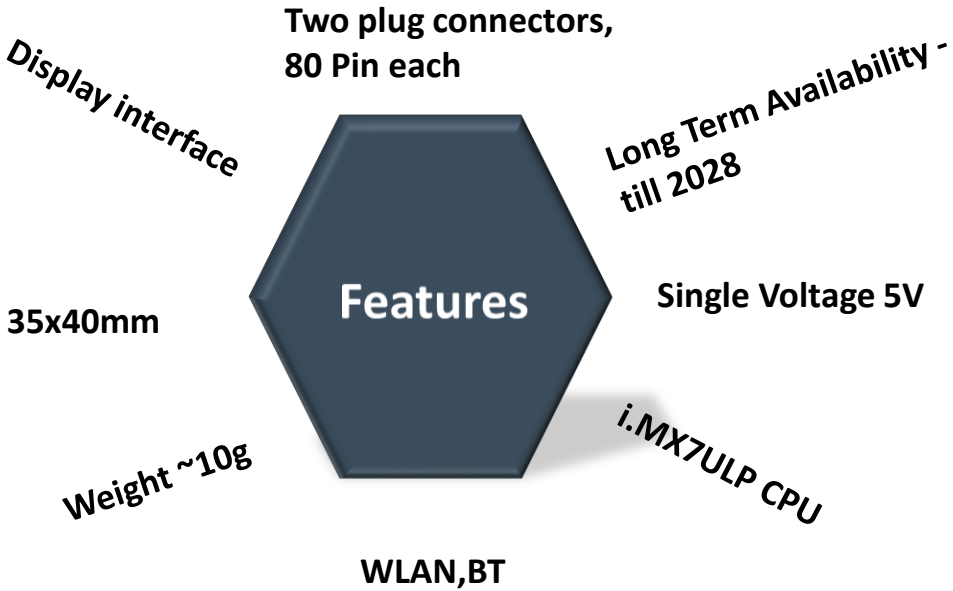
About F&S Elektronik Systeme

- Founded in 1992 as Design Office
- F&S GmbH in 1996
- Privately Held Company
- Entirely Dept Free (no bank loans)
- Hardware Development – Software Development – Production
- Application field – Industrial – Medical – IOT - Other

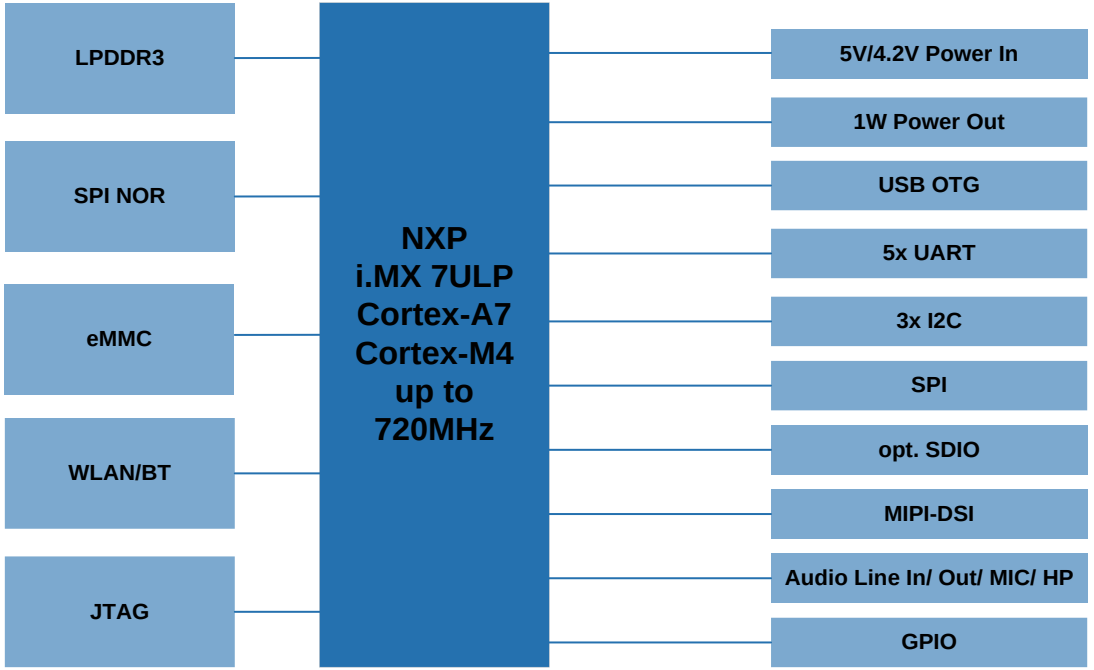
About F&S Elektronik Systeme

- **Different product families**
  - Modules in different form factor platforms with different CPUs
  - Single board computer (pITX) with different CPUs
- **Custom boards**
- **SW in linux (Buildroot/Yocto) and windows (wince6/7, compact 13) available**

PicoCoreMX7ULP



PicoCoreMX7ULP



About PicoCoreMX7ULP

CPU Overview

- CPU: NXP i.MX 7ULP
- Core: ARM Cortex-A7 + Cortex-M4
- Frequency: max. 720 MHz
- L2-Cache: 256 KB
- GPU: 2D, 3D

Operating System

- Buildroot / Yocto (uboot installed)
- Real Time FreeRTOS

Memory

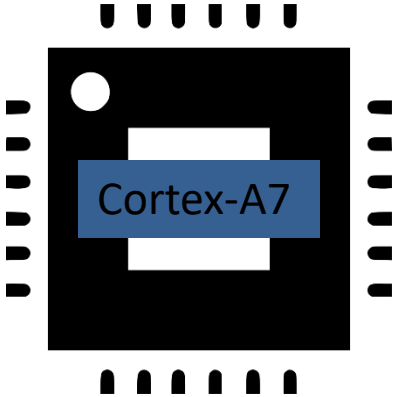
- Flash: max. 64 MB QSPI, max. 32GB eMMC
- RAM: max. 1GB LPDDR3

About PicoCoreMX7ULP

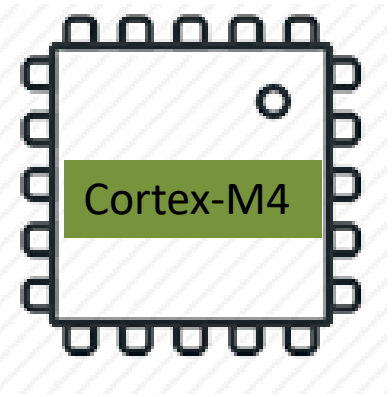
Common

-	Supply Voltage	+5VDC/ ±5% / 4.2V Battery
-	Power Consumption	TBD
-	Operating Temperature	0°C - +70°C, opt. -20°C - +85°C
-	Size	35x40mm (LxB)
-	Weight	~10g
-	Long Term Availability	2028

About i.MX 7ULP

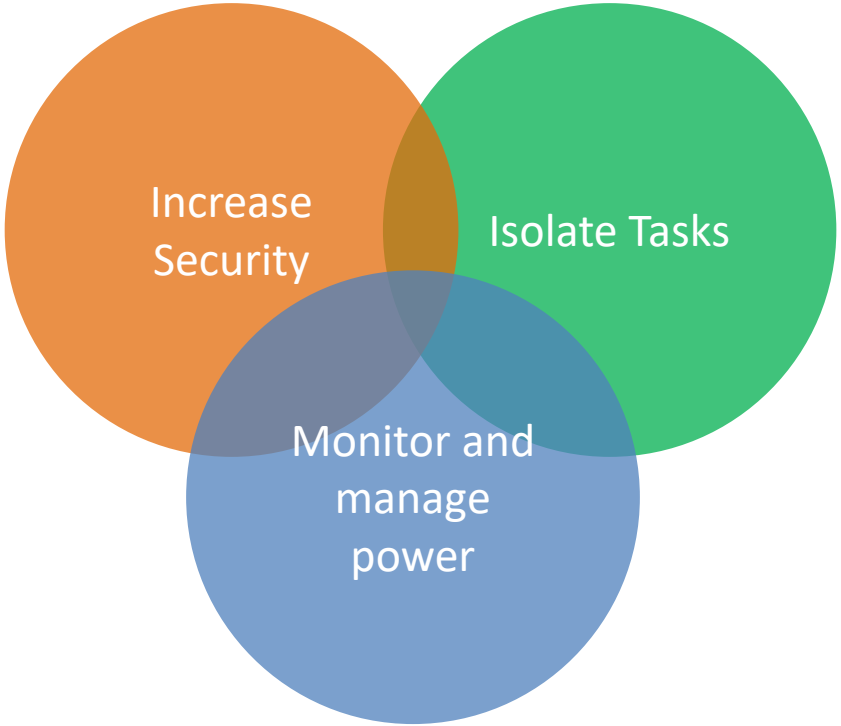


- Performance Core
- Rich OS support



- Real Time Performance
- Extreme Low Power Modes

Advantage i.MX 7ULP

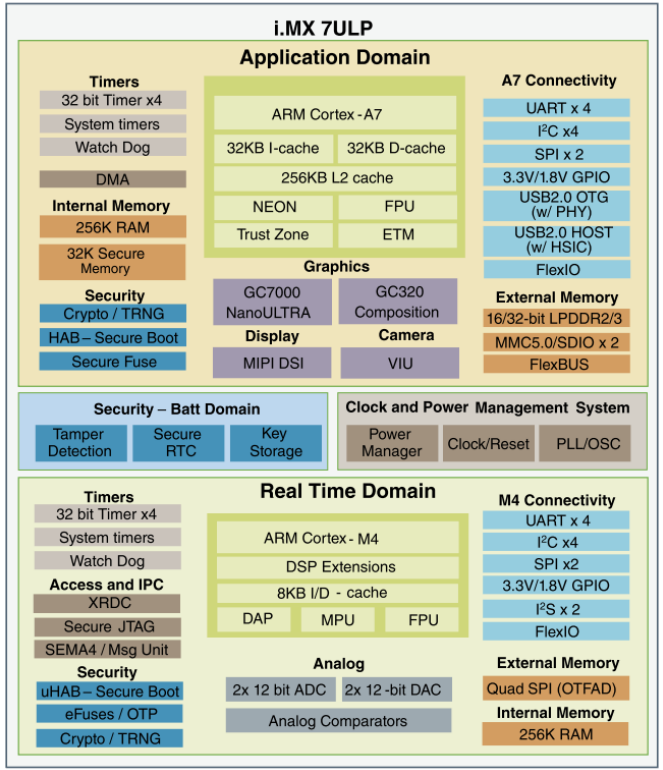


Portable devices

- Bicycle Speedometer
- Wearables
- Drones
- Home control

About i.MX 7ULP - Overview

- Two separate domains
  - Application Domain
  - Real Time Domain
- Both domains can access Clock and Power Management System
- Interfaces are specific each domain



About i.MX 7ULP CPU – What´s new on i.MX 7ULP?

- **Differently from all other heterogeneous platforms of the i.MX family**
  - Possible to swap primary/auxiliary roles of Cortex-A and Cortex-M
  - Support up to 3 boot modes:
    - Dual Boot
    - Low Power
    - Single Boot

Boot Modes

Single Boot

A7 is the primary core, M4 is the auxiliary core. A7 loads from eMMC/SD and boots M4, default mode.

Dual Boot

M4 is the primary core, A7 is auxiliary core. M4 loads from QSPI and boots A7 from eMMC/SD.

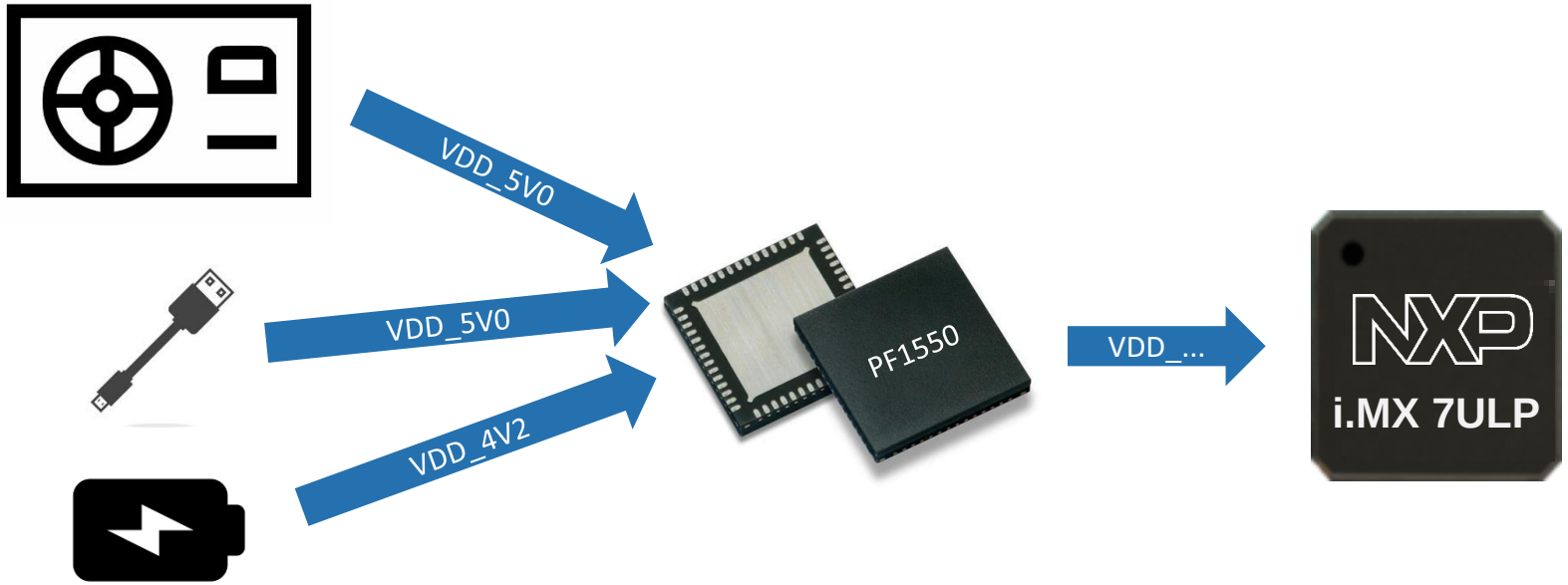
Low Power Boot

M4 is the primary core, A7 is the auxiliary core. M4 Loads from QSPI and boots A7 on demand.

About i.MX 7ULP - Advantages

- Extreme Low Power Modes
- Ability to shut down the most amount of silicon while operating from the Cortex-M4
- PMIC PF1550 specifically designed for i.MX 7ULP
- Separate Power Rails for A7 and M4
- M4 acts as master, controlling all power modes

About i.MX 7ULP – PMIC PF1550

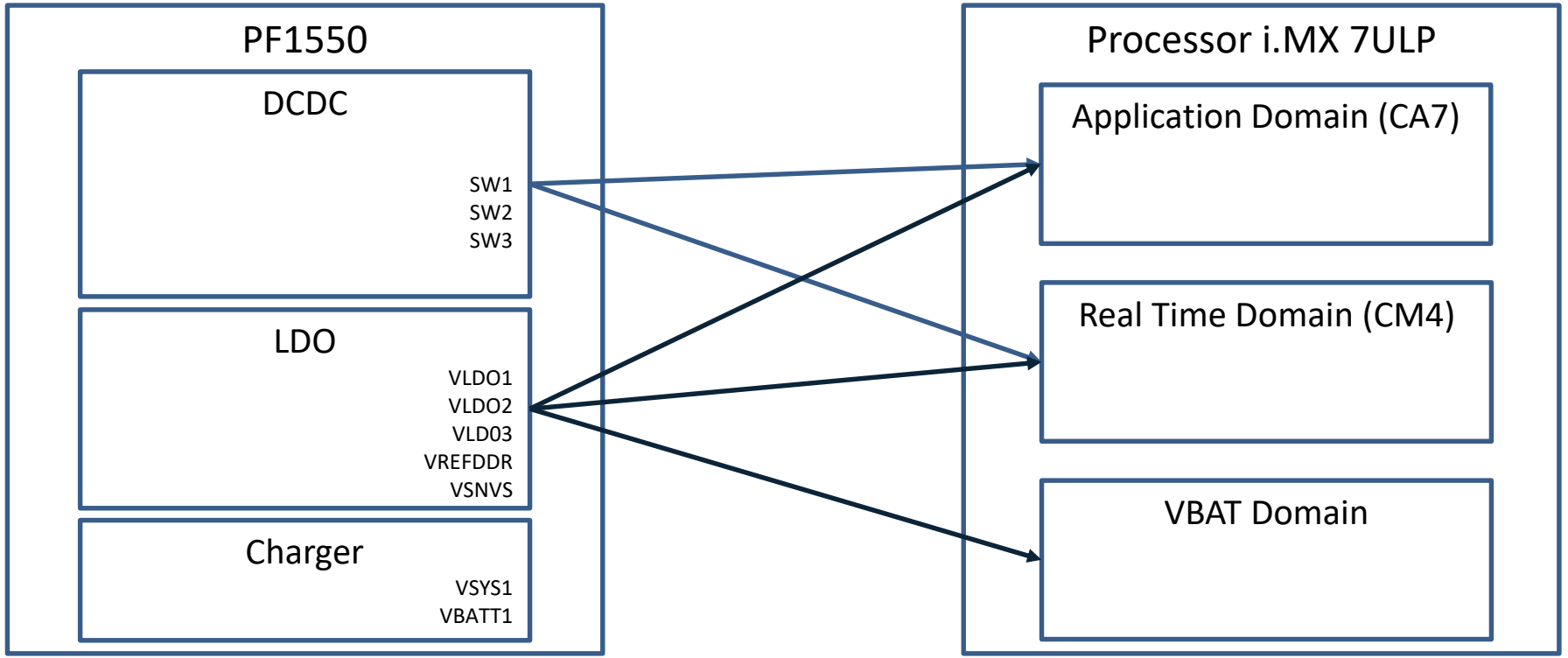


Supply voltage

PMIC PF1550

i.MX 7ULP CPU

About i.MX 7ULP – PMIC PF1550



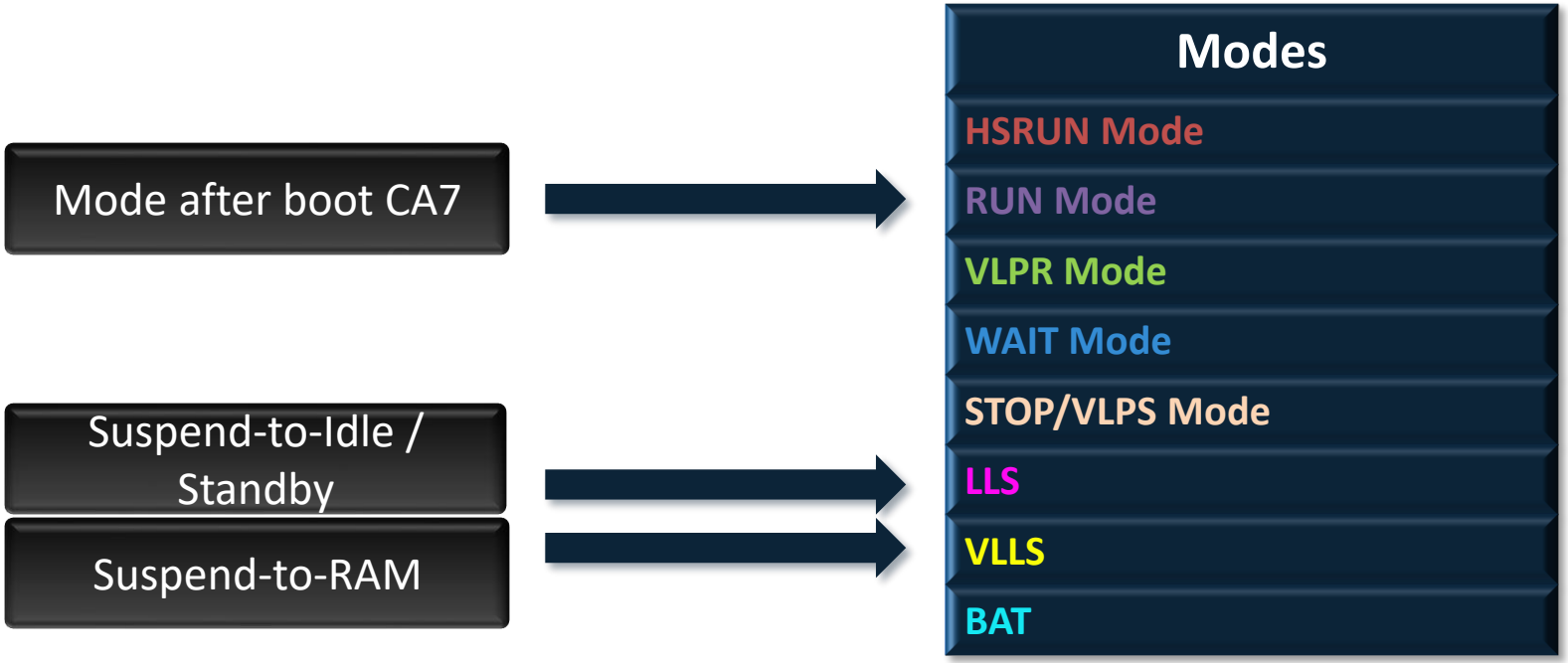
i.MX 7ULP Power Modes

- two completely separate main power domains
- Either domain can be completely shut off by removing external voltage or by turning off the internal voltage supply
- Several low power techniques are implemented on this device to enable power efficient applications

Low power techniques

- Multiple power domains and low power modes allow flexible power optimization for power-conscious applications
- Voltage and frequency scaling in dynamic operating modes
- Software-controlled clock gating for cores and peripherals
- Efficient on-chip LDO regulators and power management control

A7 Domain Power



M4 Domain Power

Modes	description	Recovery Method	Recovery Time
HSRUN Mode	• All logic is functional in this mode • Bus clock and peripherlas functional • Allows FBB (optional) • Allows Dynamic Voltage Scaling (DVS) • CM4/Platform/Bus Clock/Bus Clock (slow): 160/160/80/22.8 MHz	N/A	N/A
RUN Mode	• All logic is functional in this mode • Bus clock and peripherlas functional • FBB/RBB not allowed. • Allows Dynamic Voltage Scaling (DVS) • CM4/Platform/Bus Clock/Bus Clock (slow): 123/123/61.5/24.6 MHz	N/A	N/A

M4 Domain Power

Modes	description	Recovery Method	Recovery Time
VLPR Mode	• All logic is functional in this mode. • Max Frequency restricted to FIRC (48 MHz). PLL disabled. • Allows RBB (Optional) • Allows to disable LVD/HVD(optional)	N/A	N/A
WAIT Mode	• Allows Peripherals to function while keeping core in sleep (clock-gated). • M4 processor in WFI state	Interrupt/Reset	0 ns
STOP/VLPS Mode	• i.MX 7ULP is in static state with all registers retained with maintaining LVD protection. • Peripheral optionally operational in STOP mode • RBB only allowed in VLPS mode.	Interrupt/Reset	4 µs (STOP) and 11.5 µs (VLPS with RBB)/9 µs (VLPS without RBB)

M4 Domain Power

Modes	description	Recovery Method	Recovery Time
STOP/VLPS Mode	• FIRC enabled in VLPS mode via SCG0_FIRCCSR register. • LVDs could be turned off in VLPS mode.	Interrupt/Reset	4 µs (STOP) and 11.5 µs (VLPS with RBB)/9 µs (VLPS without RBB)
LLS	• Static mode with no active transition. • CM4 in WFI mode with core clock gated • RBB allowed	Interrupt/Reset	62 µs (LLS with RBB)/58 µs (LLS without RBB)
VLLS	• M4 Core supply OFF with majority of the logic power gated. • AWIC detects wake-up sources for M4 (via LLWU) • Selectaable Memory retention (32K/64K/256K)	Wake-up Interrupt/Reset	375 µs

M4 Domain Power

Modes	description	Recovery Method	Recovery Time
VLLS	• ADC, Comparators, LP Timers Optionally functional • RBB allowed (Optional) • DGO (aka Always ON) Logic Active	Wake-up Interrupt/Reset	375 µs

Cortex-A7 System Power Management Sleep States

- Suspend-To-Idle
  - ➢ echo freeze > /sys/power/state
- Standby / Power-On Suspend
  - ➢ echo standby > /sys/power/state
- Suspend-to-RAM
  - ➢ echo mem > /sys/power/state

Suspend-To-Idle

- Pure software, light-weight, system sleep state
- Allows more energy to be saved relative to runtime idle by freezing user space
- Putting all I/O devices into low-power states
- Processors can spend more time in their idle states
- It is always supported

Suspend-To-Idle

Cortex-A7

```
# echo freeze > /sys/power/state
PM: Syncing filesystems ... done.
Freezing user space processes ... (elapsed 0.037 seconds) done.
Freezing remaining freezable tasks ... (elapsed 0.001 seconds) done.
Suspending console(s) (use no_console_suspend to debug)
```

Cortex-M4

```
###################  Power Mode Switch Task ###################

    Build Time: May 21 2019--15:26:09
    Core Clock: 115200000Hz
    Power mode: RUN

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  H for enter: LLS      - Low Leakage Stop mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  Q for query CA7 core power status.
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..

CA7 in VLPS status, do not power off regulator!
```

Suspend-To-Idle

Cortex-A7

```
# echo freeze > /sys/power/state
PM: Syncing filesystems ... done.
Freezing user space processes ... (elapsed 0.037 seconds) done.
Freezing remaining freezable tasks ... (elapsed 0.001 seconds) done.
Suspending console(s) (use no_console_suspend to debug)
PM: suspend of devices complete after 57.636 msecs
PM: suspend devices took 0.060 seconds
PM: late suspend of devices complete after 1.446 msecs
PM: noirq suspend of devices complete after 1.361 msecs
PM: noirq resume of devices complete after 0.626 msecs
PM: early resume of devices complete after 0.824 msecs
PM: resume of devices complete after 61.530 msecs
PM: resume devices took 0.070 seconds
Restarting tasks ... done.
#
```

Cortex-M4

```
CA7 not in VLLS status, wakeup directly!

Next loop

##################  Power Mode Switch Task ##################

    Build Time: May 21 2019--15:26:09
    Core Clock: 115200000Hz
    Power mode: RUN

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  H for enter: LLS      - Low Leakage Stop mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  Q for query CA7 core power status.
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..
```

Standby / Power-On Suspend

- This state, if supported, offers moderate, though real, power savings, while providing a relatively low-latency transition back to a working system
- No operating state is lost, system easily starts up again where it left off
- freezing user space and putting all I/O devices into low-power states like Suspend-To-Idle

Standby / Power-On Suspend

Cortex-A7

```
# echo standby > /sys/PM: Syncing filesystems ... power/stadone.
te
Freezing user space processes ... (elapsed 0.041 seconds) done.
Freezing remaining freezable tasks ... (elapsed 0.001 seconds) done.
Suspending console(s) (use no_console_suspend to debug)
```

Cortex-M4

```
###################  Power Mode Switch Task ###################

    Build Time: May 21 2019--15:26:09
    Core Clock: 115200000Hz
    Power mode: RUN

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  H for enter: LLS      - Low Leakage Stop mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  Q for query CA7 core power status.
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..

CA7 in VLPS status, do not power off regulator!
```

Standby / Power-On Suspend

Cortex-A7

```
# echo standby > /sys/power/state
PM: Syncing filesystems ... done.
Freezing user space processes ... (elapsed 0.005 seconds) done.
Freezing remaining freezable tasks ... (elapsed 0.001 seconds) done.
Suspending console(s) (use no_console_suspend to debug)
PM: suspend of devices complete after 23.651 msecs
PM: suspend devices took 0.030 seconds
PM: late suspend of devices complete after 1.422 msecs
PM: noirq suspend of devices complete after 1.299 msecs
Disabling non-boot CPUs ...
PM: noirq resume of devices complete after 0.685 msecs
PM: early resume of devices complete after 0.912 msecs
Suspended for 3.059 seconds
PM: resume of devices complete after 65.819 msecs
PM: resume devices took 0.070 seconds
Restarting tasks ... done.
```

Cortex-M4

```
CA7 not in VLLS status, wakeup directly!

Next loop

####################  Power Mode Switch Task ####################

    Build Time: May 21 2019--15:26:09
    Core Clock: 115200000Hz
    Power mode: RUN

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  H for enter: LLS      - Low Leakage Stop mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  Q for query CA7 core power status.
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..
```

Suspend-to-RAM

- Significant energy savings
- Same steps like Standby/Power-On-Suspend
- RAM in self-refresh
- Buses lose power
- Wake up only by CM4

Suspend-to-RAM

Cortex-A7

```
# echo mem > /sys/power/state
PM: Syncing filesystems ... done.
Freezing user space processes ... (elapsed 0.040 seconds) done.
Freezing remaining freezable tasks ... (elapsed 0.001 seconds) done.
Suspending console(s) (use no_console_suspend to debug)
```

Cortex-M4

```
###################  Power Mode Switch Task ###################

    Build Time: May 21 2019--15:26:09
    Core Clock: 115200000Hz
    Power mode: RUN

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  H for enter: LLS      - Low Leakage Stop mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  Q for query CA7 core power status.
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..

CA7 in VLLS status, power off unused regulator!
```

Suspend-to-RAM

Cortex-A7

```
# echo mem > /sys/power/state
PM: Syncing filesystems ... done.
Freezing user space processes ... (elapsed 0.040 seconds) done.
Freezing remaining freezable tasks ... (elapsed 0.001 seconds) done.
Suspending console(s) (use no_console_suspend to debug)
PM: suspend of devices complete after 54.894 msecs
PM: suspend devices took 0.060 seconds
PM: late suspend of devices complete after 1.448 msecs
PM: noirq suspend of devices complete after 1.379 msecs
Disabling non-boot CPUs ...
PM: noirq resume of devices complete after 0.842 msecs
PM: early resume of devices complete after 0.925 msecs
ci_hdrc ci_hdrc.0: EHCI Host Controller
ci_hdrc ci_hdrc.0: new USB bus registered, assigned bus number 1
Suspended for 58.284 seconds
PM: resume of devices complete after 89.294 msecs
PM: resume devices took 0.090 seconds
ci_hdrc ci_hdrc.0: USB 2.0 started, EHCI 1.00
hub 1-0:1.0: USB hub found
hub 1-0:1.0: 1 port detected
Restarting tasks ... done.
#
```

Cortex-M4

```
CA7 in VLLS status, power on it and wakeup!

Next loop

####################  Power Mode Switch Task ####################

    Build Time: May 21 2019--15:26:09
    Core Clock: 115200000Hz
    Power mode: RUN

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  H for enter: LLS      - Low Leakage Stop mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  Q for query CA7 core power status.
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..
```

Power States – Cortex-M4

Cortex-M4

MCUXpresso SDK

example

power_mode_switch.img

```
Task 1 is working now

MCU wakeup source 0x6...

###################  Power Mode Switch Task ###################

    Build Time: May 21 2019--15:26:09
    Core Clock: 115200000Hz
    Power mode: RUN

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  H for enter: LLS      - Low Leakage Stop mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  Q for query CA7 core power status.
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..
```

Power States

Switching to Very Low Power Run mode by pressing „D“

- **Cortex-M4@16 MHz**

```
WorkingTask 1: Transfer from RUN to VLPR
== Power switch OK ==

Next loop

###################  Power Mode Switch Task ##################

    Build Time: May 21 2019 -15:26:09
    Core Clock: 16000000Hz
    Power Mode: VLPR

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  H for enter: LLS      - Low Leakage Stop mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  Q for query CA7 core power status.
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..
```

Power States

Switching to Very Low Leakage Stop Mode by pressing „I“

```
WorkingTask 1: Transfer from RUN to VLLS
Select the wake up source:
Press T for LPTMR - Low Power Timer
Press S for switch/button VOL+.

Waiting for key press..

Select the wake up timeout in seconds.
The allowed range is 1s ~ 9s.
Eg. enter 5 to wake up in 5 seconds.

Waiting for input timeout value...

9
Will wakeup in 9 seconds.
== Power switch OK ==
WorkingTask 1: Transfer from VLLS to RUN

Next loop

###################  Power Mode Switch Task ###################

    Build Time: May 21 2019--15:26:09
    Core Clock: 115200000Hz
    Power mode: RUN

Select the desired operation

Press  A for enter: RUN      - Normal RUN mode
Press  B for enter: WAIT     - Wait mode
Press  C for enter: STOP     - Stop mode
Press  D for enter: VLPR     - Very Low Power Run mode
Press  E for enter: VLPW     - Very Low Power Wait mode
Press  F for enter: VLPS     - Very Low Power Stop mode
Press  G for enter: HSRUN    - High Speed RUN mode
Press  I for enter: VLLS     - Very Low Leakage Stop mode
Press  W for wake up CA7 core in VLLS/VLPS.
Press  T for reboot CA7 core.
Press  U for shutdown CA7 core.
Press  V for boot CA7 core.
Press  R for read PF1550 Register.
Press  S for set PF1550 Register.

Waiting for power mode select..
```

Current Consumption PicoCoreMX7ULP

Cortex-M4 → Cortex-A7 ↓	HSRUN	RUN	VLPR	WAIT	VLPW	STOP	VLPS	LLS	VLLS
RUN	-	46,2	-	-	-	-	-	-	-
VLPS (freeze)	48,3	42	25,5	38,8	25,1	34	32	NA	NA
VLPS (Standby)	38,7	32,3	15,9	29,1	15,3	14,7	14,5	NA	NA
VLLS	28,1	25	8,6	21,8	8,2	7,3	3	2,9	2,8

All values are given in mA

Power Consumption i.MX 7ULP vs. PicoCoreMX7ULP

Modes	SoC i.MX 7ULP	PicoCoreMX7ULP
A7 VLLS / M4 VLPR	7,926 mW	36,12 mW
A7 VLLS / M4 RUN	24,117 mW	105 mW

Live Demo

Patrick Jakob

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