P2ETYPEARN_2_5_1
Aug 31, 2009
Rev. 2

PPP to Ethernet Type A Interworking RAM Package Release 2.5.1

General

This release note reflects differences between the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev. 2, and the features which are available for this device using the provided microcode RAM packages. The following release note reveals any exceptions to the features which are specified in this release of the specification. The notes describe any addition to the specification or any missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: MLMC PPP, Ethernet, Interworking, Header Compression, Header Decompression, IP fragmentation, and IP Reassembly. Features of these core blocks that are not supported in this package are described in Table 3.

Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Loader file name (.h)
MPC8360 rev 2.1	iw_pe_type_a_mpc8360_r2.1.h
MPC8568 rev 1.1	iw_pe_type_a_mpc8568_r1.1.h

Package Content

The tables below designate the content of this package. The baseline is the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev. 2. The tables designate additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev. 2, please contact Freescale support. Contact information may be found at www.freescale.com.

Table 2. New Features (Which are not Described in QEIWRM, Rev. 2)

Feature	Comments
DF bit checking while interworking to Ethernet with IP fragmentation	IP frames with DF bit set on IP header and violating the MTU configured on Ethernet Tx will be treated as unrecognized frames and dropped according to interworking rules.

Table 3. Removed Features (Described in QEIWRM, Rev. 2 but Not Supported)

Feature	Comments	QEIWRM, Rev. 2
Header manipulation in termination mode Insert/remove/replace VLAN	REMODER[VTagOP] and REMODER[VNonTagOP] (in RxGPRAM) are not supported.	Section 8.5.3.8, “Rx Ethernet Mode Register (REMODER)”
	TAD[VTagOP] and TAD[VNonTagOP] are not supported.	Section 8.6.2.6.5, “Termination Action Descriptor (TAD)”
LPM PCD		Section 29.3.2.4, “Longest Prefix Match (LPM) PCD”
Expanded Hash Table		Section 29.5.3.3.1, “TableLookup_FourWayHash PCD”
VLAN Specific Header Manipulation Command Descriptor		Section 30.1.10.2, “VLAN Specific Header Manipulation Command Descriptor”
PPP Mux		Section 24.9 PPP Mux Process
CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes		Section 29.5.3.1.1, “CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes”
IP Reassembly		Chapter 32 “IP Reassembly”

Table 3. Removed Features (Described in QEIWRM, Rev. 2 but Not Supported)

Feature	Comments	QEIWRM, Rev. 2
PPP Precise WFQ		Section 24.15, “Precise WFQ Table”
MLMC PPP Class 0 WFQ	MLMC PPP Class 0 WFQ is not supported.	Section 24.4.2.2, "Transmission of ML/MC PPP"
IPHCoE		Chapter 30, “Protocol Interworking Programming Model” and Chapter 33, “IPv4/UDP Header Compression”
PPP to Ethernet HES	PPP cannot interwork to an Ethernet transmitter that uses hierarchical scheduling.	Section 8.4.17, “Hierarchical Scheduling Support”

Revision History

Table 4. Revision History for Release 2.5.1

Release Date: Jun 9, 2009 Revision Register Number: 0xBBE0A251	
New Features	This package contains performance optimizations for ML/MC PPP Tx Back-End process.
Removed Features	None.
Bug Fixes	PPP and Ethernet cannot enqueue to the same queue.
	ML/MC PPP, for links under bundle configured in interworking mode, short fragments with 24 bit sequence numbers are not handled correctly.
	ML/MC PPP, packets can be lost in ML/MC receive process due to synchronization issue between front-end and back-end tasks.

Table 5. Revision History for Release 2.5.0

Release 2.5.0 Revision Register Number 0xBBE0A250	
New Features	ML/MC PPP, Flush WBD Command for flushing the WBD for a given class. This command can be used when the host is interested in limiting the time spent by the fragments the WBD ring.
	Improved support for ML/MC PPP null fragments: reception of a null fragment now will not assert a fragment loss event; null fragments received for each class are counted.
Bug Fixes	ML/MC PPP, FBP-RLI indication is not always correct.
	IPHC, IP Header Compression MIN_WRAP error mechanism does not work correctly.

Table 6. Revision History for Release 2.4.0

Release 2.4.0 Revision Register 0xBBE0A240	
New Features	This package introduces enhancements for PPP Tx bandwidth use optimization.
	The number of PPP IW CPU queues were increased from four to eight.
	New counter on IP Decompressor Statistics table - “Total bytes in error frames.” Counts the total bytes in frames that are not decompressed due to errors.
	New counter on IW Special Statistics table (IWCS) - “DQ_DroppedByte_Cnt.” Counts the total bytes in frames that are dropped due to reasons related to IW destination queue.

Table 6. Revision History for Release 2.4.0

Release 2.4.0 Revision Register 0xBBE0A240	
Bug Fixes	Race condition on class interrupt queue can cause some interrupt entries to be lost.
	Using aging for external hash tables might introduce an SDMA error exception.
	MLMC PPP transmits illegal HDLC frames when ACFC enabled and PID in buffer. In such a case illegal data is being transmitted.
	When issuing a host command "Add/Remove Entry in CAM Emulation Lookup Table" (See section 30.6.1.2, “Add/Remove Entry in CAM Emulation Lookup Table" in the QEIWRM, Rev. 1) with ADDE equal to 00 (table lookup, no change in the table), the LookupTableOffset value might be invalid even though the V bit (valid LookupTableOffset) is asserted (see Figure 30-42, “Set Entry in CAM Emulation Lookup Table Command Parameters" in the QEIWRM, Rev. 1.) In case the V bit is asserted, the user should read the first byte of the Action Descriptor (AD) which is pointed to by the LookupTableOffset and verify that the V (valid) bit on the AD is asserted. In case the V (valid) bit on the AD is negated, the table lookup result should be considered as invalid.
	A frame with packet length of 1518 bytes is not counted by EtherStatsPkts1024 counter. This counter should count all frames with a length that is between 1024 and 1518 octets in length inclusive (excluding framing bits but including FCS octets). Therefore the EtherStatsPkts1024 counter is not compatible with RFC2819.

Table 7. Revision History for Release 2.3.1

Release 2.3.1	
New Features	Interworking to Ethernet with IP fragmentation— IP frames with DF bit set on IP header and violating the MTU configured on Ethernet Tx will be treated as unrecognized frames and dropped according to interworking rules.
Bug Fixes	In the 1588V2, the Timestamp is presented in little-endian instead of big endian.
	ML/MC PPP receiver has a synchronization flaw between the front-end and back-end processes that can cause the loss of received ML fragments.
	When working in Fast Ethernet Half Duplex and a collision error occurs the port might halt.
	In an Ethernet Rx in heavy traffic load (when smoother is disabled) or in the case of an errored frame (CRC, IP Check Sum etc..) and the frame size is less the 128 bytes, unexpected behavior may occur.
	In case of IW error interrupt (Ethernet Rx) the attribute status may be faulty.
	Using IP reassembly where a case of Dynamic LookUp Table busy condition occurs the IPR may hang.
	In a heavily loaded system with IP reassembly the IPR may hang.
	Ethernet receiver can cause unpredictable memory corruption while discarding illegal short frames.
	Working with customize preamble is not supported for frames smaller then 64 bytes.
	In Dynamic Lookup table PCD busy flow, the microcode will not reload 2 registers after task switch. Wrong handling of busy event may eventually cause IPR to hang.

Table 7. Revision History for Release 2.3.1 (continued)

Release 2.3.1	
Bug Fixes	In IPR function, Free queue pool In pointer can be handled by a few IPR threads and Automatic learning PCD at the same time without MURAM semaphore mechanism. This might cause IPR queues to disappear from the pool due to no synchronization in returning the queues.
	When working with Header Compression with more then one compressor and one of the compressors is disabled, the disabled compressor may change the order of other threads without checking in curSNUM=mySNUM, and the compressors may stick.

Table 8. Revision History for Release 2.3.0

Release 2.3.0	
New Features	Code which supports IEEE Std. 1588™ Version 2 was added to the package. Refer to the IEEE Std.1588 V2 section in the Ethernet specification.
Bug Fixes	When HES and IPF modes are enabled, and the frame sizes are larger than MTU (frame is fragmented), one or more TX queues may stop transmit and recover only when frames less than MTU are sent.
	In the Customize Preamble mode, the Preamble is not transferred to the CPU for short frames.
	In PPP to Ethernet interworking, working with extended TQD is prohibited.
	In the system, Ethernet and PPP receivers use the interworking function to forward incoming traffic to the same Ethernet transmitter port. The destination SQQD cannot be shared. This means frames from Ethernet and PPP receivers cannot have the same IWAD[TQD Index] value.
	A bug that caused the compressor to use unknown RTSR register for the compression time-out mechanism.
	When working with Ethernet the LossLess flow control feature can be enabled by mistake and the transmitter may send a flow control frame.
	Data memory corruption can occur for Ethernet to Virtual Port IW in case Virtual Port decides not to forward some frames to next IW stage.
	Copy to CPU function used by ENET Rx and Virtual Port can cause these two to halt, if a busy condition occurred for a multi-BD frame.
	In PPP, Rx Adaptive Sequence Number Recovery Mechanism may cause SDMA error.
	In PPP Rx the host may read an old data pointer from a LCP BD ring and therefore read wrong data.
	Only for the MPC8568E device, working in PPP MLMC Rx swap mode (no FBP) may not work.
	In case of a busy condition during ENET RX IW copy to CPU the QUICC Engine block might halt
	ML-MC PPP, when working in swap mode (no Free Buffer Pool mode), the RX Queue Descriptors of the classes should be located in the external memory only and the bit RxExtQD in the CMR should be set.

Table 9. Revision History for Release 2.2.1

Release 2.2.1	
New Features	None
Bug Fixes	Usage of IP Insert Header Manipulation Command Descriptor could cause unexpected microcode behavior.

Table 10. Revision History for Release 2.2.0

Release 2.2.0	
New Features	None
Bug Fixes	At the Ethernet Tx the Rate limiter dynamic change might have caused the Ethernet Tx to halt.
	In PPP termination, if the interrupt bit in the TxBD is asserted, it might cause memory corruption.
	When the Ethernet receive is highly loaded with in coming frames it might stop functioning at all. This bug is valid only if the next two conditions take place: 1. More than one thread are enabled. 2. The maximum length of the incoming frames is longer than 4*(VFIFO block size). (VFIFO block size = 128 up to 248). QENET22

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Table 11. Revision History for Release 2.2.0

Release 2.2.0	
New Features	ML PPP - Adaptive Sequence Number Mechanism. This feature allows the microcode to synchronize on ML traffic in case of a temporary outage on the lines. In case of successful synchronization a special interrupt will be issued. This interrupt can be disabled by setting BMR[DisAdSeqInt] on BPT.
	ML PPP - Fragment Loss and Fragment Loss due to Threshold interrupts can be disabled by setting BMR[DisFLInt] on BPT.
Bug Fixes	None

Table 12. Revision History for Release 2.1.4

Release 2.1.4	
New Features	None
Bug Fixes	When the Ethernet receive is highly loaded with in coming frames it might stop functioning at all. This bug is valid only if the next two conditions take place: 1. More than one thread are enabled. 2. The maximum length of the incoming frames is longer than 4*(VFIFO block size). (VFIFO block size = 128 up to 248).
	When using Init_MUX/Init_DeMUX host command it might corrupt the page of another thread.

Table 13. Revision History for Release 2.1.3

Release 2.1.3	
New Features	Ethernet Hierarchical schedule (HES) work conserving mode. Programming model will be released in the next specification document.
	New bit was added in LMR register called RxMLDis which is located at position 4. If set, all frames which contain MLMC PPP PID will be dropped and the ILLEGAL FRAME counter under this link will be incremented.

Table 13. Revision History for Release 2.1.3 (continued)

Release 2.1.3	
Bug Fixes	MLMC frame received with length =< 8 Bytes with ACC Error, may result in illegal DMA (Bus Error).
	MLMC frame received with length=< (expected header size + FCS) results in illegal DMA (Bus Error).
	MLMC frame with header = 9 Bytes results in unexpected behavior.
	MLMC frame received with length =< 8 Bytes after long frame may result in losing the long frame.
	When FBPBusy, PRTBusy, or Fragment loss conditions occur, the rest of the MLMC frames for that class will never be enqueued to the PRT.
	In interworking mode, when a plain or MLMC PPP frame arrives and is discarded (due to some error condition or busy condition), the data pointer for the next Plain/MLMC frame is not correct (it is incremented in 0x80 bytes for each consecutive error). This results in an error at the next received frame.
	In interworking mode, the IW Error Interrupt in register IWEMODER has to be masked. {IWEMODER[26]==0}
	Copy2CPU option is not allowed, it might cause a halt of the system.
	For frames which belong to IPR flow, the Total byte counter in IW statistics will count only IP packet bytes instead of total length of the frame.
	For regular frames which belong to IPR flow, In case of IWAD [FwE] =0 and IWMODER [FwAllCPU] =1, the frames may end in Enet CPU queue instead of IPRQ0.

Table 14. Revision History for Release 2.1.2

Release 2.1.2	
New Features	None
Bug Fixes	PPP Receiver. Frames received with length = 3Bytes are treated as normal frames instead of 2Short frames (silently discarded).
	PPP Receiver. Frames received with length >8 bytes may lose 1 last byte.
	PPP Receiver. LCP pointer may be duplicated in FBP Busy condition, FragLoss condition.

Table 15. Revision History for Release 2.1.1

Release 2.1.1	
New Features	None

Table 15. Revision History for Release 2.1.1

Release 2.1.1	
Bug Fixes	In case of usage of header compression interworking (E2PPP), if an enqueue busy occurred, the whole QUICC Engine block might get into a deadlock status
	In case of a reassembled frame (IP reassembly) which is directed both to an interworking queue and is forwarded to CPU, a data corruption will occur.
	When using hierarchical scheduling with a SQQDs smaller the 64 byte, the Buffer Descriptor base of each queue should be allocated in the address range of: 0x0 to 0x7FFF_FFFF.
	In interworking mode frames which are larger then MAXD1 should be discarded. Actually frames where discarded only when their length was larger then Rounded_MAXD1. Note: Rounded_MAXD1=CEIL(MAXD1/MRBLR)*MRBLR.
	When using HES adding a New LPs (Logic Port) may cause old LPs to stop working for a short while to a complete stop.
	In a heavily loaded system ETH queues which are fragmented may stop transmitting.

Table 16. Revision History for Release 2.1.0

Release 2.1.0	
New Features	IP reassembly can now support reassembly of up to two out-of-order received fragments. More details about this new feature can be found in the IP reassembly specification.
	PPP Rx, which operates in interworking mode, now supports IP reassembly.
	The maximum number of MUX Tx queues in ML PPP was increased to 32. In addition, a multi-threading mechanism was introduced for PPP MUX operation.
	A mechanism was added in PPP MUX programming model that allows performing a graceful stop of the MUX operation.
Bug Fixes	BMR is undefined in case of DMA semaphore reject for IWF statistics {IWCS}.
	The following Ethernet scheduler's wrong functionality has been fixed: 1. Long response time for rate limiter changes. 2. Scheduler inaccuracy of up to 6% for different frame lengths and band width rates.

Table 17. Revision History for Release 2.0.0

Release 2.0.0	
New Features	Ethernet transmitter hierarchical scheduler. See Section 8.4.17, “Hierarchical Scheduling Support,” in the QEIWRM, Rev. 1.
	Added four PPP receive queues for quality of service. See Section 29.1.1.3 “Interworking CPU Queue Descriptor (IW_PPP_CPU_QD)” in the QEIWRM, Rev. 1.
	Weighted Random Early Detection (WRED) Queue Management on ETH to PPP. See Section 29.1.4.5, “ML/MC PPP Interworking Transmit Queue Descriptor Extension” in the QEIWRM, Rev. 1.
	Removed Tx VFIFO Block Size field in Section 8.8.1, “Init Tx, Init Rx and InitTx and Rx Parameters Command” of the QEIWRM, Rev. 1.
	Added 6 new Host commands that re-initialize receive or/and transmit parameters for dynamic changes after first MCC Initialization command was issued. See Table 4-4, “QUICC Engine Command Opcodes” and Table 4-5, “Command Descriptions” in the QEIWRM, Rev. 1.
Bug Fixes	Parser events are not set in IP reassembly flow.
	IP reassembly may not function properly in heavily loaded system.
	When a FBP busy interrupt of the PPP Tx background process occurred there was a wrong restore of a register which caused corruption.
	When handling the last MUX SubFrame the MLPPP TX will generate interrupt with wrong event register value.
	In case of PPP FBP busy condition there might be memory corruption. This condition is possible only when subframe is dropped due to length error or the aging mechanism.
	Bug in mixed mux queue (a mux queue that supports also a none mux frames) of the MLPPP. The new feature which uses Max_SubF_Size does not work properly in the MLPPP.
	In case of IW PPP Mux transmission when a zero size BD occurs the transmitter handled the “skip Bd” instead of the next BD causing data corruption.

Table 18. Revision History for Release 1.1.0

Release 1.1.0	
New Features	VFIFO block size is configurable. VFIFO block size had a fixed value of 128 bytes in previous releases. Three values are allowed now: 128, 192 and 248. Allowing block sizes beyond 128 bytes enhances the performance, in particular for large packets.
	IP fragmentation in Ethernet transmitter.
	ML PPP MUX support for max_sub_frame_len.
	New MCC INIT host commands for re-initialization during runtime.

Table 18. Revision History for Release 1.1.0 (continued)

Release 1.1.0	
Bug fixes	IW Thread PRAM address is not loaded(IW_E_ExtPage) when the frame is dropped due to CPU BUSY condition.
	Possible deadlock in Ethernet to XXX interworking in case of BUSY condition and IWCT Index = 0 (No IWCT).
	Ethernet Address classifier PCD (MC/BC) not working.
	IP reassembly does not work properly when using external lookup table.
	IWCS are incremented for short frames in Ethernet Rx.
	No IREQ was given in ML PPP when FBP Busy when returning buffer in the Fragment process.
	In case IREQ in ML PPP Tx is in 16-bit mode wrong data will be transmitted.
	In some cases when interworking from Ethernet to ML PPP the ML PPP WFQ scheduler in not updated.

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