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Errata to MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual, Rev. 1

This errata describes corrections to the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*, Revision 1, which is the initial version of this reference manual. The MPC8349EA contains an embedded Power Architecture® core. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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NOTE

This document contains errata for the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*, Revision 1. The MPC8349EA device contains MPC8349 Revision 2 silicon and later; for errata pertaining to MPC8349 Revision 1 silicon, see the errata document for the *MPC8349E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*, Revision 1 (Freescale Order ID MPC8349ERMAD).

1.2, 1-3	Update second bullet point for the DDR SDRAM memory controller to say “32- or 64- bit data interface.”
2.3, 2-1	Added the following text to first paragraph: Unless stated otherwise in a particular block, all accesses to and from the memory mapped registers must be made with 32-bit accesses. There is no support for accesses of sizes other than 32 bits.
Chapter 4, Throughout	Update field name LBIUCM to LBCM.

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4.2.2, 4-6	Changed step 13 of power-on reset flow to read as follows: 13. Before the boot sequencer finishes, it can enable the PCI interfaces to accept external requests, if required, by clearing the CFG_LOCK bit in the PCI function configuration register as described in Table 13-41.
4.3.1.3, 4-10	Modified description in second row (CFG_CLKIN_DIV = 1) of Table 4-6, “CLKIN Division,” to read as follows: In PCI agent mode, CLKIN: PCI_SYNC_OUT = 2:1 and the PCI_CLK_OUT[0:7] clocks can be programmed to CLKIN/2 in the OCCR. In PCI agent mode, internal frequency is doubled. Refer to the *MPC8349EA Hardware Specifications* for details.
4.3.2.1, 4-12	In Table 4-8, “Reset Configuration Word Low Bit Settings,” changed last sentence of field description for DDRCM to read as follows: The 2:1 mode is useful mostly with 32-bit data bus width.
4.3.2.2.5, 4-19	In Table 4-16, “TSEC1 Mode Configuration,” add the following sentence to value 10’s meaning: “This value should also be used if MII protocol is required; in this case, the MACCFG2[I/F mode] bits select between an MII or GMII interface.”
4.3.2.2.6, 4-20	In Table 4-17, “TSEC2 Mode Configuration,” add the following sentence to value 10’s meaning: “This value should also be used if MII protocol is required; in this case, the MACCFG2[I/F mode] bits select between an MII or GMII interface.”
4.3.3.1, 4-21	Add the following text to the end of the first paragraph: “+ LCS0 is the default for GPCM, so GPCM controlled is used to read the reset configuration word from EEPROM. /LGTA should be high to avoid unintended early termination of the read cycle.” Add the following two paragraphs after Table 4-22: “For loading the reset configuration word from a local bus EEPROM, the PCI_SYNC_IN/PCI_CLK input clock is divided by 32 to enable operation of slow frequency memories.Figure 4-5 and Figure 4-6 show the timing of EEPROM operation. As the figures indicate, if the HRCW is loaded through the local bus, the LA[27:31] pins are used and not the LAD[27:31] pins. The LAD[27:31] pins are not driven during HRCW loading. Note that in Figure 4-5 and Figure 4-6, only the LA[27:31] are shown incrementing during the load of the HRCW. In essence, the device does a type of burst access to the flash memory when it loads the HRCW. It drives the high-order bits of the address on LAD[0:26], which is also the first address in a 4-byte sequence, asserts LALE, latches the first byte, and then increments LA[27:31] to get the next 3 bytes. It then drives the high-order bits for the second access, asserts LALE, latches a byte, and again increments the LA[27:31] to get the next 3 bytes. Out of reset, the LA[27:31] and LAD[27:31] mirror each other (while LALE is asserted). Note that LCS0 is asserted low during the assertion of $\overline{\text{PORESET}}$ and $\overline{\text{HRESET}}$. Also, $\overline{\text{PORESET}}$ negation to LALE assertion is 36 cycles of PCI_SYNC_IN/PCI_CLK clock signal.”

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4.3.3.1.1, 4-23 Replace figures 4-5 and 4-6 with the following updated figures:

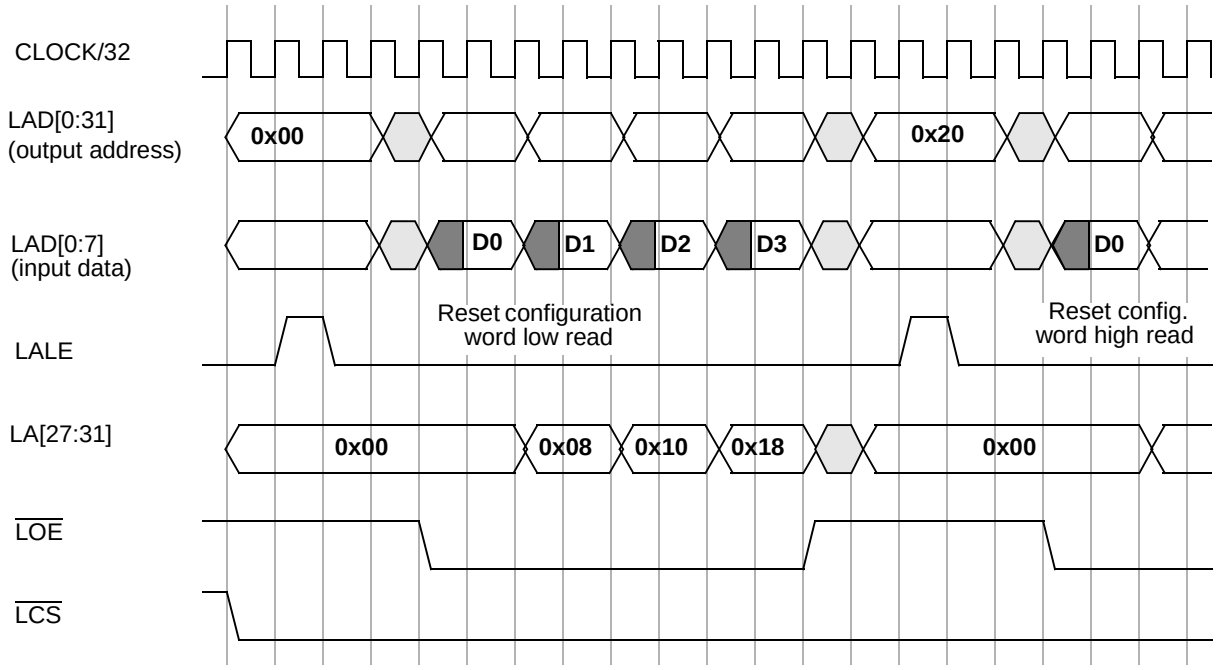

Figure 4-5. Loading Reset Configuration Words from Local Bus

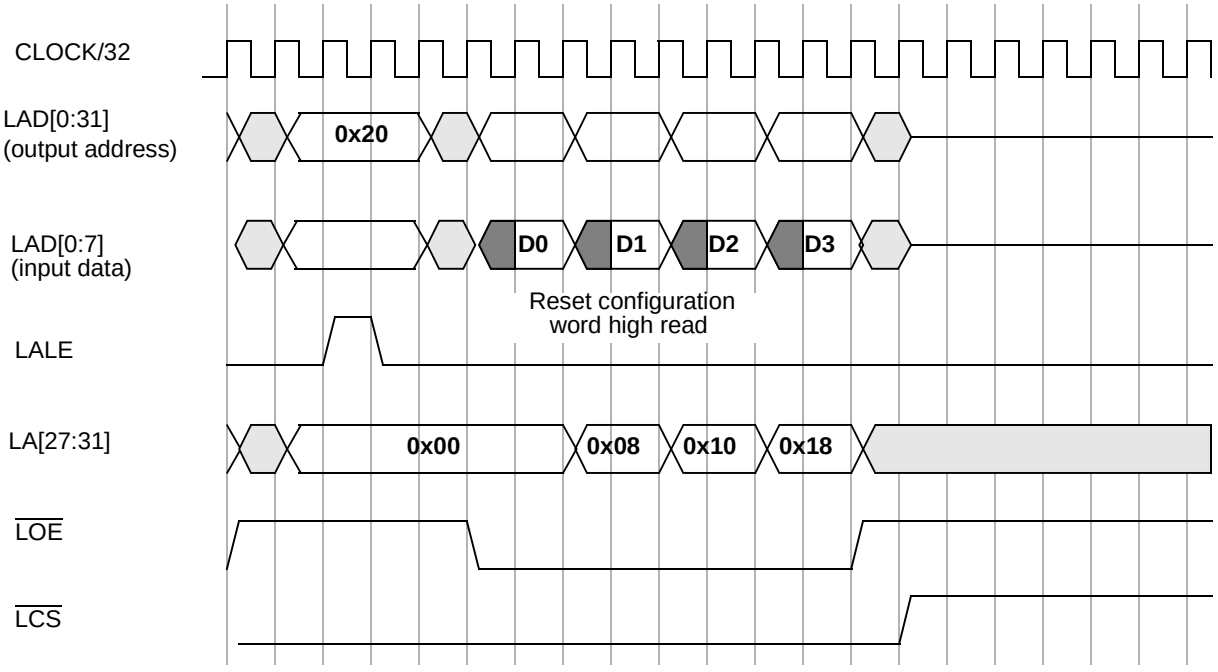

Figure 4-6. Loading Reset Configuration Words from Local Bus (continued)

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4.3.3.2.1, 4-24	Changed note to read as follows: When reset configuration words are loaded from an I^2C EEPROM, an I^2C serial EEPROM of extended addressing type must be used.
4.4.3, 4-31	Removed overbar from CFG_CLKIN_DIV in equations at top of page 4-31. In same section, removed first row (I^2C1) from Table 4-26, “Configurable Clock Units.”
4.5.1.6, 4-36	Change the first sentence to the following: “RCR, shown in Figure 4-14, can be used by software to initiate a hard reset sequence.
4.5.2.3, 4-40	Add the following note to the ENCCM bit field description in Table 4-36, “SCCR Bit Settings”: “**Note**: The encryption core must have the same clock ratio as the USB unit, unless one of them has its clock disabled.” Modify the first line of the ENCCM bit field description to read “Encryption core, JTAG, and I^2C1 clock mode.” Add the following to SCCR[ENCCM] bit field description’s: “01Encryption core clock/csb_clk ratio is 1:1”:
5.3.1, 5-16	In Table 5-20, “System Configuration Register Memory Map,” update SICRL reset value to 0x8000_0000.
5.3.2.4, 5-19	In Table 5-26, “SPCR Bit Settings,” add note to PCIPR as follows: “DMA has the same priority as PCI.”
5.3.2.5, 5-24	Update SICRL bit settings for bits 16 and bit 17 as follows:

16^2	GPIO1_K	GPIO1[10]	$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	—	—
17^2	GPIO1_J	GPIO1[9]	GTM1_TIN4/GTM2_TIN3	—	—

5.3.2.6, 5-24	In the second paragraph, change “A value of 0b11 is illegal for all groups” to “A value of Ob11 selects the GPIO mode of the appropriate pin.”
5.3.2.6, 5-25	In Figure 5-15, “System I/O Configuration Register High,” and Table 5-28, “SICRH Bit Settings”: made bits 30-31 (TSOBI1 and TSOBI2) of SICRH reserved. Removed Table 5-29, “SICRH[30-31] Bit Settings,” on page 5-28.
5.3.2.7.1, 5-28	Update introductory sentence to the following: “The DDR debug configuration enables a DDR memory controller to either debug mode in which the DDR SDRAM source ID field and data valid strobe are driven onto one of two optional sets of pins:”

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5.3.2.8, 5-28 In first two paragraphs, update 18 Ω to 18.2 Ω.

5.3.2.8, 5-30 In Table 5-30, “DDRCDR Field Descriptions,” replaced descriptions of fields DSO_PZ and DSO_NZ as follows:

Table 5-30. DDRCDR Field Descriptions

Bits	Name	Description
2–5	DSO_PZ	DDR driver software p-impedance override 0000 Half strength—Highest Z 1000 Much higher Z than nominal 1100 Higher Z than nominal 1110 Nominal impedance setting 1111 Lower Z than nominal
6–9	DSO_NZ	DDR driver software n-impedance override 0000 Half strength—Highest Z 1000 Much higher Z than nominal 1100 Higher Z than nominal 1110 Nominal impedance setting 1111 Lower Z than nominal

5.3.2.8, 5-30 In Table 5-30, “DDRCDR Field Descriptions,” update the description for the DDR_TYPE row as shown:

13	DDR_TYPE	Selects voltage level for DDR pads 0 DDR2 (1.8V mode) nominal impedance—18 Ω 1 DDR1 (2.5V mode) nominal impedance—18 Ω **Note:** DDR_TYPE must be set according to the logical type of the DDR memory devices, as it effects logic behavior of the DDR controller as well as the physical parameters of the DDR I/O pads.

5.3.2.9, 5-30 In Figure 5-17, “DDR Debug Status Register (DDRDSR),” update access and register bits to be read only.

5.4.5.2, 5-37 Remove the sentence “This is the default value after soft reset” from the first sub-bullet point of the first bullet point.

5.4.5.2, 5-37 Replaced text of second bullet with the following:

- WDT reset/interrupt output mode

  Without software periodic servicing, the software watchdog timer times out and issues a reset or a nonmaskable interrupt (*mcp*), programmed in SWCRR[SWRI].

  According to the value of SWCRR[SWRI], the WDT timer causes a hard reset or machine check interrupt to the core.

  — Reset mode (SWCRR[SWRI] = 1)

  Software watchdog timer causes a hard reset (this is the default value after hard reset)

  — Interrupt mode (SWCRR[SWRI] = 0)

  Software watchdog timer causes a machine check interrupt to the core

5.5.5.5, 5-43 In Table 5-43, “RTEVR Bit Settings,” update AIF bit field description to “The bit is set if the RTC issues an interrupt when the RTC counter value equals RTALR[ALRM].”

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5.6.5.5, 5-50	In Table 5-52, “PTEVR Bit Settings,” update PTEVR[PIF] bit field description to “Periodic interrupt flag bit. It is asserted after the SPMPIT counter counts to zero. This status bit should be cleared by software.”
5.7, 5-52	Modified the first paragraph as follows: The following sections describe theory of operation of the two general purpose (global) timer modules, including a definition of the external signals and the functionality. Additionally, the configuration, control, and status registers are described. Note that individual chapters in this book describe additional specific initialization aspects for each individual block.
5.7.1, 5-52	Added the following paragraph: Note that while the MPC8349EA has two global timer modules, signals GTM2_TOUT2 and GTM2_TOUT4 are not available externally.
5.7.2, 5-53	Update section title to “GTM Features.” Update fifth and sixth items in the bullet list to: • Maximum period of ~206 seconds (at 333-MHz bus clock in slow go mode, primary and secondary prescaler = 256) for 16-bit timer • Maximum period of ~3298 seconds (at 333-MHz bus clock and prescaler = 256) for 32-bit timer
5.7.3, 5-53	Update title to “GTM Modes of Operation.” Update section to read: “The GTM unit can operate in the following modes: • Cascaded modes • Clock source modes • Reference modes • Capture modes”
5.7.4.2, 5-55	In Table 5-54, “GTM External Signals—Detailed Signal Descriptions,” update the state meaning of signal TGATEn description from “In a reset gate mode...” to “In a restart gate mode...” In the state meaning of signal TOUTn, clarify #2 by changing “TOUTn changes occur on the rising edge of the system clock” to “TOUTn begins or stops counting, depending on the signal state and the configured mode.”; also clarify Timing by changing “system clock” to “timer input clock.”
5.7.6.1, 5-65	In the second paragraph following the bulleted list, update 65,537 to 65,536. In the third paragraph, update the final sentence to read “The maximum period (when the reference value is all ones and the prescaler divides by 256) for one 16-bit timer is ~206 s at 333 MHz.”
5.7.6.3, 5-66	In the note at the end of the section, update “the counter begins counting after...” to “the counter begins or stops counting after one system clock when working with the internal clock.”
6.1.1, 6-1	Added the following note to section: “Write accesses to different interfaces are not guaranteed to finish in order.”

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6.2.1, 6-3	In Table 6-2, “ACR Field Descriptions, change reserved fields throughout table to read “Reserved, write should preserve reset value.”
6.2.3, 6-5	Add the following section. Renumber subsequent sections accordingly.

6.2.3 Arbiter Transfer Error Register (ATER)

Arbiter transfer error register (ATER) specifies, which kind of events are considered as error events. If event is defined as non error event, it also won’t be reported neither in event register nor in event attributes and address registers. For transfer types, that are not defined as error events, arbiter also does not end address/data tenures. Figure 6-3 shows the fields of ATER.

Offset 0x08 Access: Read/Write

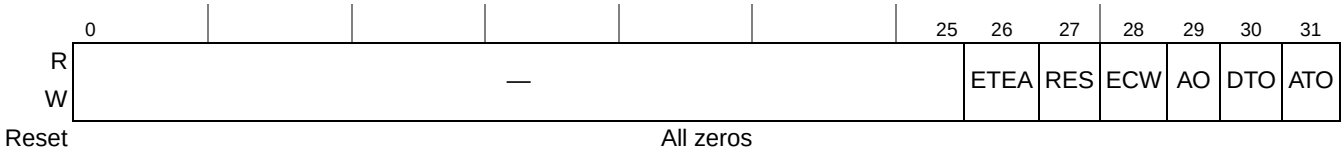

Figure 6-3. Arbiter Transfer Error Register (ATER)

Table 6-4 defines the bit fields of ATER.

Table 6-4. ATER Bit Settings

Bits	Name	Description
0–25	—	Write reserved, read = 0
26	ETEA	External $\overline{\text{TEA}}$. Specifies, whether assertion of $\overline{\text{TEA}}$ signal by one of the slaves is going be reported in arbiter event registers. 0 Assertion of $\overline{\text{TEA}}$ signal by one of the slaves isn’t reported in arbiter event registers. 1 Assertion of $\overline{\text{TEA}}$ signal by one of the slaves is reported in arbiter event registers.
27	RES	Reserved transfer type. Specifies, whether transaction with reserved transfer type will be reported in arbiter event registers. 0 Reserved transaction isn’t reported in arbiter event registers. 1 Reserved transaction is reported in arbiter event registers.
28	ECW	External Control Word transfer type. Specifies, whether transaction with external control word transfer type will be reported in arbiter event registers. 0 External control word read/write transaction isn’t reported in arbiter event registers. 1 External control word read/write transaction is reported in arbiter event registers.
29	AO	Address Only transfer type. Specifies, whether transaction with address only transfer type will be reported in arbiter event registers. 0 Address only transaction isn’t reported in arbiter event registers. 1 Address only transaction is reported in arbiter event registers.

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Table 6-4. ATER Bit Settings

Bits	Name	Description
30	DTO	DTO - Data Time Out. Specifies, whether data tenure time out will be reported in arbiter event registers. 0 Data time out isn't reported in arbiter event registers. 1 Data time out is reported in arbiter event registers.
31	ATO	ATO - Address Time Out. Specifies, whether address tenure time out will be reported in arbiter event registers. 0 Address time out isn't reported in arbiter event registers. 1 Address time out is reported in arbiter event registers.

6.2.6, 6-8 In Figure 6-6, "Arbiter Event Attributes Register (AEATR)," update the access from read/write to read only.

6.2.7, 6-9 In Figure 6-7, "Arbiter Event Address Register (AEADR)," update the access from read/write to read only.

6.3.1.3, 6-13 Update final sentence in paragraph to read "After the completion of snoop copyback, the arbiter grants the bus to the most ahead master among those masters which have an active bus request signal at that time, which may or may not be the same master that had its transaction ARTRYed. Only when a transaction address phase is completed with no ARTRY (and no repeat conditions), the master moves to the end of the line."

7.3.1, 7-14 Removed performance monitor registers from Figure 7-2, both from user model and supervisor model.

7.3.1.3.3, 7-20 In Table 7-2, "e300 HID0 Bit Descriptions, add the following note to EBA and EBD field descriptions: "Do not set this bit; the CSB does not have parity signals.

7.3.1.3.3, 7-22 Added new table to show how HID0[ECLK] and HID0[SBCLK] are used to set frequency of *clk_out* signal.

Table 7-3. Using HID0[ECLK] and HID0[SBCLK] to Configure *clk_out*

hreset	**ECLK**	**SBCLK**	***clk_out***
Asserted	x	x	Bus clock (small pulse for every rising edge of sysclk)
Negated	0	0	Clock output off
	0	1	Core clock/2
	1	0	Core clock
	1	1	Bus clock

7.3.2.2, 7-27 Removed last bullet and sub-bullets concerning performance monitor instructions (**mfmpr** and **mtmpr**); these instructions are not supported on this device.

8.4.2, 8-5 In Table 8-2, "IPIC External Signals—Detailed Signal Descriptions," in the IRQ[0:7] state meaning description, remove the following sentence fragment: "(according to the programmed polarity),"

8.5.2, 8-10–8-11	In Table 8-6, “IVEC/CVEC/MVEC Field Definition,” changed the interrupt meaning for interrupt ID number 69 from USB MPH to MU and for 71 from USB MPH to DMA.
8.5.2, 8-11	In Table 8-6, “IVEC/CVEC/MVEC Field Definition,” update the Interrupt Vector range for Interrupt ID number 92–127 to “0b101_1111–0b111_1111”
8.5.11, 8-20	In Figure 8-14, “System External Interrupt Mask Register (SEMSR),” change the text appearing under the reset values of 0–15 bits from: "The reset values of implemented bits reflect the values of the external IRQ signals. Reserved bits are zeros." to “All zeros.”
	In addition, remove the second footnote.
8.5.16, 8-25	In Table 8-25, “SIFCR_H Field Descriptions,” and Table 8-26, “SIFCR_L Field Descriptions,” changed description to read “... corresponds to an internal interrupt source....”
Chapter 9	Removed all references to differential strobe signals ($\overline{\text{MDQS}}$).
9.1, 9-1	Changed first sentence to read as follows:
	The fully programmable DDR SDRAM controller supports most JEDEC standard x8, x16, or x32 DDR and DDR2 memories available.
9.3.1, 9-3	Added a note before Table 9-1, “DDR Memory Interface Signal Summary,” as follows:
	“The MCKE logic LOW state cannot be guaranteed in the first moments (50-200 ns) following /PORESET assertion. This will cause the DDR to exit from self-refresh mode. To prevent exit from the self-refresh mode, it is recommended to use /HRESET instead of /PORESET. However, while using /PORESET, an external circuit is needed for the MCKE logic to force the signal low during /PORESET assertion, and to prevent exit from the self-refresh mode.”
9.3.2.1, 9-5	Replaced description of MDQS as follows:
	Data strobes. Inputs with read data, outputs with write data.
9.3.2.1, 9-5	In Table 9-3, “Memory Interface Signals—Detailed Signal Descriptions,” update the timing signal description of MA[14:0] to:
	“Assertion/Negation—The address lines are only driven when the controller has a command scheduled to issue on the address/CMD bus; otherwise they will be at high-Z. It is valid when a transaction is driven to DRAM (when MCS*n* is active).”

9.4.1.6, 9-18 Modified descriptions of TIMING_CFG_2 fields CPO and FOUR_ACT as follows:

Table 9-11. TIMING_CFG_2 Register Field Descriptions

Bits	Name	Description
4–8	CPO[1]	$\overline{\text{MCAS}}$-to-preamble override. Defines the number of DRAM cycles between when a read is issued and when the corresponding DQS preamble is valid for the memory controller. For these decodings, “READ_LAT” is equal to the CAS latency plus the additive latency. 00000READ_LAT + 1 00001Reserved 00010READ_LAT 00011READ_LAT + 1/4 00100READ_LAT + 1/2 00101READ_LAT + 3/4 00110READ_LAT + 1 00111READ_LAT + 5/4 01000READ_LAT + 3/2 01001READ_LAT + 7/4 01010READ_LAT + 2 01011READ_LAT + 9/4 01100READ_LAT + 5/2 01101READ_LAT + 11/4 01110READ_LAT + 3 01111READ_LAT + 13/4 10000READ_LAT + 7/2 10001READ_LAT + 15/4 10010READ_LAT + 4 10011READ_LAT + 17/4 10100READ_LAT + 9/2 10101READ_LAT + 19/4 10110–11111 Reserved
. . .		
26–31	FOUR_ACT	Window for four activates (t_{FAW}). This is applied to DDR2 with eight logical banks only. Must be set to 0001 for DDR1. 000000Reserved 0000011 cycle 0000102 cycles 0000113 cycles 0001004 cycles . . . 01001119 cycles 01010020 cycles 010101–111111 Reserved

[1] For CPO decodings other than 00000 and 11111, ‘READ_LAT’ is rounded up to the next integer value

9.4.1.7, 9-20 In Table 9-12, “DDR_SDRAM_CFG Field Descriptions,” added notes to RD_EN and 2T_EN field descriptions stating that these fields must not both be set at the same time.

9.4.1.7, 9-20 In Table 9-12, “DDR_SDRAM_CFG Field Descriptions,” modify the notes in the 8_BE field description to read as follows:

Note: DDR1 must use 8-beat bursts when using 32-bit bus mode (32_BE = 1) and 4-beat bursts when using 64-bit bus mode.

Note: DDR2 must use 4-beat bursts when using 32/64-bit bus mode.

9.4.1.8, 9-23 Changed setting 01 of DDR_SDRAM_CONFIG_2[DQS_CFG] to reserved.

9.4.1.14, 9-28 Replaced this section with the following:

The DDR SDRAM clock control configuration register, shown in Figure 9-15, provides a 1/4-cycle clock adjustment.

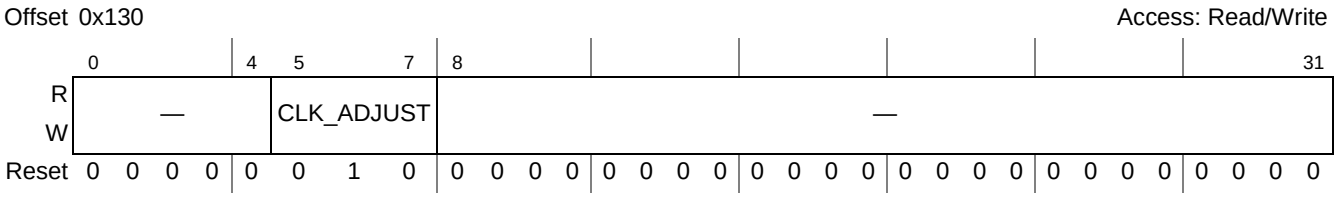

Figure 9-15. DDR SDRAM Clock Control Configuration Register (DDR_SDRAM_CLK_CNTL)

Table 9-20 describes the DDR_SDRAM_CLK_CNTL fields.

Table 9-20. DDR_SDRAM_CLK_CNTL Field Descriptions

Bits	Name	Description
0–4	—	Reserved
5–7	CLK_ADJUST	Clock adjust 000 Clock will be launched aligned with address/command 001 Clock will be launched 1/4 applied cycle after address/command 010 Clock will be launched 1/2 applied cycle after address/command 011 Clock will be launched 3/4 applied cycle after address/command 100 Clock will be launched 1 applied cycle after address/command 101–111Reserved
8	—	Reserved, should be set to 0
9–31	—	Reserved

9.4.1.23, 9-33 In Figure 9-24, “Memory Data Path Read Capture ECC Register (CAPTURE_ECC),” extend bit field for ECE from 24–31 to 16–31.

In Table 9-29, “CAPTURE_ECC Field Descriptions,” add the following:

16:23—8-bit ECC code for 1st 32 bits
24:31—8-bit ECC code for 2nd 32 bits
Note: In 64-bit mode, only 24–31 should be used, although 16–23 shows the 8-bit ECC code replicated.

9.4.1.27, 9-36 In Table 9-33, “Capture_Attributes Field Descriptions,” add the following to the TSIZ field description:

000 4 double words
001 1 double word
010 2 double words
011 3 double words
Others Reserved

9.5, 9-39 In paragraph after Figure 9-31, update final sentence to read, “Bank sizes up to 2 Gbits (maximum total physical memory size of 4 Gbytes) are supported, providing up to a maximum of 4 Gbits.”

9.5.3, 9-50 Added sentence to 6th bullet (mode register set): “For DDR2 in 32-bit bus mode, all 32-byte burst accesses from the platform are split into two 16-byte (that is, 4 beat) accesses to the SDRAMs in the memory controller.”

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9.5.6, 9-56 Add the following note after the first paragraph:

NOTE

Application system board must assert the reset signal on DDR memory devices until software is able to program the DDR memory controller configuration registers, and must deassert the reset signal on DDR memory devices before DDR_SDRAM_CFG[MEM_EN] is set. This ensures that the DDR memory devices are held in reset until a stable clock is provided and, further, that a stable clock is provided before memory devices are released from reset.

9.5.11, 9-62 Add the following text before Table 9-49: “In 32-bit mode, Table 9-49 is split into 2 halves. The first half, consisting of rows 0–31, is used to calculate the ECC bits for the first 32 data bits of any 64-bit granule of data. This always applies to the odd data beats on the DDR data bus. The second half of the table, consisting of rows 32–63, is used to calculate the ECC bits for the second 32 bits of any 64-bit granule of data. This always applies to the even data beats on the DDR data bus.”

9.6.1, 9-69 Changed DDR2 setting for DQS_CFG (in Table 9-53) to ‘Should be set to 00.’

9.6.1, 9-70 In Table 9-53, “Programming Differences Between Memory Types,” update the following rows: as shown

ODT_PD_EXIT	ODT Powerdown Exit	DDR1	Should be set to 0001
		DDR2	Should be set according to the DDR2 specifications for the memory used. The JEDEC parameter this applies to is t_{AXPD}.
FOUR_ACT	Four Activate Window	DDR1	Should be set to 00001
		DDR2	Should be set according to the specifications for the memory used (t_{FAW}). Only applies to eight logical banks.

10.3.1.3, 10-18 Updated MAR (memory address register) to show that field A is 32 bits wide (bits 0–31).

10.4.2.3, 10-47 Replace Figure 10-33, “External Termination of GPCM Access,” with the following two figures:

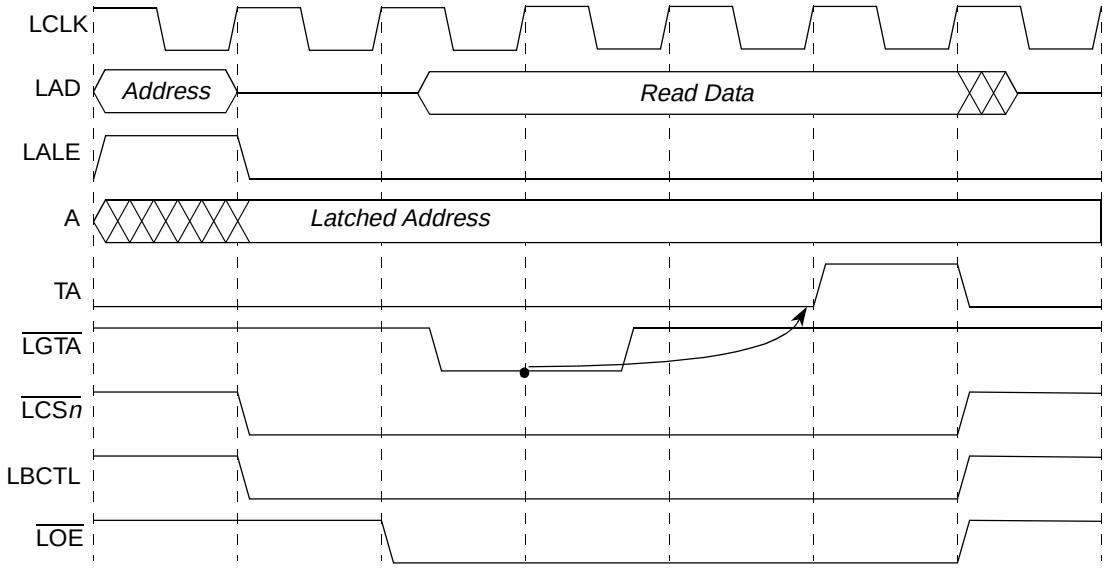

Figure 10-32. External Termination of GPCM Access (PLL Enabled Mode)

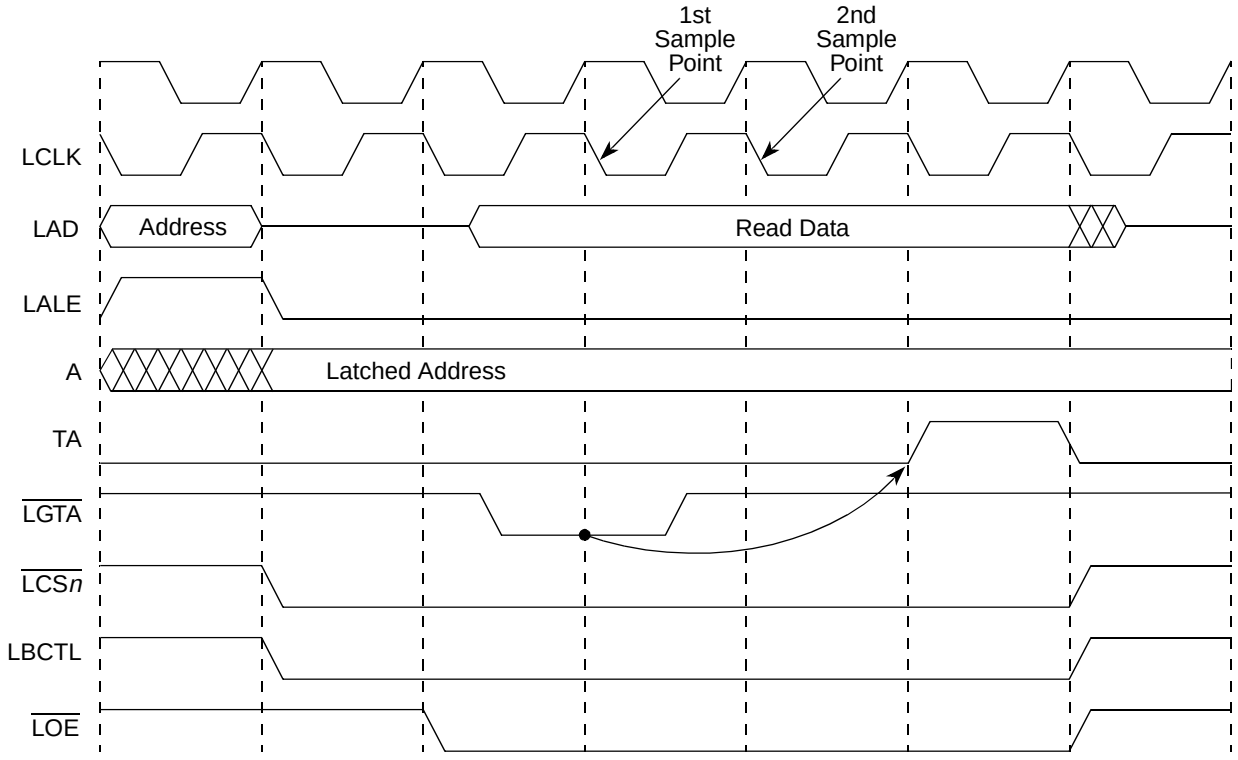

Figure 10-33. External Termination of GPCM Access (PLL Bypass Mode)

10.4.4, 10-59 Add the following statement to the end of the first paragraph: “A gap of two dead LCLK cycles is present on the UPM interface between UPM transactions.”

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10.4.4.2, 10-63	Add the following guidelines to end of section: “For proper signalling, the following guidelines must be followed while programming UPM RAM words: • For UPM reads, program UTA and LAST in the same or consecutive RAM words. • For UPM burst reads, program last UTA and LAST in the same or consecutive RAM words. • For UPM writes, program UTA and LAST in the same RAM word. • For UPM burst writes, program last UTA and LAST in the same RAM word.”
10.4.4.4.1, 10-66	In Table 10-30, “UPM RAM Word Field Descriptions” add the following note to RAM words fields LOOP and AMX: “AMX must not change values in any RAM word which begins a loop.”
10.4.4.4.7, 10-71	Add note “AMX must not change values in any RAM word which begins a loop.”
10.4.4.4.10, 10-73	In the second paragraph, add the following sentence before the final sentence: “Setting the WAEN bit for the first RAM word does not have any effect since the first RAM word signifies the start of a new bus cycle and the initial values of the signals driven onto the bus should be present.”
10.5.6.3, 10-98	In paragraph beginning, “The remaining issue is the synchronization of the UPM cycles...” change parenthetical in final sentence to (LGPL*n* are 1 when inactive).
11.4.1, 11-3	In Table 11-2, “POTAR*n* Field Descriptions, add the following sentence to the TA bit field description: “The translation address must be aligned based on the window’s size.”
12.4.1, 12-5	In Figure 12-2, “Outbound Message Interrupt Status Register (OMISR),” update bits 0 and 1 to w1c and user access to “mixed.”
12.4.2, 12-6	Update second sentence in the register description paragraph to “OMIMR can be read from the CSB or the PCI bus, but it can be written only from the PCI bus.”
12.4.6, 12-9	Changed IMISR access to mixed—bits IM1I and IM0I are w1c.
12.4.6, 12-9	Replaced first paragraph with the following: The IMISR contains the interrupt status of the doorbell and message register events. Writing a 1 to IM1I clears the bit. The events are generated by the PCI masters.
12.4.7, 12-11	Replaced first paragraph with the following: This register contains the interrupt mask of the doorbell and message register events generated by the PCI master. Figure 12-9 shows the IMIMR fields.
12.4.8.1, 12-13	In Table 12-11, “DMAMRn Field Descriptions,” added the following to bit fields DAHE and SAHE: “The DMA does not support address hold when external trigger mode is selected (EMSEN = 1).”
12.4.8.1, 12-13	In Table 12-11, “DMAMRn Field Descriptions,” update the TEM bit description to read: 0 The DMA will halt when a transfer error occurs. 1 The DMA will complete the transfer regardless of whether a transfer error occurs.

Note: Regardless of the setting of TEM, if an error condition was detected during the DMA transfer, it will cause DMASRn[TE] to be set.

12.4.8.2, 12-14 In Table 12-12, “DMASRn Field Descriptions,” update TE bit description to read “Set when there is an error condition during the DMA transfer.”

Update CB bit description to read “It is cleared as a result of any of the following conditions: an error or completion of the DMA transfer.”

12.5.3, 12-20 Update paragraph beginning “Accesses to CSB memory depend...” to read, “Accesses to CSB memory depend on the alignment of the source and destination addresses and the size of the transfer. The DMA controller transfers a full cache line whenever possible. On misaligned addresses, full cache line transfers (32 byte bursting) occur if the source and destination offsets end in the same byte offset. For example, if the destination address is 0x4000_1050 and the source address is 0x9000_2050, the transfer bursts because both end in 0x50. However, if the destination address is 0x4000_1050 and the source is 0x9000_2000, the transfer does not burst because the last byte offset is not the same. On misaligned destination addresses, subtransfers of less than a cache line occur on the initial and final beats of the transfer while full cache lines occur on intermediate beats.”

13.3.2.12, 13-26 Add the following text at the end of the introductory paragraph: “Inbound and outbound windows for the same bus should not overlap. Therefore, situations where an inbound window translation points back into an outbound window, or where an outbound translation window points back into an inbound window, are not allowed.”

13.3.2.12, 13-27 In Table 13-19, “PITAR*n* Field Descriptions,” update translation address (TA) field to include the sentence “The specified address must be aligned to the window size, as defined by PIWARn[IWS].”

13.3.2.13, 13-27 In Table 13-20, “PIBAR*n* Field Descriptions,” update base address (BA) field to include the sentence “The specified address must be aligned to the window size, as defined by PIWARn[IWS].”

13.3.3.13, 13-37 Modified PIMMR[BA] as follows:

Offset 10 Access: Read/Write

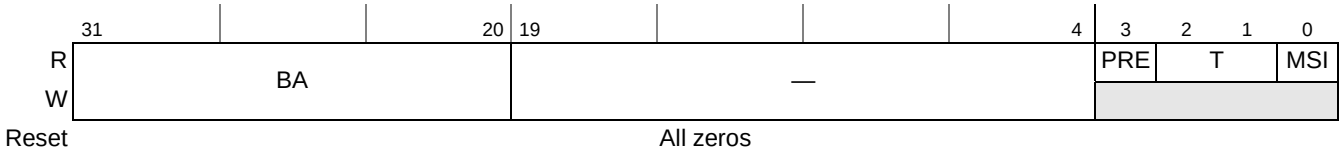

Figure 13-32. PIMMR Base Address Configuration Register

Table 13-34. PIMMR Base Address Configuration Register Field Descriptions

Bits	Name	Description
31–20	BA	Base address. Defines the base address for the internal (on-chip) memory-mapped register space. The size of this space is 1 MB.
19–4	—	Reserved

Table 13-34. PIMMR Base Address Configuration Register Field Descriptions (continued)

Bits	Name	Description
3	PRE	Prefetchable. Hard-wired to 0.
2–1	T	Type. Hard-wired to 00.
0	MSI	Memory space indicator. Hard-wired to 0.

13.4.8, 13-61 Add the following section

13.4.8 Byte Ordering

Whenever data must cross a bridge between two busses, the byte ordering of data on the source and destination buses must be considered. The internal platform bus of this device is inherently big endian and the PCI bus interface is inherently little endian.

There are two methods to handle ordering of data as it crosses a bridge—address invariance and data invariance. Address invariance preserves the addressing of bytes within a scalar data element, but not the relative significance of the bytes within that scalar. Conversely, data invariance preserves the relative significance of bytes within a scalar, but not the addressing of the individual bytes that make up a scalar.

This device uses address invariance as its byte ordering policy

14.1, 14-2 Removed second sub-bullet of bullet “Master/slave logic, with DMA capability” (item read “Up to 200-MHz operation)

14.5.6.9.1, 14-78 Update the following bullets:

- IV1 holds the *least* significant bytes of the initialization vector (bytes 1–8).
- IV2 holds the *most* significant bytes of the initialization vector (bytes 9–16).

to the following bullets:

- IV1 holds the *most* significant bytes of the initialization vector (bytes 1–8).
- IV2 holds the *least* significant bytes of the initialization vector (bytes 9–16).

14.7.2.4, 14-98 In Figure 14-75, “ID Register,” and its introductory sentence, update reset value to 0x0030_0000_0001_0003.

15.5.3.1.4, 15-26 In Table 15-7, modified description of ECNTRL[R100M] to read as follows:

RGMII 100 mode. This bit is ignored unless ECNTRL[RPM] = 1 and MACCFG2[I/F Mode] = 01.
0 RGMII is in 10-Mbps mode
1 RGMII is in 100-Mbps mode

15.5.3.6.2, 15-50 In Table 15-34, changed field description of MACCFG2[I/F Mode] as follows:

Determines the type of interface to which the MAC is connected. Its default is 00.
00 Reserved
01 MII
10 GMII/RGMII/TBI/RTBI
11 Reserved

Section, Page No.	Changes
15.5.3.6.6, 15-54	In field description of MIIMCFG[MgmtClock Select] in Table 15-38, “MIIMCFG Field Descriptions,” replaced reference to clock register to read SCCR[TSEC*n*CM].
15.6.2.6.3, 15-115	Add the following subsection:

15.6.2.6.3 CRC Computation Examples

There are many algorithms for calculating the CRC value of a number. Refer to the RFC 3309 standard, which can be found at http://www.faqs.org/rfcs/rfc3309.html, to compute the CRC value for the purposes of TSEC. The RFC 3309 algorithm uses the following polynomial to calculate the CRC value:

x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x1 + x0 or 0x04c11db7

Given a destination MAC address of DA = 01000CCCCCCC, the algorithm results in a CRC remainder value of 0xA29F4BBC.

Bit-reversing the low-order byte of the CRC value (0xBC) yields:

BR_CRC = 0x3D = 0b00111101

The high-order 3-bits of the new BR_CRC value are used to select which 32-bit register (of the 8) to use. This example maps the DA to register 1.

High-order 3 bits of BR_CRC: HO_CRC = 0b001 = 1

The low-order 5 bits are used to select which bit to set in the given register (with a value of 0 setting 0x8000_0000 and 31 setting 0x0000_0001). Therefore, the example DA maps to bit 29 of register 1.

Low-order 5 bits of BR_CRC: LO_CRC = 0b11101 = 29

Therefore, GADDR1 is ORed with the value 0x0000_0004.

Additional calculated examples follow:

Example 1:

- Destination MAC address: DA = 01005E000128
- CRC remainder value: CRC = 0x821D6CD3
- Bit-reversed least-significant byte of CRC value: BR_CRC = 0xCB = 0b11001011
- High-order 3 bits of BR_CRC: HO_CRC = 0b110 = 6
- Low-order 5 bits of BR_CRC: LO_CRC = 0b01011 = 11
- GADDR6 = 0x0010_0000

Example 2:

- Destination MAC address: DA = 0004F0604F10
- CRC remainder value: CRC = 0x1F5A66B5
- Bit-reversed least-significant byte of CRC value: BR_CRC = 0xAD = 0b10101101
- High-order 3 bits of BR_CRC: HO_CRC = 0b101 = 5
- Low-order 5 bits of BR_CRC: LO_CRC = 0b01101 = 13
- GADDR5 = 0x0004_0000

Section, Page No.	Changes
15.7.1.14, 15-127	In Table 15-123, changed the value of ECNTRL in step 5 from [0000_0000_0000_0000_0001_0000_0000_0000] to [0000_0000_0000_0000_0001_0000_0001_0000].
16.3.1.3, 16-20	In Table 16-10, ““HCSPARAMS Register Field Descriptions,” update reset value for DR of N_TT from “0001” to “0000.”
16.3.2.16, 16-42	In Table 16-29, “PORTSC*n* Register Field Descriptions,” swapped LS settings 01 and 10 as follows: 01 K-state 10 J-state
16.3.2.27, 16-54	Update “If AGE_CNT_THRESH is equal to zero, priority state zero is always chosen.” to “If AGE_CNT_THRESH is equal to zero, priority state one is always chosen.”
16.3.2.28, 16-56	Update the following row in Table 16-41, “SI_CTRL Register Field Descriptions,” as shown:

31	rd_prefetch_val	Selects whether 32 bytes or 64 bytes are fetched during burst read transactions at the system interface. When this input is LOW 64 bytes are fetched and when it is HIGH 32 bytes are fetched. The setting of rd_prefetch_val must match the setting of the larger of TXPBURST and RXPBURST fields in the BURSTSIZE register. If either of these fields is 64 bytes, then rd_prefetch_val must be left cleared. Otherwise, this value should be set. 0 64-byte fetch 1 32-byte fetch

16.5.6, 16-74 Update Figure 16-43, “Queue Head Layout,” as follows:

31–27	26–24	23–21	20–16	15	14–12	11–8	7	6–5	4–3	2–1	0	offset
Queue Head Horizontal Link Pointer									00	Typ	T	0x00
RL	C	Maximum Packet Length		H	dtc	EPS	EndPt		I	Device Address		0x04[1]
Mult	Port Number	Hub Addr		μFrame C-mask			μFrame S-mask					0x08[1]
Current qTD Pointer[2]									00000			0x0C
Next qTD Pointer[2]									0000		T[2]	0x10[3]
Alternate Next qTD Pointer[2]									NakCnt[2]		T[2]	0x14[3,4]
dt[1]	Total Bytes to Transfer[2]			ioc[2]	C_Page[2]		Cerr[2]	PID Code[2]	Status[2]			0x18[3,4]
Buffer Pointer (Page 0)[2]							Current Offset[2]					0x1C[3,4]
Buffer Pointer (Page 1)[2]							0000	C-prog-mask[2]				0x20[3,4]
Buffer Pointer (Page 2)[2]							S-bytes[2]			FrameTag[2]		0x24[3,4]
Buffer Pointer (Page 3)[2]							0000_0000_0000					0x28[3]
Buffer Pointer (Page 4)[2]							0000_0000_0000					0x2C[3]

Figure 16-43. Queue Head Layout

[1] Offsets 0x04 through 0x0B contain the static endpoint state.

[2] Host controller read/write; all others read-only.

[3] Offsets 0x10 through 0x2F contain the transfer overlay.
[4] Offsets 0x14 through 0x27 contain the transfer results.

16.7.1, 16-138 Updated Figure 16-69, “Endpoint Queue Head Layout,” as follows:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
Mult		zlt	00		Maximum Packet Length											ios	000_0000_0000_0000																	0x00
Current dTD Pointer[1]																											0_0000					0x04
Next dTD Pointer[1]																											0000				T[1]	0x08[2]
0	Total Bytes[1]															ioc[1]	000			MultO[1]		00		Status[1]								0x0C[2]
Buffer Pointer (Page 0)[1]																				Current Offset[1]												0x10[2]
Buffer Pointer (Page 1)[1]																				Reserved												0x14[2]
Buffer Pointer (Page 2)[1]																				Reserved												0x18[2]
Buffer Pointer (Page 3)[1]																				Reserved												0x1C[2]
Buffer Pointer (Page 4)[1]																				Reserved												0x20[2]
Reserved																																0x24
Set-up Buffer Bytes 3–0[1]																																0x28
Set-up Buffer Bytes 7–4[1]																																0x2C

Figure 16-69. Endpoint Queue Head Layout

[1] Device controller read/write; all others read-only.
[2] Offsets 0x08 through 0x20 contain the transfer overlay.

16.7.2, 16-140 Update Figure 16-70, “Endpoint Transfer Descriptor (dtD) as follows:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	offset
Next Link Pointer																													0000		T	0x00
0	Total Bytes[1]															ioc	000			MultO		00		Status[1]								0x04
Buffer Pointer (Page 0)																				Current Offset[1]												0x08
Buffer Pointer (Page 1)																				0	Frame Number[1]											0x0C
Buffer Pointer (Page 2)																				0000_0000_0000												0x10
Buffer Pointer (Page 3)																				0000_0000_0000												0x14
Buffer Pointer (Page 4)																				0000_0000_0000												0x18

Figure 16-70. Endpoint Transfer Descriptor (dTD)

[1] Device controller read/write; all others read-only.

17.3.1.2, 17-6 Added two notes to Table 17-5, “I2Cn FDR Field Descriptions,” as follows:

Note: The values shown in the table are applicable only for the default value of DFSRR. Refer to AN2919.
Note: I^2C controller clock of I^2C1 is derived from csb_clk / SCCR[SDHCCM].

Section, Page No.	Changes
17.3.1.5, 17-9	In Table 17-8, “I2C*n*DR Field Description,” modify the last sentence in the DATA description to read as follows: “Note that in both master receive and slave receive modes, the very first read is always a dummy read.”
17.5.5, 17-23	Remove the following sentence, “For 1-byte transfers, a dummy read should be performed by the interrupt service routine (see Figure 17-11).”
18.2.2, 18-5	In Table 18-2, “DUART Signals—Detailed Signal Descriptions,” for UART_RTS[1:2], change sentence in description from: “Can be programmed to be automatically negated and asserted by either the receiver or transmitter” to: “Can be programmed to be negated and asserted by either the receiver or transmitter.”
18.3.1.3, 18-8	Update calculating percent error value step 1 calculation (at end of section) to “AFI = baud rate × 16 × divisor”
19.2.3.3, 19-6	Update the paragraph following Figure 19-3 to read as follows: “The SPI can transfer a single character at a rate of input clock/4 in master mode and input clock/2 in slave mode, subject to the timing parameters of the interconnected devices and board trace delays. Gaps should be inserted between multiple characters to keep from exceeding the maximum sustained data rate.”
19.4.1.2, 19-12	In Table 19-5, “SPIE Field Descriptions,” update description of bit 17 (LT) to the following: “Last character was transmitted.” The last character of the frame was completely transferred. This bit is set only if the transmitted character was the last character of the frame (if SPCOM[LST] is set). New data can be written to SPITD is indicated by bit NF.”
19.4.1.4, 19-14	Changed SPCOM to write only in Figure 19-9, “SPI Command Register (SPCOM)”
19.4.1.4, 19-14	In Table 19-7, “SPCOM Field Descriptions,” add the sentence “This bit is cleared internally” to SPCOM[LST] description.”
19.4.1.5, 19-14	Changed SPITD to write only in Figure 19-10, “SPI Transmit Data Hold Register”

20.1, 20-1 Removed resistor from TCK signal in Figure 20-1. Figure should appear as follows:

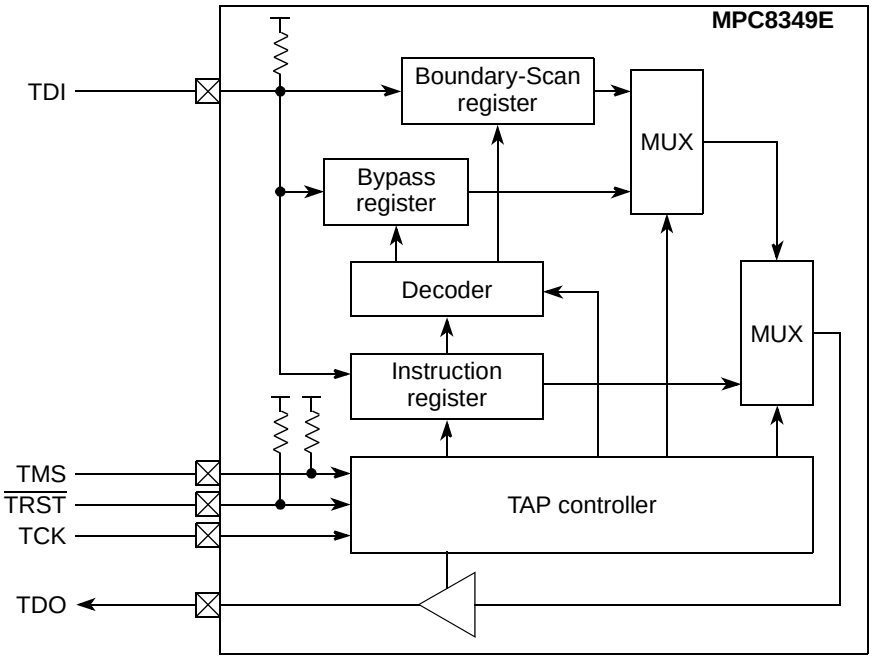

Figure 20-71. JTAG Interface Block Diagram

20.2.1, 20-2 Removed reset values (replaced with '—') from all input signals (TCK, TDI, TMS) in Table 20-1, "JTAG Test Signals Summary." Modified function column of TCK and $\overline{\text{TRST}}$. Table should appear as follows:

Table 20-1. JTAG Test Signals Summary

Name	Description	Functional Block	Function	Reset Value	I/O
TCK	Test clock	Debug	Clock for JTAG testing.	—	I
TDI	Test data input		Serial input for instructions and data to the JTAG test subsystem. Internally pulled up.	—	I
TDO	Test data output		Serial data output for the JTAG test subsystem. High impedance except when scanning out data.	High impedance	O
TMS	Test mode select		Carries commands to the TAP controller for boundary scan operations. Internally pulled up.	—	I
$\overline{\text{TRST}}$	Test reset		Resets the TAP controller asynchronously. Internally pulled up.	—	I

In the same section, in Table 20-2, "JTAG Test—Detailed Signal Descriptions," removed sentence "An unterminated input appears as a high signal level to the test logic due to an internal pull up resister" from description of $\overline{\text{TRST}}$.

Section, Page No.	Changes
22.3, 22-3	Add the following text to the end of the section: “Use the following sequence to ensure DLL lock before starting to access the local bus devices: 1. Write LCRR[DBYP] = 0 (DLL is enabled). 2. Sync. 3. Wait 1 ms. 4. Poll the DLLSR[LOCK] bit until it becomes 1. 5. Access can now be gained to the local bus devices.”

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