Freescale Semiconductor
User's Manual Addendum

MCF5272UMAD
Rev. 6, 02/2006

MCF5272 Integrated Microprocessor User's Manual Errata

by: Microcontroller Division

This errata document describes corrections to the *MCF5272 ColdFire Integrated Microprocessor User's Manual*, order number MCF5272UM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/coldfire for the latest updates.

The current version available of the MCF5272 User's Manual is Revision 2.1.

Table of Contents

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1 Errata for Revision 2 & 2.1

Table 1. MCF5272UM Rev 2 & 2.1 Errata

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 9-3/Page 9-4</td><td>Change “Total page size” row as shown below:
Table 9-3. Configurations for 16-Bit Data Bus
<table>
<tr><th rowspan="2">Parameter</th><th colspan="2">8-Bit</th><th colspan="4">16-Bit</th></tr>
<tr><th>16 Mbits</th><th>64 Mbits</th><th>16 Mbits</th><th>64 Mbits</th><th>128 Mbits</th><th>256 Mbits</th></tr>
<tr><td>Number of devices</td><td colspan="2">2</td><td colspan="4">1</td></tr>
<tr><td>Total size</td><td>4 Mbytes</td><td>16 Mbytes</td><td>2 Mbytes</td><td>8 Mbytes</td><td>16 Mbytes</td><td>32 Mbytes</td></tr>
<tr><td>Total page size</td><td>2 Kbytes</td><td>4 Kbytes</td><td>2 Kbytes</td><td>4 Kbytes</td><td>4 Kbytes</td><td>8 Kbytes</td></tr>
<tr><td>Number of banks</td><td>2</td><td>4</td><td>2</td><td>4</td><td>4</td><td>4</td></tr>
<tr><td>Refresh count in 64 mS</td><td>4K</td><td>4K</td><td>4K</td><td>4K</td><td>4K</td><td>8K</td></tr>
</table></td></tr>
<tr><td>Table 9-4/Page 9-4</td><td>Change “Total page size” row as shown below:
Table 9-4. Configurations for 32-Bit Data Bus
<table>
<tr><th rowspan="2">Parameter</th><th colspan="2">8-Bit</th><th colspan="4">16-Bit</th><th colspan="2">32-Bit</th></tr>
<tr><th>16 Mbits</th><th>64 Mbits</th><th>16 Mbits</th><th>64 Mbits</th><th>128 Mbits</th><th>256 Mbits</th><th>64 Mbits</th><th>128 Mbits</th></tr>
<tr><td>Number of devices</td><td colspan="2">4</td><td colspan="4">2</td><td colspan="2">1</td></tr>
<tr><td>Total size</td><td>8 Mbytes</td><td>32 Mbytes</td><td>4 Mbytes</td><td>16 Mbytes</td><td>32 Mbytes</td><td>64 Mbytes</td><td>8 Mbytes</td><td>16 Mbytes</td></tr>
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<tr><td>Refresh count in 64 mS</td><td>4K</td><td>4K</td><td>4K</td><td>4K</td><td>4K</td><td>8K</td><td>4K</td><td>8K</td></tr>
</table></td></tr>
<tr><td>Table 11-9/11-14</td><td>Change encodings for bits 31–9 to:
0 The corresponding interrupt source is masked.
1 The corresponding interrupt source is not masked.</td></tr>
<tr><td>Table 13-17/13-33</td><td>The description of CMULT reads “100 x 32” instead of “100 x 23” as printed in the user’s manual.</td></tr>
<tr><td>14.4.3/14-8</td><td>Replaced “Adequate delay between transfers must be specified for long data streams because the QSPI module requires time to load a transmit RAM entry for transfer. Receiving devices need at least the standard delay between successive transfers.” with “Receiving devices need at least the standard delay (DT=0) between successive transfers for long data streams because the QSPI module requires time to load a transmit RAM entry for transfer.”</td></tr>
</table>

Table 1. MCF5272UM Rev 2 & 2.1 Errata (continued)

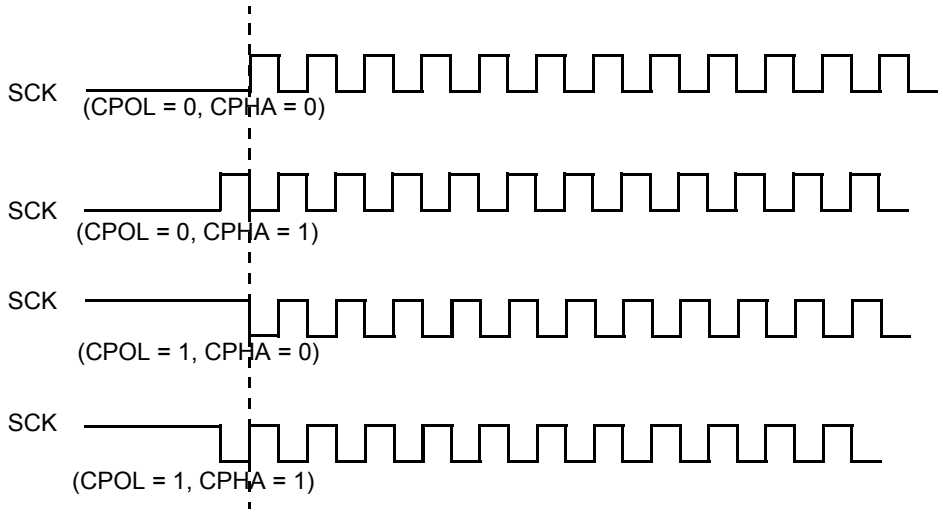
Location	Description
14.5.1/14-11	Added Figure 14-5 “SPI Modes Timing” shown below. 
14.5.6/14-14	Added this text: “A read or a write to QDR causes the value in QAR to increment.”
Table 14-7/14-15	In this table, the CONT bit description has been reworded to read: “Chip selects remain asserted between transfers for a transfer of up to 16 words of data.”
14.5.8/14-16	In example 4, replaced “0x D00F” with “0x D00D.”
15.2/15-3	Changed “Timers 0 and 2” to “Timers 0 and 1” because these drive TOUT0 and TOUT1.
Figure 15-4/15-5	Corrected address field to read “MBAR + 0x208 (TCAP0); 0x228 (TCAP1); 0x248 (TCAP2); 0x268 (TCAP3).”
Figure 16-24/16-23	Changed upper “UART Transmit FIFO (URB) (24 Bytes)” to “UART Transmit FIFO (UTB) (24 Bytes)” and lower “UART Transmit FIFO (URB) (24 Bytes)” to “UART Receive FIFO (URB) (24 Bytes).”
Table 17-5/17-6	The description of PBCNT11 reads “10 Reserved” instead of “10 QSPI_CS” as printed in the user’s manual.
20.12/20-23	Add to note. “SDCLK can be affected if master reset is not used for power-on.”
20.12.1/20-24	Changed $\overline{\text{RSTI}}$ to $\overline{\text{RSTO}}$ in “The levels of the mode select inputs, QSPI_Dout/WSEL, QSPI_CLK/BUSW1, and QSPI_CS0/BUSW0, are sampled when $\overline{\text{RSTO}}$ negates and they select the port size of $\overline{\text{CS0}}$ and the physical data bus width after a master reset occurs.”

Table 1. MCF5272UM Rev 2 & 2.1 Errata (continued)

Location	Description
Figure 20-5/20-10	Replaced Figure 20-5 with the figure below. This figure differs from the user's manual in that it reflects the assertion of $\overline{OE}$, $\overline{BS}$[3:0] one clock earlier.

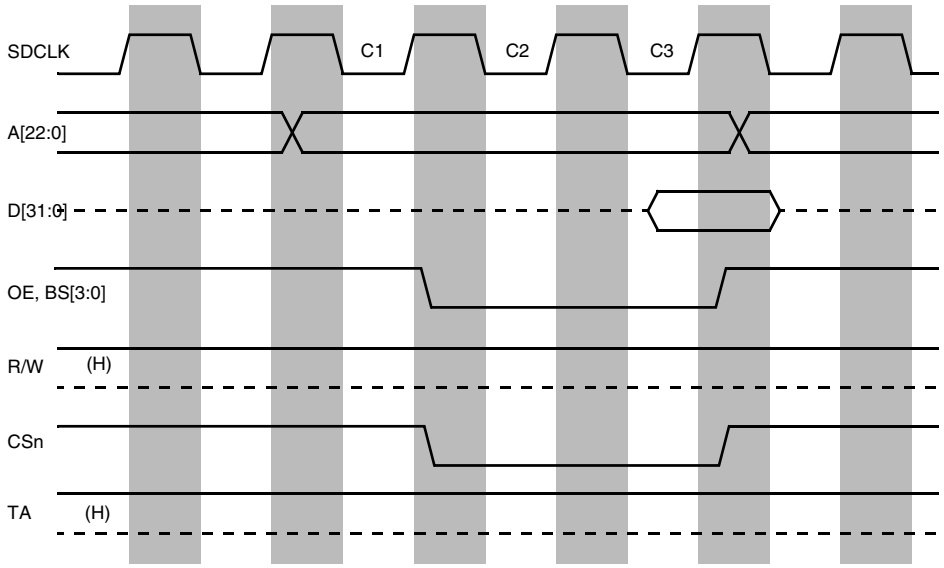
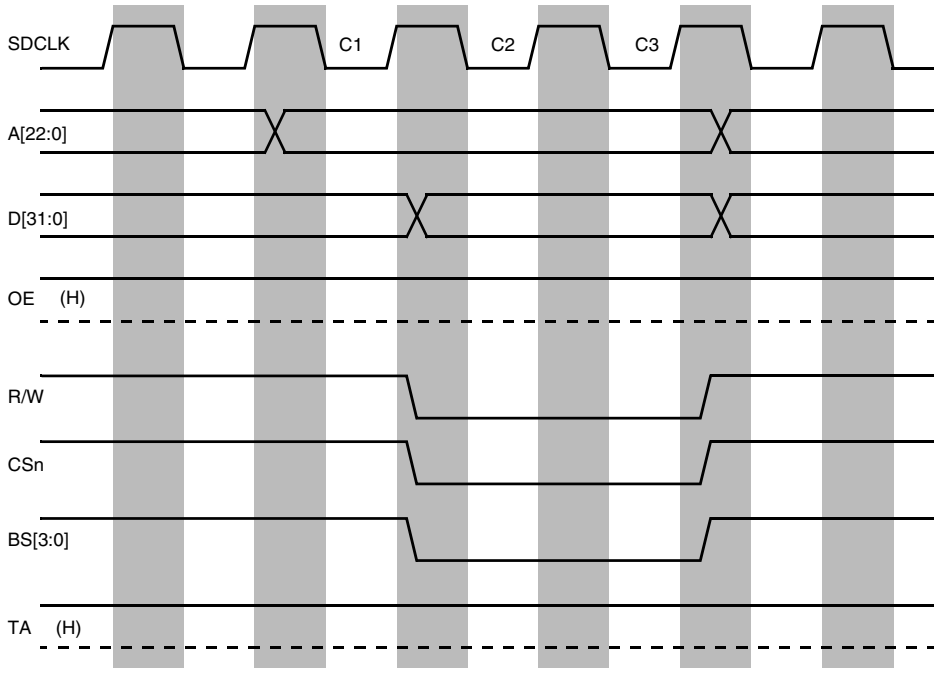


Figure 20-5. Longword Read with Address Setup; EBI = 00; 32-Bit Port; Internal Termination

Table 1. MCF5272UM Rev 2 & 2.1 Errata (continued)

Location	Description
Figure 20-6/20-11	Replaced Figure 20-6 with the figure below. This figure differs from the user's manual in that it reflects the assertion of R/$\overline{W}$, $\overline{BS}$[3:0] one clock earlier.  **Figure 20-6. Longword Write with Address Setup; EBI = 00; 32-Bit Port; Internal Termination**
Table 23-4/23-3	Input high voltage (VIH) maximum entry should be 5.5V instead of 5.0V.

2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
5	• Added Table 11-9 errata. • Added Figure 16-24 errata. • Added SDCLK errata for Section 20.12. • Added VIH max errata.	07/2005
6	• Added SDRAM configuration tables errata.	02/2006

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