Freescale Semiconductor
Reference Manual Addendum

MCF5271RMAD
Rev. 2.2, 05/2007

MCF5271 Reference Manual Errata

by: Microcontroller Division

This errata document describes corrections to the *MCF5271 Reference Manual*, order number MCF5271RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/coldfire for the latest updates.

The current version available of the *MCF5271 Reference Manual* is Revision 2.

Table of Contents

1 Errata for Revision 2 2
2 Errata for Revision 1.1 6
3 Errata for Revision 1 6
4 Revision History 9

1 Errata for Revision 2

Table 1. MCF5271RM Rev 2 Errata

Location	Description
Figure 1-1/Page 1-3	Remove INTC1 from block diagram. Change instance of CIM to “CCM and Reset Controller”.
Section 1.3.1/Page 1-7	Change “Chip Integration Module (CIM)” to “Chip Configuration Module (CCM)”. Move Reset sub-bullet (and its sub-bullets) up one level.
Section 1.3.15/Page 1-11	Remove INTC1 and mention of two interrupt controllers in section. Only one interrupt controller is present on this deivce.
Table 2-1/Page 2-4	Change SD_CKE pin location from 139 to “—” for the 160QFP device.
Table 2-1/Page 2-5	Change QSPI_CS1 pin location from “—” to 139 for the 160QFP device.
Table 2-1/Page 2-6	Change DT3IN pin’s alternate 2 function from “—” to QSPI_CS2. Change DT3OUT pin’s alternate 2 function from “—” to QSPI_CS3.
Table 3-1/Page 3-4	Remove last sentence in C bit field description.
Table 3-5/Page 3-8	Change PC’s Written with MOVEC entry to “No”.
Section 3.4/Page 3-9	Change last bullet to “Use of separate system stack pointers for user and supervisor modes”
Section 3.5/Page 3-10	Change last sentence in fourth paragraph (step 2) to “The IACK cycle is mapped to special locations within the interrupt controller's address space with the interrupt level encoded in the address."
Figure 4-9/Page 4-14	Add minus sign to the exponent so that it is “–(i + 1 – N)”.
Table 5-3/Page 5-7	Change reset value of ACR0, ACR1 to “See Section” since some of the bits are undefined after reset.
Figure 5-2/Page 5-7	Change CACR fields to R/W, since they may be read via the debug module.
Table 5-5/Page 5-10	For split instruction/data cache entry, swap text in parantheses in the description field. Instruction cache uses the upper half of the arrays, while data cache uses the lower half.
Figure 5-3/Page 5-11	Change reset value of ACR: Bits 31-16, 14-13, 6-5, and 2 are undefined, and other bits are cleared. Change ACR fields to R/W, since they may be read via the debug module.
Section 5.2.1.2/Page 5-11	Change note to: **NOTE** Peripheral (IPSBAR) space should not be cached. The combination of the CACR defaults and the two ACR*n* registers must define the non-cacheable attribute for this address space.
Figure 6-1/Page 6-2	Change RAMBAR fields to R/W, since they may be read via the debug module.
Section 8.3.2.11/Page 8-8	Remove mention of INTC1.

Table 1. MCF5271RM Rev 2 Errata (continued)

Location	Description
Section 11.2.1.1/Page 11-3	After the first paragraph add the following note: **NOTE** Accessing reserved IPSBAR memory space could result in an unterminated bus cycle that causes the core to hang. Only a hard reset will allow the core to recover from this state. Therefore, all bus accesses to IPSBAR space should fall within a module's memory map space.
Table 11-11/Page 11-16	Replace INTC1 with — in PACR7[ACCESS_CTRL0] entry.
Table 12-1/Page 12-5	Change SD_CKE pin location from 139 to “—” for the 160QFP device.
Table 12-1/Page 12-6	Change QSPI_CS1 pin location from “—” to 139 for the 160QFP device.
Table 12-1/Page 12-8	Change DT3IN pin’s alternate 2 function from “—” to QSPI_CS2. Change DT3OUT pin’s alternate 2 function from “—” to QSPI_CS3.
Table 12-9/Page 12-19	Change footnote from “...of the RCSC field in the CIM reset configuration register.” to “... of the RCR[RCSC] field in the reset controller.”
Table 12-10/Page 12-20	In PAR_TSIZ1 field change CIM to CCM. In PAR_TSIZ0 field change CIM to CCM.

Table 1. MCF5271RM Rev 2 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 13-1/Page 13-3</td><td>Replace table with the one below to better illustrate the interrupt priority and level assignments.
<table>
<tr><th>Interrupt Level ICR[IL]</th><th>Priority

ICR[IP]</th><th>Supported Interrupt Sources</th></tr>
<tr><td rowspan="10">7</td><td>7</td><td rowspan="4">#8–63</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td></tr>
<tr><td>— (Mid-point)</td><td>#7 (IRQ7)</td></tr>
<tr><td>3</td><td rowspan="4">#8–63</td></tr>
<tr><td>2</td></tr>
<tr><td>1</td></tr>
<tr><td>0</td></tr>
<tr><td rowspan="3">6</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#6 (IRQ6)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">5</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#5 (IRQ5)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">4</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#4 (IRQ4)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">3</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#3 (IRQ3)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">2</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#2 (IRQ2)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">1</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#1 (IRQ1)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
</table></td></tr>
<tr><td>Table 13-2/Page 13-5</td><td>Remove global IACK registers space row as it is not supported, since there is only one interrupt controller.</td></tr>
<tr><td>Section 13.2.1.6.1/Page 13-13</td><td>Remove instance of INTC1.</td></tr>
<tr><td>Section 13.2.1.7/Page 13-15</td><td>Remove last paragraph as there is no global IACK space.</td></tr>
<tr><td>Figure 14-2/Page 14-3</td><td>Remove this second figure as it is incorrect for this device. The figure preceding it on page 14-2 (without $\overline{\text{DREQ3}}$) is correct.</td></tr>
<tr><td>Section 14.4/Page 14-13</td><td>Remove last sentence in this section starting with “BCRn decrements...” since SAA bit is not supported.</td></tr>
<tr><td>Section 14.4.4.1/Page 14-16</td><td>Remove instances of eTPU in this section.
Change $\overline{\text{DREQ}}$[32:0] to $\overline{\text{DREQ}}$[2:0].</td></tr>
<tr><td>Figure 14-9/Page 14-17</td><td>Change CLKIN to CLKOUT
Add overbars to TS, CS, and TA.
Remove extra figure that contains A[31:0].</td></tr>
<tr><td>Section 14.4.4.1/Page 14-17</td><td>Remove all text and figures in this section starting with “Since bus timings...”</td></tr>
</table>

Table 1. MCF5271RM Rev 2 Errata (continued)

Location	Description
Figure 15-3/Page 15-4	Figure incorrectly shows that EPDDR is 16-bits wide. Change to an 8-bit register with each EPDD*n* bit a one-bit field from bits 7–1 to match Table 15-4.
Figure 16-2/Page 16-5	Re-labeled the WS states in the timing diagram. The first should be IWS to indicate that the length of this wait state is determined by CSCR[IWS]. The rest of the wait states should be IWS/SWWS to indicate that either CSCR[IWS] or CSCR[SWWS] determine the length of the wait state depending on the value of CSCR[AA].
Figure 16-3/Page 16-5	Re-labeled the WS states in the timing diagram. The first should be IWS to indicate that the length of this wait state is determined by CSCR[IWS]. The rest of the wait states should be IWS/SRWS to indicate that either CSCR[IWS] or CSCR[SRWS] determine the length of the wait state depending on the value of CSCR[AA]. Change Write labels on the data signals to Read.
Table 18-5/Page 18-8	Add the following note to the DACR*n*[CBM] field description: **Note:** It is important to set CBM according to the location of the command bit.
Table 19-1/Page 19-5	Correct MIB block counters end address to IPSBAR + 0x12FF.
Table 19-3/Page 19-8	Add RMON_R_DROP with an IPSBAR Offset of 0x1280 and a description of ‘Count of frames not counted correctly’.
Section 19.3.6/Page 19-38	Add the following subsection entitled “Duplicate Frame Transmission”: The FEC fetches transmit buffer descriptors (TxBDs) and the corresponding transmit data continuously until the transmit FIFO is full. It does not determine whether the TxBD to be fetched is already being processed internally (as a result of a wrap). As the FEC nears the end of the transmission of one frame, it begins to DMA the data for the next frame. In order to remain one BD ahead of the DMA, it also fetches the TxBD for the next frame. It is possible that the FEC will fetch from memory a BD that has already been processed but not yet written back (that is, it is read a second time with the R bit still set). In this case, the data is fetched and transmitted again. Using at least three TxBDs fixes this problem for large frames, but not for small frames. To ensure correct operation for either large or small frames, one of the following must be true: • The FEC software driver ensures that there is always at least one TxBD with the ready bit cleared. • Every frame uses more than one TxBD and every TxBD but the last is written back immediately after the data is fetched. • The FEC software driver ensures a minimum frame size, *n*. The minimum number of TxBDs is then (Tx FIFO Size ÷ (*n* + 4)) rounded up to the nearest integer (though the result cannot be less than three). The default Tx FIFO size is 192 bytes; this size is programmable.
Figure 28-8/Page 28-7	Move SKMR[CTRM,DKP] bit fieldsfrom 11–7 to 12–8.
Table 28-2/Page 28-8	Correct bit locations for CTRM and DKP fields: 31–13 Reserved 12–9 CTRM 8 DKP 7–5 Reserved
Table 30-13/Page 30-13	Add the following note to the PBR[Address] field description: **Note:** PBR[0] should always be loaded with a 0.
Table 30-21/Page 30-36	Change CSR’s initial state to 0x0000_0000.
Table A-2/Page A-2	Change entry in row IPSBAR+0x00_0D00 from INTC1 to Reserved.

2 Errata for Revision 1.1

Table 2. MCF5271RM Rev 1.1 Errata

Location	Description
Table 2-1/Page 2-5	ERXER direction should be input, ETXEN direction should be output.
Table 2-8/Page 2-11	ERXER direction should be input.
Table 7-3/Page 7-7	Footnote should read: “In 1:1 mode for the MCF5271, $f_{sys} = 2 \times f_{ref\_1:1}$”
Table 9-8/Page 9-8	Default output pad drive strength should be partial instead of full.
Table 9-8/Page 9-9	Footnote #2: Changed which pins do not affect reset configuration: “The D[31:26, 23:22, 18:17, 15:0] pins do not affect reset configuration.”
Table 12-1/Page 12-6	ERXER direction should be input, ETXEN direction should be output.
Table 12-10/Page 12-22	Change an erroneous TSIZ1 to TSIZ0 in the PAR_TSIZ0 entry.
Throughout Chapter 16	Replace instances of D[19:18] with D[20:19].
Figure 20-1/Page 20-2	Change value in divide by box to 4096 instead of 8192.
Figure 28-7/Page 28-15	Replace entries with “Bytes 5-7 + Parity” with “Bytes 5-8” to reduce confusion. The parity is included in the last bit of each byte, not the 8th byte.

3 Errata for Revision 1

Table 3. MCF5271RM Rev 1 Errata

Location	Description
Throughout	Core frequency has been improved and device is now available in 150MHz versions. Update all core frequency references from 100MHz to 150MHz and all internal bus frequencies from 50MHz to 75MHz.
Throughout	Remove overbar from DACK*n* signals, as they are not asserted low.
Throughout	Replace $\overline{\text{RSTI}}$ with $\overline{\text{RESET}}$ and $\overline{\text{RSTO}}$ with $\overline{\text{RSTOUT}}$.
Table 2-5/Page 2-9	Byte Strobes function column should say: “$\overline{\text{BS0}}$ controls access to the least significant byte lane of data, and $\overline{\text{BS3}}$ controls access to the most significant byte lane of data.” and also “Note that most SDRAMs associate DQM3 with the MSB, in which case $\overline{\text{BS3}}$ should be connected to the SDRAM's DQM3 input.”
Table 2-13/Page 2-15	Added entry in table for PSTCLK output signal. “PSTCLK indicates when the development system should sample PST and DDATA values.”
Figure 3-7/Page 3-18	The reset value of D1[DCSIZ] is 0x0 and the reset value of D1[RAM1SIZ] is 0x8. Table 3-11 is correct
Table 6-1/Page 6-3	In SPV bit field description, fix cross-reference to Section “Memory Base Address Register (RAMBAR)”. It should be Section 11.2.1.2 instead of 8.4.2.
Section 7.1.3.5/Page 7-6	The PLL cannot be stopped when the device enters stop mode. Remove paragraphs 3-6 and add in their place “During stop mode, the PLL continues to run. The external CLKOUT signal may be enabled or disabled when the device enters stop mode, depending on the LPCR[STPMD] bit settings. The external CLKOUT output pin may be disabled to lower power consumption via the SYNCR[DISCLK] bit. The external CLKOUT pin function is enabled by default at reset.”

Table 3. MCF5271RM Rev 1 Errata (continued)

Location	Description
Table 7-5/Page 7-9	The first equation in footnote #1 in the MFD bit description field is incorrect. It should be: "$f_{sys} = f_{ref} \times 2(MFD + 2)/2^{RFD}$" instead of $f_{sys/2}$.
Table 7-5/Page 7-9	The second equation in footnote #1 in the MFD bit description field is incorrect. It should be: "$f_{ref} \times 2(MFD + 2) \leq 150MHz$" instead 50MHz
Section 7.4.3/Page 7-15	First paragraph, the default core frequency is one and a half times the reference frequency after reset instead of two times the reference frequency. An MFD = 0b001 is 2x not 6x.
Table 7-11/Page 7-30	Delete 4th and 5th rows on this page, as the PLL cannot be disabled in stop mode.
Table 8-4/Page 8-4	The description of bits 2-0 is missing from the LPCR Field Description table. These should be included with the following description: "Reserved, should be cleared."
Section 8.3.2.3/Page 8-6	Corrected second paragraph since the core watchdog cannot reset the device. Second paragraph should read "When enabled, the core watchdog can bring the device out of low-power mode via a core watchdog interrupt. This system setup must meet the conditions specified in Section 8.3.1, "Low-Power Modes" for the core watchdog interrupt to bring the part out of low-power mode.
Section 8.3.2.16/Page 8-10	The PLL cannot be stopped when the device enters stop mode. Remove paragraphs 2-5 and add in their place "During stop mode, the PLL continues to run. The external CLKOUT signal may be enabled or disabled when the device enters stop mode, depending on the LPCR[STPMD] bit settings."
Table 9-1/Page 9-2	Reset config override signals should be D[25:24, 21:19, 16] instead of D[26:24, 21, 19:16].
Section 9.2.3/Page 9-3	Section title should be "D[25:24, 21:19, 16]..." instead of "D[26:24, 21, 19:16]..."
Figure 9-3/Page 9-5	Unreserved RCON register bits should be read only.
Table 9-7/Page 9-8	Reset config override signals should be D[25:24, 21:19, 16] instead of D[26:24, 21, 19:16].
Table 9-8/Page 9-8	Chip mode heading should be D16 only, since D26 & D17 have no affect on the selected chip mode. Master mode (default) is selected by asserting D16. Deasserting D16 during $\overline{\text{RCON}}$ assertion at reset places the device in a reserved mode.
Table 9-8/Page 9-8	Remove "RCON[2]=0" in boot device default configuration field.
Table 9-8/Page 9-9	Remove "RCON[7:6]=10" from clock mode default configuration field. Footnote 5 added: "There is no default configuration for clock mode selection. The actual values for the CLKMOD pins must always be driven during reset. Once out of reset, the CLKMOD pins have no effect on the clock mode selection."
Table 9-8/Page 9-9	"Chip select configuration" entry for setting D[25:24]=11, should read "PADDR[7:5] = $\overline{\text{CS}}$[6:4]" instead of "PADDR[7:6] = $\overline{\text{CS}}$[6:4]"
Table 9-8/Page 9-9	Footnote #2: Changed which pins do not affect reset configuration: "The D[31:26, 23:22, 20:17, 15:0] pins do not affect reset configuration."
Section 9.4.2/Page 9-9	The MODE field is in the RCON register instead of the CCR.
Table 9-9/Page 9-9	Remove MODE[2] and MODE[1] columns since the MODE field is only one bit wide and also D26 and D17 have no affect on chip configuration mode selection.
Figure 14-9/Page 14-17	DACK*n* is only asserted for a single clock cycle. All other signals (TS, CS, TA, R/$\overline{\text{W}}$, and A[23:0] are subsequently moved one cycle sooner.
Section 16.2.1/Page 16-1	An overbar should be placed over the CS[7:0] in the section heading. The last sentence should read: "Port size for $\overline{\text{CS0}}$ is configured by the logic levels of D[20:19] when $\overline{\text{RSTOUT}}$ negates and $\overline{\text{RCON}}$ is asserted."

Table 3. MCF5271RM Rev 1 Errata (continued)

Location	Description
Table 16-6/Page 16-9	In the CSMR*n*[BAM] bit description, the first example BAM bit setting is incorrect. Change from 0x0008 to 0x0001.
Section 18.3.4.1/Page 18-10	Add Note “Because the device has 24 external address lines, the maximum SDRAM address size is 128 Mbits.”
Chapter 19	The maximum buffer size of the FEC is 2032 bytes. Replace all instances of 2047 with 2032. R_BUF_SIZE is at bit position 10:4 in the EMRBR register. Therefore the maximum setting is $7F0 which equals 2032.
Figure 19-24/Page 19-28	Change EMRBR register address to “IPSBAR + 0x1188” instead of “IPSBAR +0x11B8”.
Table 22-3/Page 22-6	The MODE16 bit field description should read: “Selects the increment mode for the timer. MODE16 = 1 is intended to exercise the upper bits of the 32-bit timer in diagnostic software without requiring the timer to count through its entire dynamic range. When set, the counter’s upper 16 bits mirror its lower 16 bits. All 32 bits of the counter are still compared to the reference value.”
Figure 24-17/Page 24-18	Remove 16-bit divider blocks from both timer inputs, as it is not available when using an external clock source.
Section 24.4.1.2.2/Page 24-19	Change equation to: Baudrate = f_{extc}/(16 or 1), since the 16-bit divider is not available when using an external clock source.
Section 26.4.1/Page 26-15	Swap steps 4 & 5 and change “...(without padding) in bits” to “...(without padding) in bytes”.
Section 26.4.2.1/Page 26-16	Swap steps 4 & 5.
Section 26.4.2.2/Page 26-16	Swap steps 4 & 5.
Section 26.4.2.3/Page 26-17	Swap steps 8 & 9.
Section 26.4.3/Page 26-18	Swap steps 8 & 9.
Section 26.4.4/Page 26-18	Swap steps 6 & 7.
Section 26.4.5/Page 26-18	Swap steps 7 & 8.
Figure 28-8/Page 28-7	Change SKMR[CTRM] bit field to straddle bits 11–8.
Table 28-2/Page 28-8	Change the first 4 SKMR bit fields bit numbers to 31–12, 11–8, 7, & 6–5.
Section 28.3.1/Page 28-19	Remove last sentence of section, as this refers to internal logic only.
Section 28.4.1/Page 28-20	Swap steps 9 & 10.
Section 28.4.2/Page 28-20	Swap steps 9 & 10. Swap steps 23 & 24.
Table 30-1/Page 30-2	Change CLKOUT to PSTCLK.
Figure 30-2/Page 30-2	Change CLKOUT to PSTCLK.
Figure 30-41/Page 30-48	Change pin 24 from CLKOUT to PSTCLK.

4 Revision History

Table 4 provides a revision history for this document.

Table 4. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	• Initial release.	11/2004
1.1	• Added D1 reset value errata. • Added FEC max buffer size errata.	01/2005
1.2	• Added FEC EMRBR address errata.	03/2005
1.3	• Added core & internal bus frequency improvement. • Added $\overline{\text{RSTI}}$/$\overline{\text{RSTO}}$ errata. • Added multiple PSTCLK errata. • Added SPV bit field cross-reference errata. • Added multiple errata regarding the PLL unable to be stopped during stop mode. • Added MFD bit field errata. • Added Section 7.4.3 default core frequency errata. • Added core watchdog reset errata. • Added chip select configuration entry errata. • Added CSMR*n*[BAM] example errata. • Added SDRAM address line note errata. • Added DMA Timer MODE16 bit errata. • Added MDHA & SKHA application examples errata. • Added the SKMR[CTRM] bit field errata.	04/2005
The below errata were added for MCF5271RM Revision 1.1		
1.4	• Added PAR_TSIZ0 errata. • Added D[19:18]->D[20:19] errata. • Corrected previous errata with Table 9-8, Footnote #2	07/2005
1.5	• Added ERXER and ETXER direction errata in Chapter 2 and 12. • Added default output pad drive strength • Added Table 7-3 footnote errata. • Added SKHA parity errata. • Added UART external clock source, 16-bit divider errata.	08/2005
1.6	• Added watchdog timer divide-by value errata.	07/2006
The below errata were added for MCF5271RM Revision 2		
2	• Added QSPI_CS/SD_CKE pin location errata. • Added DT3IN/DT3OUT alternate 2 functionality errata.	08/2006

Table 4. Revision History Table (continued)

Rev. Number	Substantive Changes	Date of Release
2.1	• Added RMON_R_DROP counter errata.	11/2006
2.2	• Added various core, EMAC, cache, SRAM and debug chapter errata. • Added CLKIN to CLKOUT errata. • Added FEC MIB counter memory map errata. • Added “Duplicate Frame Transmission” section to FEC chapter. • Added DACR*n*[CBM] field description note. • Added secondary wait state timing diagram errata. • Added SKMR[CTRM,DKP] errata. • Added CIM/CCM errata. • Added multiple INTC1 errata. • Added EPDDR figure errata. • Added DMA figure errata. • Added DMA external request and acknowledge operation section errata. • Added DMA SAA bit errata. • Added interrupt level/priority table. • Added IPSBAR note in SCM chapter. • Added global IACK space errata.	05/2007

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Rev. 2.2
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