MC68HC11F1RG/AD
REV 2

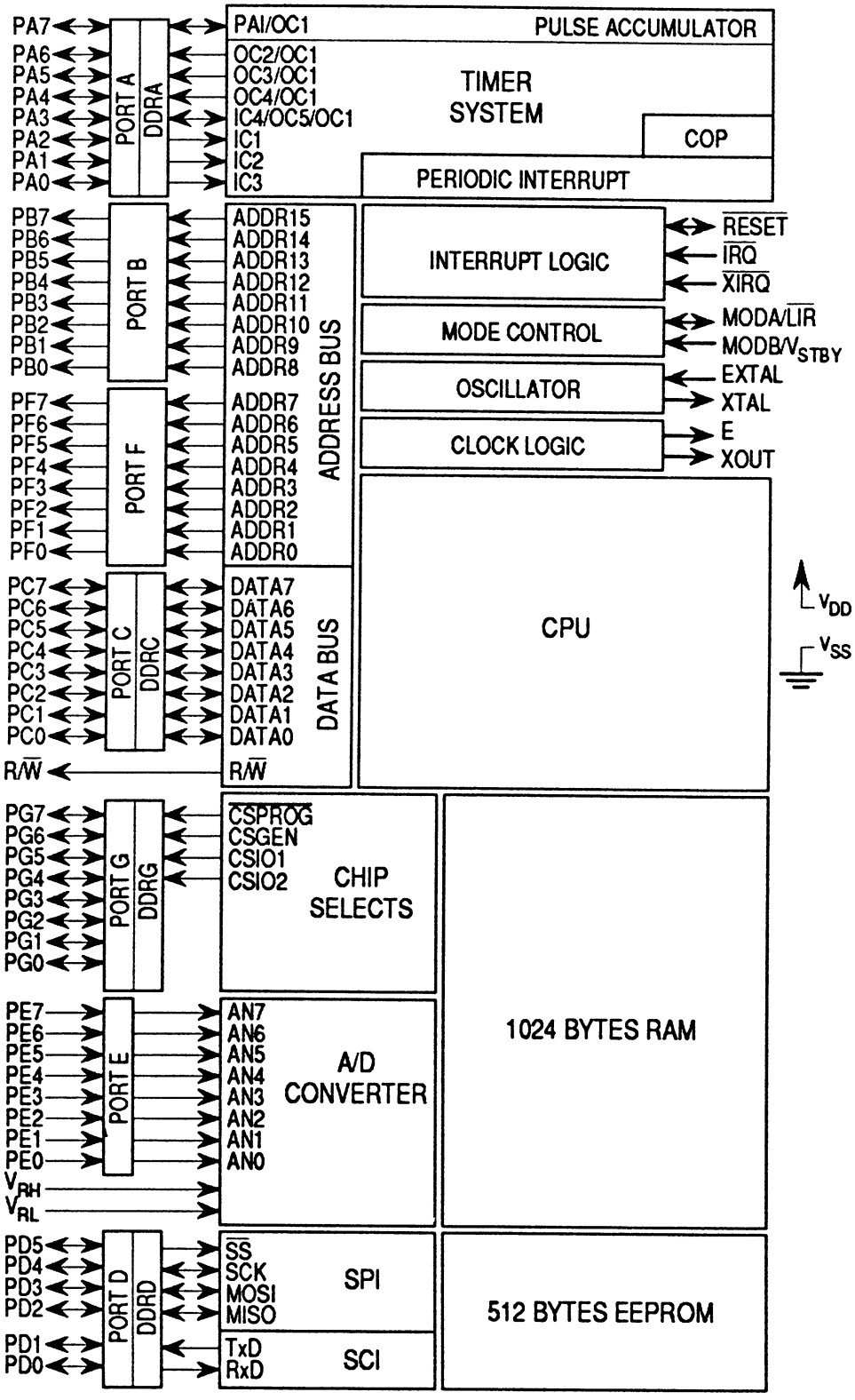
HC11

MC68HC11F1

PROGRAMMING REFERENCE GUIDE

MOTOROLA

Block Diagram



PROGRAMMING MODEL
CRYSTAL DEPENDENT TIMING
INTERRUPTS

MEMORY MAP
OPCODE MAPS

INSTRUCTIONS
ADDRESSING MODES
EXECUTION TIMES
SPECIAL OPERATIONS

REGISTER AND
CONTROL BIT
ASSIGNMENTS

MECHANICAL DATA
HEX/DEC CONVERSION
ASCII CHART

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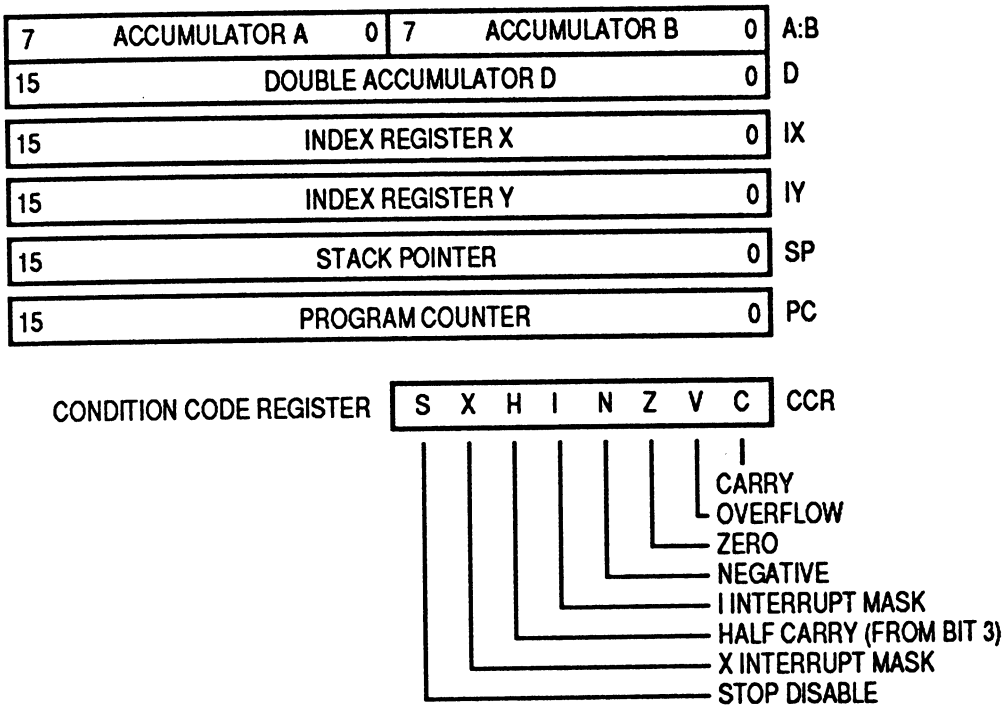
MC68HC11F1 Programming Model



Crystal Dependent Timer Summary

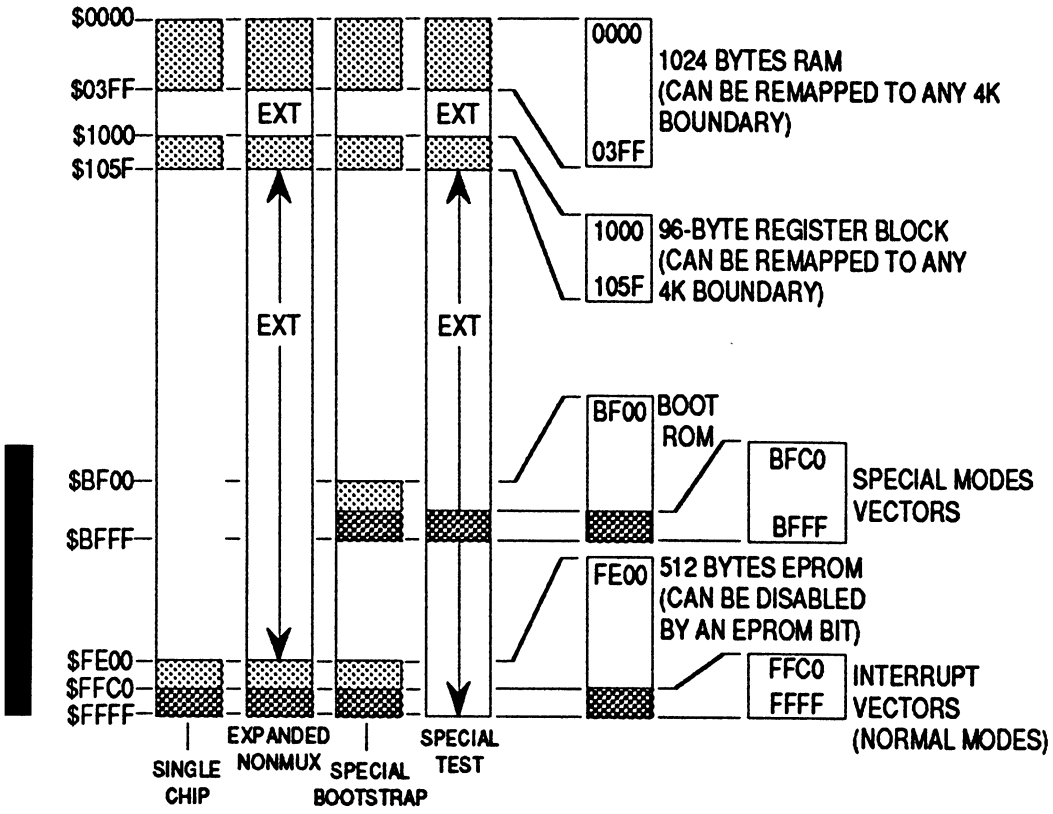
	Selected Crystal	Common XTAL Frequencies		
		8.0 MHz	12.0 MHz	16.0 MHz
CPU Clock	(E)	2.0 MHz	3.0 MHz	4.0 MHz
Cycle Time	(1/E)	500 ns	333 ns	250 ns
	Pulse Accumulator (in Gated Mode)			
($E/2^6$) ($E/2^{14}$)	1 count — overflow —	32.0 µs 8.192 ms	21.330 µs 5.461 ms	16.0 µs 4.096 ms
	PR[1:0]	Main Timer Count Rates		
(E/1) ($E/2^{16}$)	0 0 1 count — overflow —	500 ns 32.768 ms	333 ns 21.845 ms	250 ns 16.384 ms
(E/4) ($E/2^{18}$)	0 1 1 count — overflow —	2.0 µs 131.07 ms	1.333 µs 87.381 ms	1.0 µs 65.536 ms
(E/8) ($E/2^{19}$)	1 0 1 count — overflow —	4.0 µs 262.14 ms	2.667 µs 174.76 ms	2.0 µs 131.07 ms
(E/16) ($E/2^{20}$)	1 1 1 count — overflow —	8.0 µs 524.29 ms	5.333 µs 349.52 ms	4.0 µs 262.14 ms
	RTR[1:0]	Periodic (RTI) Interrupt Rates		
($E/2^{13}$)	0 0	4.096 ms	2.731 ms	2.048 ms
($E/2^{14}$)	0 1	8.192 ms	5.461 ms	4.096 ms
($E/2^{15}$)	1 0	16.384 ms	10.923 ms	8.192 ms
($E/2^{16}$)	1 1	32.768 ms	21.845 ms	16.384 ms
	CR[1:0]	COP Watchdog Timeout Rates		
($E/2^{15}$)	0 0	16.384 ms	10.923 ms	8.192 ms
($E/2^{17}$)	0 1	65.536 ms	43.691 ms	32.768 ms
($E/2^{19}$)	1 0	262.14 ms	174.76 ms	131.07 ms
($E/2^{21}$)	1 1	1.049 s	699.05 ms	5024.28 ms
($E/2^{15}$)	Timeout Tolerance (– 0 ms/+...)	16.4 ms	10.9 ms	8.192 ms

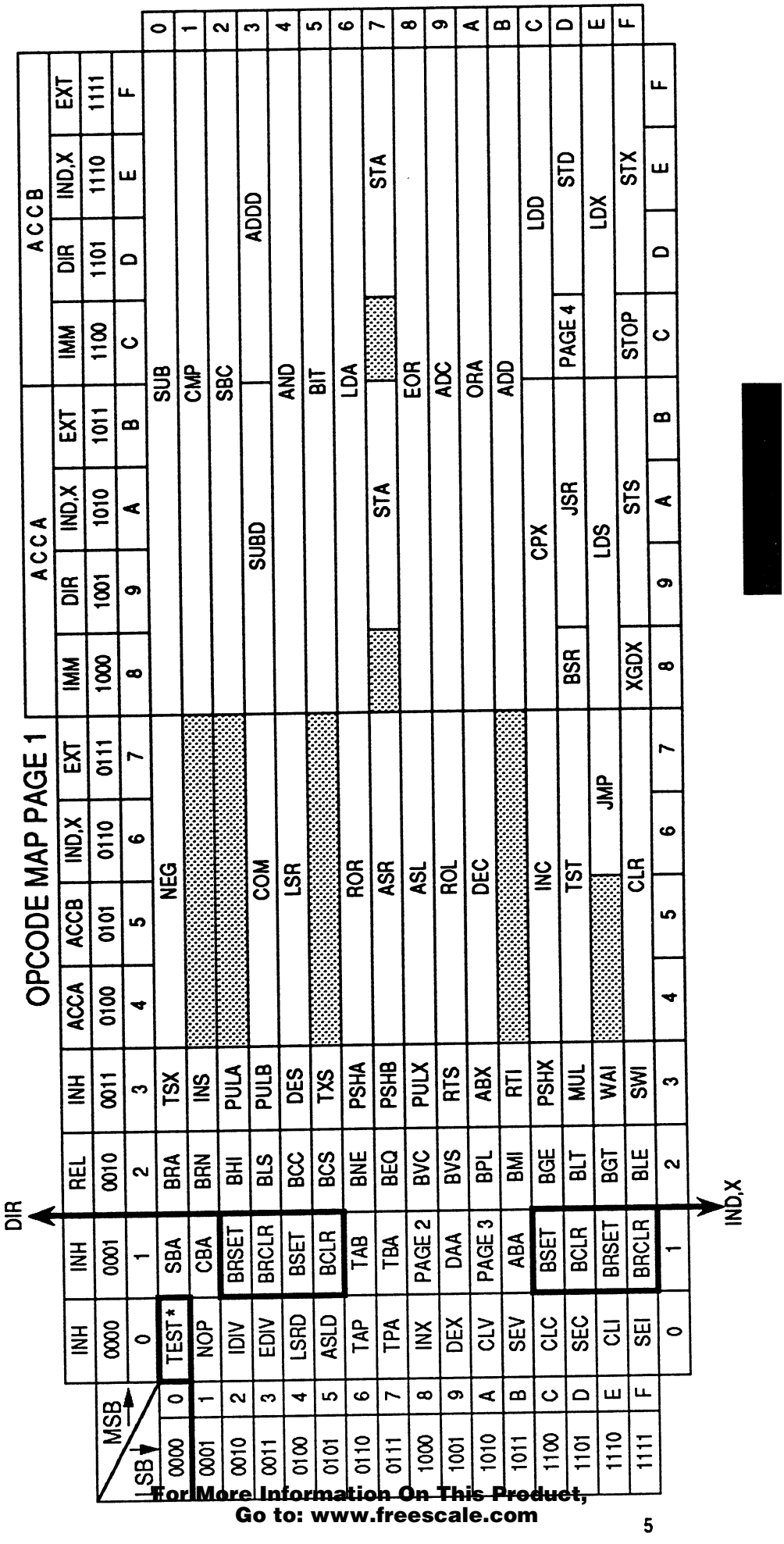
Interrupt Vector Assignments

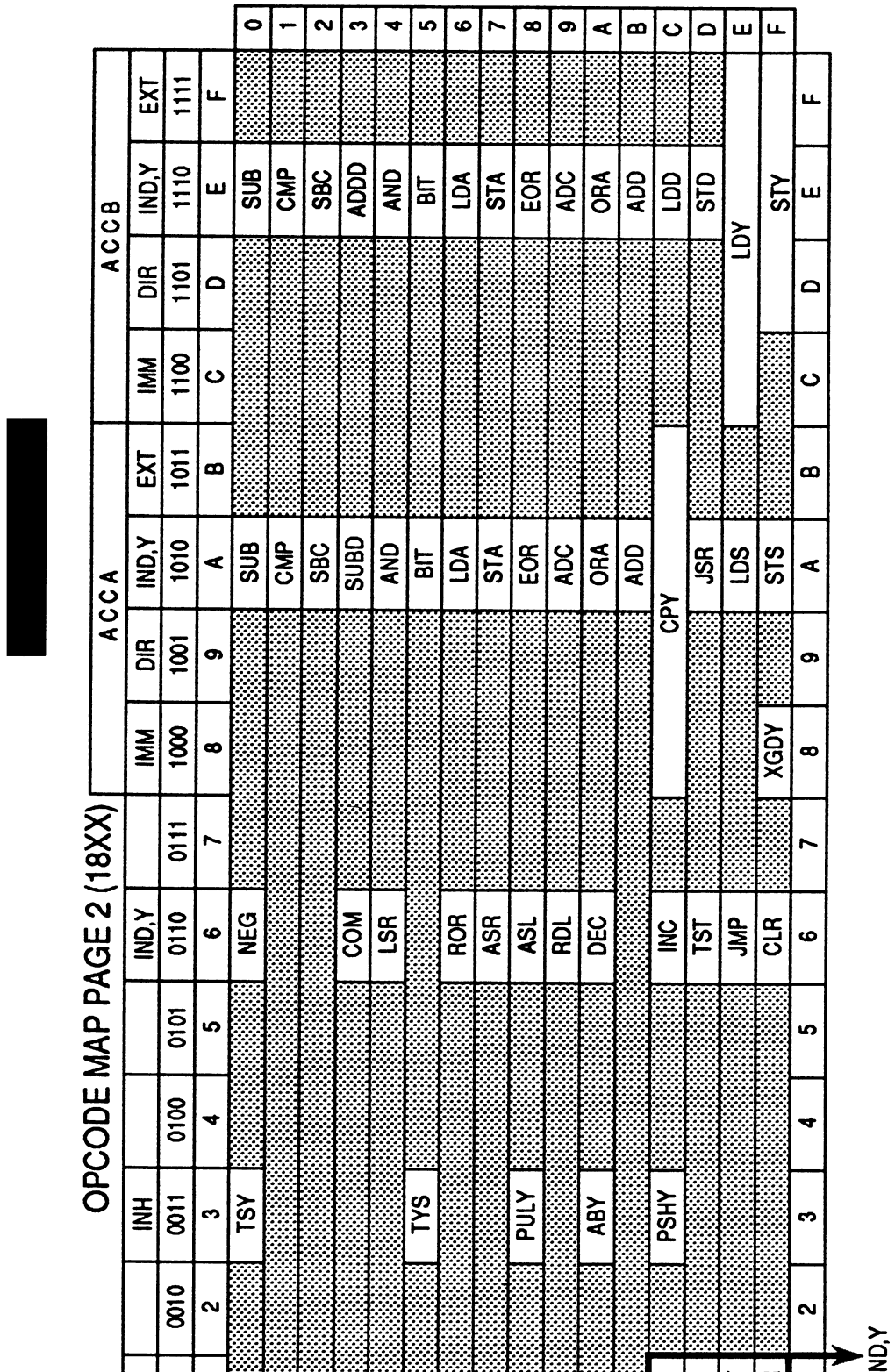
Vector Address	Interrupt Source	CCR Mask Bit	Local Mask
FFC0, C1 – FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System*	I	
	• SCI Receive Data Register Full		RIE
	• SCI Receiver Overrun		RIE
	• SCI Transmit Data Register Empty		TIE
	• SCI Transmit Complete		TCIE
	• SCI Idle Line Detect		ILIE
FFD8, D9	SPI Serial Transfer Complete	I	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I	PAII
FFDC, DD	Pulse Accumulator Overflow	I	PAOVI
FFDE, DF	Timer Overflow	I	TOI
FFE0, E1	Timer Input Capture 4/ Output Compare 5	I	I4/O5I
FFE2, E3	Timer Output Compare 4	I	OC4I
FFE4, E5	Timer Output Compare 3	I	OC3I
FFE6, E7	Timer Output Compare 2	I	OC2I
FFE8, E9	Timer Output Compare 1	I	OC1I
FFEA, EB	Timer Input Capture 3	I	IC3I
FFEC, ED	Timer Input Capture 2	I	IC2I
FFEE, EF	Timer Input Capture 1	I	IC1I
FFF0, F1	Real-Time Interrupt	I	RTII
FFF2, F3	$\overline{\text{IRQ}}$ (External Pin)	I	None
FFF4, F5	$\overline{\text{XIRQ}}$ Pin	X	None
FFF6, F7	Software Interrupt	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure	None	NOCOP
FFFC, FD	Clock Monitor Fail	None	CME
FFFE, FF	$\overline{\text{RESET}}$	None	None

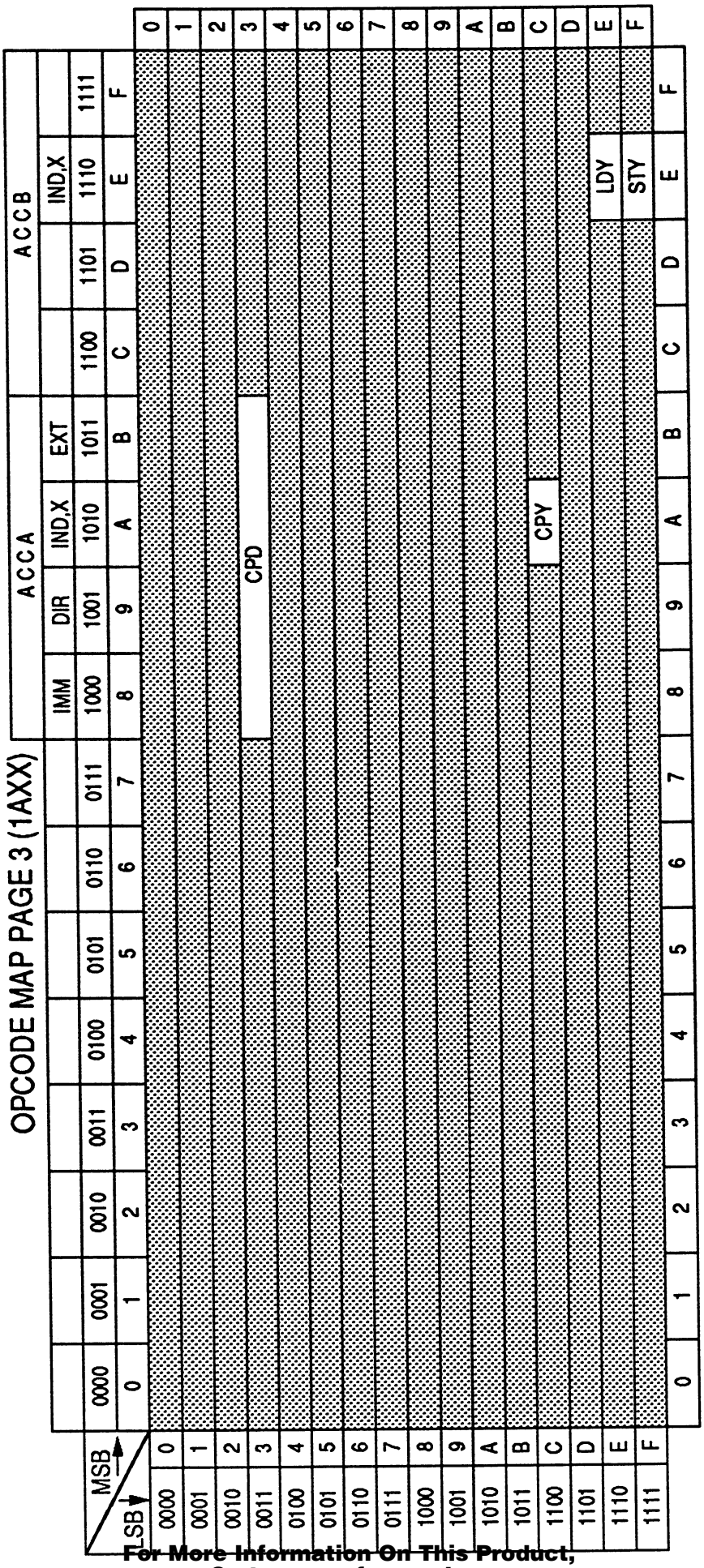
*Interrupts generated by SCI; read SCSR to determine source

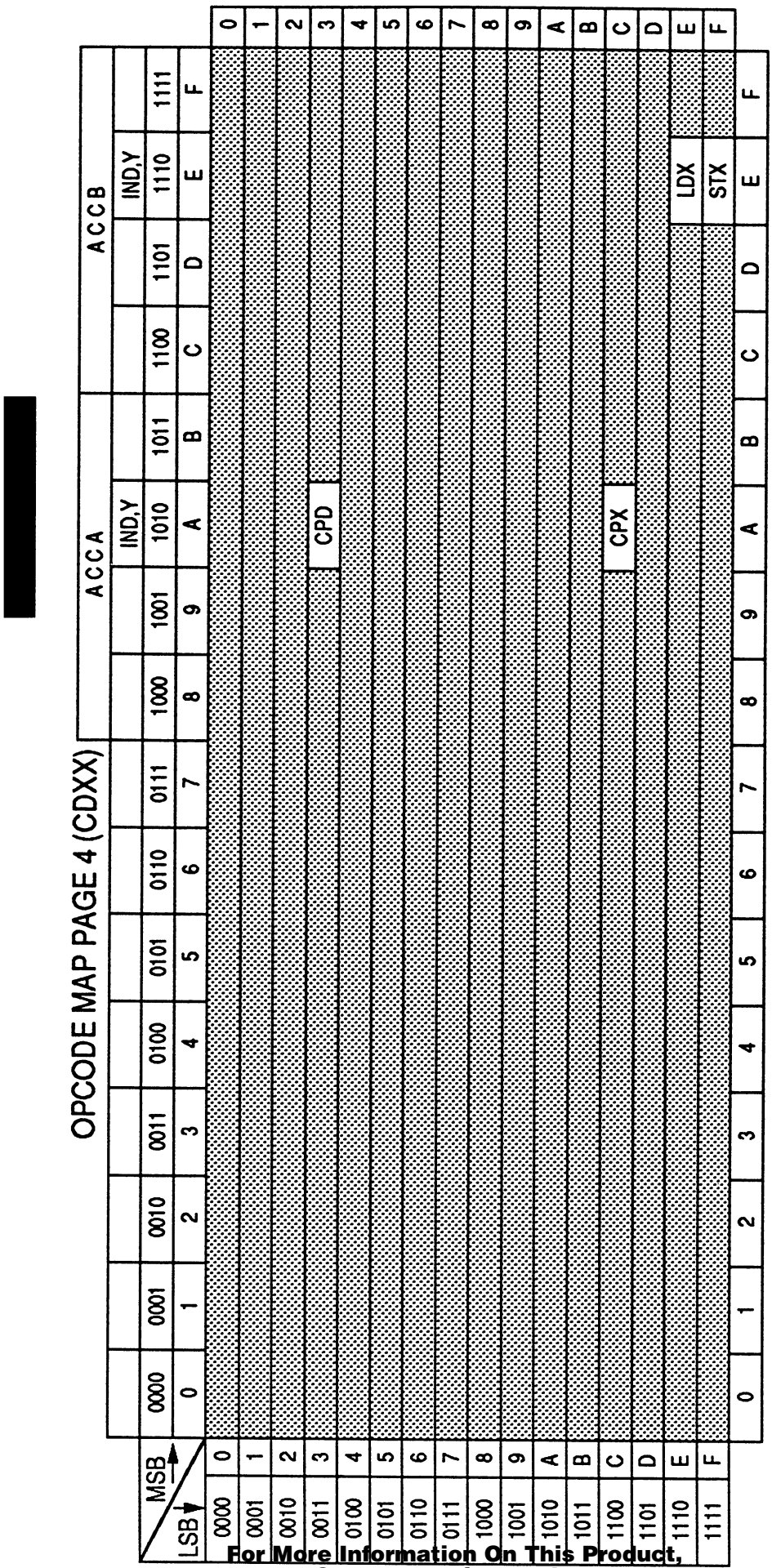
MC68HC11F1 Memory Map











Simple Branches		
Mnemonic	Opcode	Cycles
BRA	20	3
BRN	21	3
BSR	8D	7

Simple Conditional Branches				
	True		False	
Test	Instruction	Opcode	Instruction	Opcode
N = 1	BMI	2B	BPL	2A
Z = 1	BEQ	27	BNE	26
V = 1	BVS	29	BVC	28
C = 1	BCS	25	BCC	24

Signed Conditional Branches				
	True		False	
Test	Instruction	Opcode	Instruction	Opcode
r > m	BGT	2E	BLE	2F
r ≥ m	BGE	2C	BLT	2D
r = m	BEQ	27	BNE	26
r ≤ m	BLE	2F	BGT	2E
r < m	BLT	2D	BGE	2C

Unsigned Conditional Branches				
	True		False	
Test	Instruction	Opcode	Instruction	Opcode
r > m	BHI	22	BLS	23
r ≥ m	BHS/BCC	24	BLO/BCS	25
r = m	BEQ	27	BNE	26
r ≤ m	BLS	23	BHI	22
r < m	BLO/BCS	25	BHS/BCC	24

Bit Manipulation Branches
BRCLR — Branch if all selected bits are clear (opcode) (operand addr) (mask) (rel offset) M • mm = 0? M = operand in memory; mm = mask
BRSET — Branch if all selected bits are set (opcode) (operand addr) (rel offset) ($\overline{M}$) • mm = 0? M = operand in memory; mm = mask

Opcode vs Instruction Cross Reference

Opcode	Operands	Instruction	ADDR Mode	Cycle
00		TEST	INH	—
01		NOP	INH	2
02		IDIV	INH	41
03		FDIV	INH	41
04		LSRD	INH	3
05		ASLD/LSLD	INH	3
06		TAP	INH	2
07		TPA	INH	2
08		INX	INH	3
09		DEX	INH	3
0A		CLV	INH	2
0B		SEV	INH	2
0C		CLC	INH	2
0D		SEC	INH	2
0E		CLI	INH	2
0F		SEI	INH	2
10		SBA	INH	2
11		CBA	INH	2
12	dd mm rr	BRSET (opr) (msk) (rel)	DIR	6
13	dd mm rr	BRCLR (opr) (msk) (rel)	DIR	6
14	dd mm	BSET (opr) (msk)	DIR	6
15	dd mm	BCLR (opr) (msk)	DIR	6
16		TAB	INH	2
17		TBA	INH	2
18		(Page 2 Switch)		
19		DAA	INH	2
1A		(Page 3 Switch)		
1B		ABA	INH	2
1C	ff mm	BSET (opr) (msk)	IND,X	7
1D	ff mm	BCLR (opr) (msk)	IND,X	7
1E	ff mm rr	BRSET (opr) (msk) (rel)	IND,X	7
1F	ff mm rr	BRCLR (opr) (msk) (rel)	IND,X	7

Opcode vs Instruction Cross Reference

Opcode	Operands	Instruction	ADDR Mode	Cycle
20	rr	BRA (rel)	REL	3
21	rr	BRN (rel)	REL	3
22	rr	BHI (rel)	REL	3
23	rr	BLS (rel)	REL	3
24	rr	BCC/BHS (rel)	REL	3
25	rr	BCS/BLO (rel)	REL	3
26	rr	BNE (rel)	REL	3
27	rr	BEQ (rel)	REL	3
28	rr	BVC (rel)	REL	3
29	rr	BVS (rel)	REL	3
2A	rr	BPL (rel)	REL	3
2B	rr	BMI (rel)	REL	3
2C	rr	BGE (rel)	REL	3
2D	rr	BLT (rel)	REL	3
2E	rr	BGT (rel)	REL	3
2F	rr	BLE (rel)	REL	3
30		TSX	INH	3
31		INS	INH	3
32		PULA	INH	4
33		PULB	INH	4
34		DES	INH	3
35		TXS	INH	3
36		PSHA	INH	3
37		PSHB	INH	3
38		PULX	INH	5
39		RTS	INH	5
3A		ABX	INH	3
3B		RTI	INH	12
3C		PSHX	INH	4
3D		MUL	INH	10
3E		WAI	INH	14
3F		SWI	INH	14
40		NEGA	INH	2
43		COMA	INH	2
44		LSRA	INH	2
46		RORA	INH	2
47		ASRA	INH	2
48		ASLA/LSLA	INH	2
49		ROLA	INH	2
4A		DECA	INH	2
4C		INCA	INH	2
4D		TSTA	INH	2
4F		CLRA	INH	2
50		NEGB	INH	2

Opcode vs Instruction Cross Reference

Opcode	Operands	Instruction	ADDR Mode	Cycle
53		COMB	INH	2
54		LSRB	INH	2
56		RORB	INH	2
57		ASRB/ASLB	INH	2
58		LSLB	INH	2
59		ROLB	INH	2
5A		DECB	INH	2
5C		INCB	INH	2
5D		TSTB	INH	2
5F		CLRB	INH	2
60	ff	NEG (opr)	IND,X	6
63	ff	COM (opr)	IND,X	6
64	ff	LSR (opr)	IND,X	6
66	ff	ROR (opr)	IND,X	6
67	ff	ASR (opr)	IND,X	6
68	ff	ASL/LSL (opr)	IND,X	6
69	ff	ROL (opr)	IND,X	6
6A	ff	DEC (opr)	IND,X	6
6C	ff	INC (opr)	IND,X	6
6D	ff	TST (opr)	IND,X	6
6E	ff	JMP (opr)	IND,X	3
6F	ff	CLR (opr)	IND,X	6
70	hh ll	NEG (opr)	EXT	6
73	hh ll	COM (opr)	EXT	6
74	hh ll	LSR (opr)	EXT	6
76	hh ll	ROR (opr)	EXT	6
77	hh ll	ASR (opr)	EXT	6
78	hh ll	ASL/LSL (opr)	EXT	6
79	hh ll	ROL (opr)	EXT	6
7A	hh ll	DEC (opr)	EXT	6
7C	hh ll	INC (opr)	EXT	6
7D	hh ll	TST (opr)	EXT	6
7E	hh ll	JMP (opr)	EXT	3
7F	hh ll	CLR (opr)	EXT	6
80	ii	SUBA (opr)	IMM	2
81	ii	CMPA (opr)	IMM	2
82	ii	SBCA (opr)	IMM	2
83	jj kk	SUBD (opr)	IMM	4
84	ii	ANDA (opr)	IMM	2
85	ii	BITA (opr)	IMM	2
86	ii	LDAA (opr)	IMM	2
88	ii	EORA (opr)	IMM	2
89	ii	ADCA (opr)	IMM	2
8A	ii	ORAA (opr)	IMM	2

Opcode vs Instruction Cross Reference

Opcode	Operands	Instruction	ADDR Mode	Cycle
8B	ii	ADDA (opr)	IMM	2
8C	jj kk	CPX (opr)	IMM	4
8D	rr	BSR (rel)	REL	6
8E	jj kk	LDS (opr)	IMM	3
8F		XGDX	INH	3
90	dd	SUBA (opr)	DIR	3
91	dd	CMPA (opr)	DIR	3
92	dd	SBCA (opr)	DIR	3
93	dd	SUBD (opr)	DIR	5
94	dd	ANDA (opr)	DIR	3
95	dd	BITA (opr)	DIR	3
96	dd	LDAA (opr)	DIR	3
97	dd	STAA (opr)	DIR	3
98	dd	EORA (opr)	DIR	3
99	dd	ADCA (opr)	DIR	3
9A	dd	ORAA (opr)	DIR	3
9B	dd	ADDA (opr)	DIR	3
9C	dd	CPX (opr)	DIR	5
9D	dd	JSR (opr)	DIR	5
9E	dd	LDS (opr)	DIR	4
9F	dd	STS (opr)	DIR	4
A0	ff	SUBA (opr)	IND,X	4
A1	ff	CMPA (opr)	IND,X	4
A2	ff	SBCA (opr)	IND,X	4
A3	ff	SUBD (opr)	IND,X	6
A4	ff	ANDA (opr)	IND,X	4
A5	ff	BITA (opr)	IND,X	4
A6	ff	LDAA (opr)	IND,X	4
A7	ff	STAA (opr)	IND,X	4
A8	ff	EORA (opr)	IND,X	4
A9	ff	ADCA (opr)	IND,X	4
AA	ff	ORAA (opr)	IND,X	4
AB	ff	ADDA (opr)	IND,X	4
AC	ff	CPX (opr)	IND,X	6
AD	ff	JSR (opr)	IND,X	6
AE	ff	LDS (opr)	IND,X	5
AF	ff	STS (opr)	IND,X	5
B0	hh ll	SUBA (opr)	EXT	4
B1	hh ll	CMPA (opr)	EXT	4
B2	hh ll	SBCA (opr)	EXT	4
B3	hh ll	SUBD (opr)	EXT	6
B4	hh ll	ANDA (opr)	EXT	4
B5	hh ll	BITA (opr)	EXT	4
B6	hh ll	LDAA (opr)	EXT	4

Opcode vs Instruction Cross Reference

Opcode	Operands	Instruction	ADDR Mode	Cycle
B7	hh ll	STAA (opr)	EXT	4
B8	hh ll	EORA (opr)	EXT	4
B9	hh ll	ADCA (opr)	EXT	4
BA	hh ll	ORAA (opr)	EXT	4
BB	hh ll	ADDA (opr)	EXT	4
BC	hh ll	CPX (opr)	EXT	6
BD	hh ll	JSR (opr)	EXT	6
BE	hh ll	LDS (opr)	EXT	5
BF	hh ll	STS (opr)	EXT	5
C0	ii	SUBB (opr)	IMM	2
C1	ii	CMPB (opr)	IMM	2
C2	ii	SBCB (opr)	IMM	2
C3	jj kk	ADDD (opr)	IMM	4
C4	ii	ANDB (opr)	IMM	2
C5	ii	BITB (opr)	IMM	2
C6	ii	LDAB (opr)	IMM	2
C8	ii	EORB (opr)	IMM	2
C9	ii	ADCB (opr)	IMM	2
CA	ii	ORAB (opr)	IMM	2
CB	ii	ADDB (opr)	IMM	2
CC	jj kk	LDD (opr)	IMM	3
CD		(Page 4 Switch)		
CE	jj kk	LDX (opr)	IMM	3
CF		STOP	INH	2
D0	dd	SUBB (opr)	DIR	3
D1	dd	CMPB (opr)	DIR	3
D2	dd	SBCB (opr)	DIR	3
D3	dd	ADDD (opr)	DIR	5
D4	dd	ANDB (opr)	DIR	3
D5	dd	BITB (opr)	DIR	3
D6	dd	LDAB (opr)	DIR	3
D7	dd	STAB (opr)	DIR	3
D8	dd	EORB (opr)	DIR	3
D9	dd	ADCB (opr)	DIR	3
DA	dd	ORAB (opr)	DIR	3
DB	dd	ADDB (opr)	DIR	3
DC	dd	LDD (opr)	DIR	4
DD	dd	STD (opr)	DIR	4
DE	dd	LDX (opr)	DIR	4
DF	dd	STX (opr)	DIR	4
E0	ff	SUBB (opr)	IND,X	4
E1	ff	CMPB (opr)	IND,X	4
E2	ff	SBCB (opr)	IND,X	4
E3	ff	ADDD (opr)	IND,X	6

Opcode vs Instruction Cross Reference

Opcode	Operands	Instruction		ADDR Mode	Cycle
E4	ff	ANDB	(opr)	IND,X	4
E5	ff	BITB	(opr)	IND,X	4
E6	ff	LDAB	(opr)	IND,X	4
E7	ff	STAB	(opr)	IND,X	4
E8	ff	EORB	(opr)	IND,X	4
E9	ff	ADCB	(opr)	IND,X	4
EA	ff	ORAB	(opr)	IND,X	4
EB	ff	ADDB	(opr)	IND,X	4
EC	ff	LDD	(opr)	IND,X	5
ED	ff	STD	(opr)	IND,X	5
EE	ff	LDX	(opr)	IND,X	5
EF	ff	STX	(opr)	IND,X	5
F0	hh ll	SUBB	(opr)	EXT	4
F1	hh ll	CMPB	(opr)	EXT	4
F2	hh ll	SBCB	(opr)	EXT	4
F3	hh ll	ADDD	(opr)	EXT	6
F4	hh ll	ANDB	(opr)	EXT	4
F5	hh ll	BITB	(opr)	EXT	4
F6	hh ll	LDAB	(opr)	EXT	4
F7	hh ll	STAB	(opr)	EXT	4
F8	hh ll	EORB	(opr)	EXT	4
F9	hh ll	ADCB	(opr)	EXT	4
FA	hh ll	ORAB	(opr)	EXT	4
FB	hh ll	ADDB	(opr)	EXT	4
FC	hh ll	LDD	(opr)	EXT	5
FD	hh ll	STD	(opr)	EXT	5
FE	hh ll	LDX	(opr)	EXT	5
FF	hh ll	STX	(opr)	EXT	5
18 08		INY		INH	4
18 09		DEY		INH	4
18 1C	ff mm	BSET	(opr) (msk)	IND,Y	8
18 1D	ff mm	BCLR	(opr) (msk)	IND,Y	8
18 1E	ff mm rr	BRSET	(opr) (msk) (rel)	IND,Y	8
18 1F	ff mm rr	BRCLR	(opr) (msk) (rel)	IND,Y	8
18 30		TSY		INH	4
18 35		TYS		INH	4
18 38		PULY		INH	6
18 3A		ABY		INH	4

Opcode vs Instruction Cross Reference

Opcode	Operands	Instruction	ADDR Mode	Cycle
18 3C		PSHY	INH	5
18 60	ff	NEG (opr)	IND,Y	7
18 63	ff	COM (opr)	IND,Y	7
18 64	ff	LSR (opr)	IND,Y	7
18 66	ff	ROR (opr)	IND,Y	7
18 67	ff	ASR (opr)	IND,Y	7
18 68	ff	ASL/LSL (opr)	IND,Y	7
18 69	ff	ROL (opr)	IND,Y	7
18 6A	ff	DEC (opr)	IND,Y	7
18 6C	ff	INC (opr)	IND,Y	7
18 6D	ff	TST (opr)	IND,Y	7
18 6E	ff	JMP (opr)	IND,Y	4
18 6F	ff	CLR (opr)	IND,Y	7
18 8C	jj kk	CPY (opr)	IMM	5
18 8F		XGDY	INH	4
18 9C	dd	CPY (opr)	DIR	6
18 A0	ff	SUBA (opr)	IND,Y	5
18 A1	ff	CMPA (opr)	IND,Y	5
18 A2	ff	SBCA (opr)	IND,Y	5
18 A3	ff	SUBD (opr)	IND,Y	7
18 A4	ff	ANDA (opr)	IND,Y	5
18 A5	ff	BITA (opr)	IND,Y	5
18 A6	ff	LDAA (opr)	IND,Y	5
18 A7	ff	STAA (opr)	IND,Y	5
18 A8	ff	EORA (opr)	IND,Y	5
18 A9	ff	ADCA (opr)	IND,Y	5
18 AA	ff	ORAA (opr)	IND,Y	5
18 AB	ff	ADDA (opr)	IND,Y	5
18 AC	ff	CPY (opr)	IND,Y	7
18 AD	ff	JSR (opr)	IND,Y	7
18 AE	ff	LDS (opr)	IND,Y	6
18 AF	ff	STS (opr)	IND,Y	6
18 BC	hh ll	CPY (opr)	EXT	7
18 CE	jj kk	LDY (opr)	IMM	4
18 DE	dd	LDY (opr)	DIR	5
18 DF	dd	STY (opr)	DIR	5
18 E0	ff	SUBB (opr)	IND,Y	5
18 E1	ff	CMPB (opr)	IND,Y	5
18 E2	ff	SBCB (opr)	IND,Y	5
18 E3	ff	ADDD (opr)	IND,Y	5
18 E4	ff	ANDB (opr)	IND,Y	5
18 E5	ff	BITB (opr)	IND,Y	5
18 E6	ff	LDAB (opr)	IND,Y	5
18 E7	ff	STAB (opr)	IND,Y	5

Opcode vs Instruction Cross Reference

Opcode	Operands	Instruction	ADDR Mode	Cycle
18 E8	ff	EORB (opr)	IND,Y	5
18 E9	ff	ADCB (opr)	IND,Y	5
18 EA	ff	ORAB (opr)	IND,Y	5
18 EB	ff	ADDB (opr)	IND,Y	5
18 EC	ff	LDD (opr)	IND,Y	6
18 ED	ff	STD (opr)	IND,Y	6
18 EE	ff	LDY (opr)	IND,Y	6
18 EF	ff	STY (opr)	IND,Y	6
18 FE	hh ll	LDY (opr)	EXT	6
18 FF	hh ll	STY (opr)	EXT	6
1A 83	jj kk	CPD (opr)	IMM	5
1A 93	dd	CPD (opr)	DIR	6
1A A3	ff	CPD (opr)	IND,X	7
1A AC	ff	CPY (opr)	IND,X	7
1A B3	hh ll	CPD (opr)	EXT	7
1A EE	ff	LDY (opr)	IND,X	6
1A EF	ff	STY (opr)	IND,X	6
CD A3	ff	CPD (opr)	IND,Y	7
CD AC	ff	CPX (opr)	IND,Y	7
CD EE	ff	LDX (opr)	IND,Y	6
CD EF	ff	STX (opr)	IND,Y	6

NOTES:

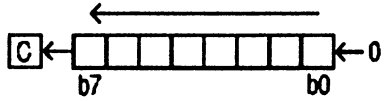
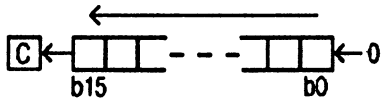
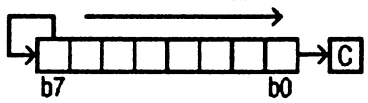
Operands:

- dd = 8-bit direct address $0000–$00FF. (High byte assumed to be $00.)
- ff = 8-bit positive offset $00 (0) to $FF (255) added to index.
- hh = High order byte of 16-bit extended address.
- ii = One byte of immediate data.
- jj = High order byte of 16-bit immediate data.
- kk = Low order byte of 16-bit immediate data.
- ll = Low order byte of 16-bit extended address.
- mm = 8-bit mask (set bits to be affected).
- rr = Signed relative offset $80 (–128) to $7F (+127). Offset relative to the address following the machine code offset byte.

INSTRUCTIONS, ADDRESSING MODES, AND EXECUTION TIMES

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
ABA	Add Accumulators	A + B → A	INH	1B		1	2	—	—	Δ	—	Δ	Δ	Δ	Δ
ABX	Add B to X	IX + 00:B → IX	INH	3A		1	3	—	—	—	—	—	—	—	—
ABY	Add B to Y	IY + 00:B → IY	INH	18 3A		2	4	—	—	—	—	—	—	—	—
ADCA (opr)	Add with Carry to A	A + M + C → A	A IMM	89	ii	2	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			A DIR	99	dd	2	3								
			A EXT	B9	hh ll	3	4								
			A IND,X	A9	ff	2	4								
			A IND,Y	18 A9	ff	3	5								
ADCB (opr)	Add with Carry to B	B + M + C → B	B IMM	C9	ii	2	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			B DIR	D9	dd	2	3								
			B EXT	F9	hh ll	3	4								
			B IND,X	E9	ff	2	4								
			B IND,Y	18 E9	ff	3	5								

ADDA	(opr)	Add Memory to A	A + M → A	A	IMM	8B	ii		2	2	—	—	Δ	—	Δ	Δ	Δ	Δ
				A	DIR	9B	dd		2	3								
				A	EXT	BB	hh	ll	3	4								
				A	IND,X	AB	ff		2	4								
				A	IND,Y	18 AB	ff		3	5								
ADDB	(opr)	Add Memory to B	B + M → B	B	IMM	CB	ii		2	2	—	—	Δ	—	Δ	Δ	Δ	Δ
				B	DIR	DB	dd		2	3								
				B	EXT	FB	hh	ll	3	4								
				B	IND,X	EB	ff		2	4								
				B	IND,Y	18 EB	ff		3	5								
ADDD	(opr)	Add 16-Bit to D	D + M:M + 1 → D		IMM	C3	jj	kk	3	4	—	—	—	—	Δ	Δ	Δ	Δ
					DIR	D3	dd		2	5								
					EXT	F3	hh	ll	3	6								
					IND,X	E3	ff		2	6								
					IND,Y	18 E3	ff		3	7								
ANDA	(opr)	AND A with Memory	A • M → A	A	IMM	84	ii		2	2	—	—	—	—	Δ	Δ	0	—
				A	DIR	94	dd		2	3								
				A	EXT	B4	hh	ll	3	4								
				A	IND,X	A4	ff		2	4								
				A	IND,Y	18 A4	ff		3	5								

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
ANDB (opr)	AND B with Memory	B • M → B	B IMM	C4	ii	2	2	—	—	—	—	Δ	Δ	0	—
			B DIR	D4	dd	2	3								
			B EXT	F4	hh ll	3	4								
			B IND,X	E4	ff	2	4								
			B IND,Y	18 E4	ff	3	5								
ASL (opr)	Arithmetic Shift Left		EXT	78	hh ll	3	6	—	—	—	—	Δ	Δ	Δ	Δ
			IND,X	68	ff	2	6								
			IND,Y	18 68	ff	3	7								
			A INH	48		1	2								
			B INH	58		1	2								
ASLD	Arithmetic Shift Left Double		INH	05		1	3	—	—	—	—	Δ	Δ	Δ	Δ
ASR (opr)	Arithmetic Shift Right		EXT	77	hh ll	3	6	—	—	—	—	Δ	Δ	Δ	Δ
			IND,X	67	ff	2	6								
			IND,Y	18 67	ff	3	7								
			A INH	47		1	2								
			B INH	57		1	2								
BCC (rel)	Branch if Carry Clear	? C = 0	REL	24	rr	2	3	—	—	—	—	—	—	—	—

BCLR	(opr) (msk)	Clear Bit(s)	M • (mm) → M		DIR IND,X IND,Y	15 1D 18 1D	dd ff ff	mm mm mm		3 3 4	6 7 8	—	—	—	—	Δ	Δ	0	—
BCS	(rel)	Branch if Carry Set	?C = 1		REL	25	rr			2	3	—	—	—	—	—	—	—	—
BEQ	(rel)	Branch if = Zero	?Z = 1		REL	27	rr			2	3	—	—	—	—	—	—	—	—
BGE	(rel)	Branch if ≥ Zero	?N ⊕ V = 0		REL	2C	rr			2	3	—	—	—	—	—	—	—	—
BGT	(rel)	Branch if > Zero	?Z + (N ⊕ V) = 0		REL	2E	rr			2	3	—	—	—	—	—	—	—	—
BHI	(rel)	Branch if Higher	?C + Z = 0		REL	22	rr			2	3	—	—	—	—	—	—	—	—
BHS	(rel)	Branch if Higher or Same	?C = 0		REL	24	rr			2	3	—	—	—	—	—	—	—	—
BITA	(opr)	Bit(s) Test A with Memory	A • M	A A A A A	IMM DIR EXT IND,X IND,Y	85 95 B5 A5 18 A5	ii dd hh ff ff	ll		2 2 3 2 3	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
BITB	(opr)	Bit(s) Test B with Memory	B • M	B B B B B	IMM DIR EXT IND,X IND,Y	C5 D5 F5 E5 18 E5	ii dd hh ff ff	ll		2 2 3 2 3	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—

[redacted]

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S X H I N Z V C
BLE (rel)	Branch if ≤ Zero	?Z + (N ⊕ V) = 1	REL	2F	rr	2	3	— — — — — — — —
BLO (rel)	Branch if Lower	?C = 1	REL	25	rr	2	3	— — — — — — — —
BLS (rel)	Branch if Lower or Same	?C + Z = 1	REL	23	rr	2	3	— — — — — — — —
BLT (rel)	Branch if < Zero	?N ⊕ V = 1	REL	2D	rr	2	3	— — — — — — — —
BMI (rel)	Branch if Minus	?N = 1	REL	2B	rr	2	3	— — — — — — — —
BNE (rel)	Branch if Not = Zero	?Z = 0	REL	26	rr	2	3	— — — — — — — —
BPL (rel)	Branch if Plus	?N = 0	REL	2A	rr	2	3	— — — — — — — —
BRA (rel)	Branch Always	?1 = 1	REL	20	rr	2	3	— — — — — — — —
BRCLR (opr) (msk) (rel)	Branch if Bit(s) Clear	?M • mm = 0	DIR IND,X IND,Y	13 1F 18 1F	dd mm rr ff mm rr ff mm rr	4 4 5	6 7 8	— — — — — — — —
BRN (rel)	Branch Never	?1 = 0	REL	21	rr	2	3	— — — — — — — —
BRSET (opr) (msk) (rel)	Branch if Bit(s) Set	?(M) • mm = 0	DIR IND,X IND,Y	12 1E 18 1E	dd mm rr ff mm rr ff mm rr	4 4 5	6 7 8	— — — — — — — —

BSET	(opr) (msk)	Set Bit(s)	M + mm → M		DIR IND,X IND,Y	14 1C 18 1C	dd mm ff mm ff mm	3 3 4	6 7 8	—	—	—	—	Δ	Δ	0	—
BSR	(rel)	Branch to Subroutine	See Special Ops		REL	8D	rr	2	6	—	—	—	—	—	—	—	—
BVC	(rel)	Branch if Overflow Clear	? V = 0		REL	28	rr	2	3	—	—	—	—	—	—	—	—
BVS	(rel)	Branch if Overflow Set	? V = 1		REL	29	rr	2	3	—	—	—	—	—	—	—	—
CBA		Compare A to B	A – B		INH	11		1	2	—	—	—	—	Δ	Δ	Δ	Δ
CLC		Clear Carry Bit	0 → C		INH	0C		1	2	—	—	—	—	—	—	—	0
CLI		Clear Interrupt Mask	0 → I		INH	0E		1	2	—	—	—	0	—	—	—	—
CLR	(opr)	Clear Memory Byte	0 → M		EXT IND,X IND,Y	7F 6F 18 6F	hh ll ff ff	3 2 3	6 6 7	—	—	—	—	0	1	0	0
CLRA		Clear Accumulator A	0 → A	A	INH	4F		1	2	—	—	—	—	0	1	0	0
CLRB		Clear Accumulator B	0 → B	B	INH	5F		1	2	—	—	—	—	0	1	0	0
CLV		Clear Overflow Flag	0 → V		INH	0A		1	2	—	—	—	—	—	—	0	—

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Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
CMPA (opr)	Compare A to Memory	A – M	A IMM	81	ii	2	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	91	dd	2	3								
			A EXT	B1	hh ll	3	4								
			A IND,X	A1	ff	2	4								
			A IND,Y	18 A1	ff	3	5								
CMPB (opr)	Compare B to Memory	B – M	B IMM	C1	ii	2	2	—	—	—	—	Δ	Δ	Δ	Δ
			B DIR	D1	dd	2	3								
			B EXT	F1	hh ll	3	4								
			B IND,X	E1	ff	2	4								
			B IND,Y	18 E1	ff	3	5								
COM (opr)	1's Complement Memory Byte	$FF – M → M	EXT	73	hh ll	3	6	—	—	—	—	Δ	Δ	0	1
			IND,X	63	ff	2	6								
			IND,Y	18 63	ff	3	7								
COMA	1's Complement A	$FF – A → A	A INH	43		1	2	—	—	—	—	Δ	Δ	0	1
COMB	1's Complement B	$FF – B → B	B INH	53		1	2	—	—	—	—	Δ	Δ	0	1
CPD (opr)	Compare D to Memory 16-Bit	D – M:M + 1	IMM	1A 83	jj kk	4	5	—	—	—	—	Δ	Δ	Δ	Δ
			DIR	1A 93	dd	3	6								
			EXT	1A B3	hh ll	4	7								
			IND,X	1A A3	ff	3	7								
			IND,Y	CD A3	ff	3	7								

CPX	(opr)	Compare X to Memory 16-Bit	IX – M:M + 1		IMM DIR EXT IND,X IND,Y	8C 9C BC AC CD AC	jj dd hh ff ff	kk ll 	3 2 3 2 3	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
CPY	(opr)	Compare Y to Memory 16-Bit	IY – M:M + 1		IMM DIR EXT IND,X IND,Y	18 8C 18 9C 18 BC 1A AC 18 AC	jj dd hh ff ff	kk ll 	4 3 4 3 3	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
DAA		Decimal Adjust A	Adjust Sum to BCD		INH	19			1	2	—	—	—	—	Δ	Δ	Δ	Δ
DEC	(opr)	Decrement Memory Byte	M – 1 → M		EXT IND,X IND,Y	7A 6A 18 6A	hh ff ff	ll 	3 2 3	6 6 7	—	—	—	—	Δ	Δ	Δ	—
DECA		Decrement Accumulator A	A – 1 → A	A	INH	4A			1	2	—	—	—	—	Δ	Δ	Δ	—
DECB		Decrement Accumulator B	B – 1 → B	B	INH	5A			1	2	—	—	—	—	Δ	Δ	Δ	—
DES		Decrement Stack Pointer	SP – 1 → SP		INH	34			1	3	—	—	—	—	—	—	—	—
DEX		Decrement Index Register X	IX – 1 → IX		INH	09			1	3	—	—	—	—	—	Δ	—	—

[redacted]

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
DEY	Decrement Index Register Y	IY − 1 → IY	INH	18 09		2	4	—	—	—	—	—	Δ	—	—
EORA (opr)	Exclusive OR A with Memory	A ⊕ M → A	A IMM	88	ii	2	2	—	—	—	—	Δ	Δ	0	—
			A DIR	98	dd	2	3								
			A EXT	B8	hh ll	3	4								
			A IND,X	A8	ff	2	4								
			A IND,Y	18 A8	ff	3	5								
EORB (opr)	Exclusive OR B with Memory	B ⊕ M → B	B IMM	C8	ii	2	2	—	—	—	—	Δ	Δ	0	—
			B DIR	D8	dd	2	3								
			B EXT	F8	hh ll	3	4								
			B IND,X	E8	ff	2	4								
			B IND,Y	18 E8	ff	3	5								
FDIV	Fractional Divide 16 by 16	D/IX → IX; r → D	INH	03		1	41	—	—	—	—	—	Δ	Δ	Δ
IDIV	Integer Divide 16 by 16	D/IX → IX; r → D	INH	02		1	41	—	—	—	—	—	Δ	0	Δ
INC (opr)	Increment Memory Byte	M + 1 → M	EXT	7C	hh ll	3	6	—	—	—	—	Δ	Δ	Δ	—
			IND,X	6C	ff	2	6								
			IND,Y	18 6C	ff	3	7								
INCA	Increment Accumulator A	A + 1 → A	A INH	4C		1	2	—	—	—	—	Δ	Δ	Δ	—
INCB	Increment Accumulator B	B + 1 → B	B INH	5C		1	2	—	—	—	—	Δ	Δ	Δ	—

INS		Increment Stack Pointer	SP + 1 → SP		INH		31			1	3	—	—	—	—	—	—	—	—
INX		Increment Index Register X	IX + 1 → IX		INH		08			1	3	—	—	—	—	—	Δ	—	—
INY		Increment Index Register Y	IY + 1 → IY		INH		18 08			2	4	—	—	—	—	—	Δ	—	—
JMP	(opr)	Jump	See Special Ops		EXT		7E	hh	ll	3	3	—	—	—	—	—	—	—	—
					IND,X		6E	ff		2	3								
					IND,Y		18 6E	ff		3	4								
JSR	(opr)	Jump to Subroutine	See Special Ops		DIR		9D	dd		2	5	—	—	—	—	—	—	—	—
					EXT		BD	hh	ll	3	6								
					IND,X		AD	ff		2	6								
					IND,Y		18 AD	ff		3	7								
LDAA	(opr)	Load Accumulator A	M → A	A	IMM		86	ii		2	2	—	—	—	—	Δ	Δ	0	—
				A	DIR		96	dd		2	3								
				A	EXT		B6	hh	ll	3	4								
				A	IND,X		A6	ff		2	4								
				A	IND,Y		18 A6	ff		3	5								
LDAB	(opr)	Load Accumulator B	M → B	B	IMM		C6	ii		2	2	—	—	—	—	Δ	Δ	0	—
				B	DIR		D6	dd		2	3								
				B	EXT		F6	hh	ll	3	4								
				B	IND,X		E6	ff		2	4								
				B	IND,Y		18 E6	ff		3	5								

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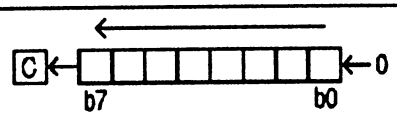
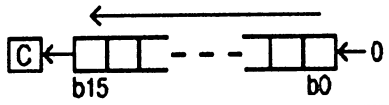
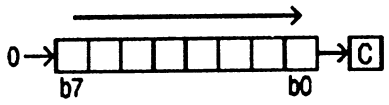
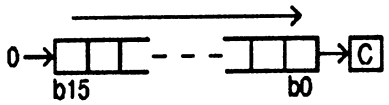
Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
LDD (opr)	Load Double Accumulator D	M → A, M + 1 → B	IMM	CC	jj kk	3	3	—	—	—	—	Δ	Δ	0	—
			DIR	DC	dd	2	4								
			EXT	FC	hh ll	3	5								
			IND,X	EC	ff	2	5								
			IND,Y	18 EC	ff	3	6								
LDS (opr)	Load Stack Pointer	M:M + 1 → SP	IMM	8E	jj kk	3	3	—	—	—	—	Δ	Δ	0	—
			DIR	9E	dd	2	4								
			EXT	BE	hh ll	3	5								
			IND,X	AE	ff	2	5								
			IND,Y	18 AE	ff	3	6								
LDX (opr)	Load Index Register X	M:M + 1 → IX	IMM	CE	jj kk	3	3	—	—	—	—	Δ	Δ	0	—
			DIR	DE	dd	2	4								
			EXT	FE	hh ll	3	5								
			IND,X	EE	ff	2	5								
			IND,Y	CD EE	ff	3	6								
LDY (opr)	Load Index Register Y	M:M + 1 → IY	IMM	18 CE	jj kk	4	4	—	—	—	—	Δ	Δ	0	—
			DIR	18 DE	dd	3	5								
			EXT	18 FE	hh ll	4	6								
			IND,X	1A EE	ff	3	6								
			IND,Y	18 EE	ff	3	6								

LSL (opr)	Logical Shift Left			EXT	78	hh ll		3	6	—	—	—	—	Δ	Δ	Δ	Δ
				IND,X	68	ff		2	6								
				IND,Y	18 68	ff		3	7								
			A	INH	48			1	2								
			B	INH	58			1	2								
LSLD	Logical Shift Left Double			INH	05			1	3	—	—	—	—	Δ	Δ	Δ	Δ
LSR (opr)	Logical Shift Right			EXT	74	hh ll		3	6	—	—	—	—	0	Δ	Δ	Δ
				IND,X	64	ff		2	6								
				IND,Y	18 64	ff		3	7								
			A	INH	44			1	2								
			B	INH	54			1	2								
LSRD	Logical Shift Right Double			INH	04			1	3	—	—	—	—	0	Δ	Δ	Δ
MUL	Multiply 8 by 8	A × B → D		INH	3D			1	10	—	—	—	—	—	—	—	Δ
NEG (opr)	2's Complement Memory Byte	0 − M → M		EXT	70	hh ll		3	6	—	—	—	—	Δ	Δ	Δ	Δ
				IND,X	60	ff		2	6								
				IND,Y	18 60	ff		3	7								
NEGA	2's Complement A	0 − A → A	A	INH	40			1	2	—	—	—	—	Δ	Δ	Δ	Δ
NEGB	2's Complement B	0 − B → B	B	INH	50			1	2	—	—	—	—	Δ	Δ	Δ	Δ
NOP	No Operation	No Operation		INH	01			1	2	—	—	—	—	—	—	—	—

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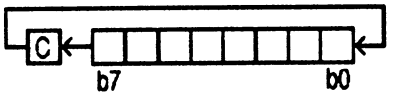
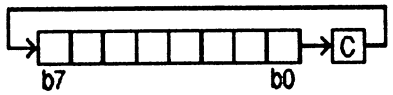
Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S X H I N Z V C
ORAA (opr)	OR Accumulator A (Inclusive)	A + M → A	A IMM A DIR A EXT A IND,X A IND,Y	8A 9A BA AA 18 AA	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	— — — — Δ Δ 0 —
ORAB (opr)	OR Accumulator B (Inclusive)	B + M → B	B IMM B DIR B EXT B IND,X B IND,Y	CA DA FA EA 18 EA	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	— — — — Δ Δ 0 —
PSHA	Push A onto Stack	A → Stk, SP = SP – 1	A INH	36		1	3	— — — — — — — —
PSHB	Push B onto Stack	B → Stk, SP = SP – 1	B INH	37		1	3	— — — — — — — —
PSHX	Push X onto Stack (Lo First)	IX → Stk, SP = SP – 2	INH	3C		1	4	— — — — — — — —
PSHY	Push Y onto Stack (Lo First)	IY → Stk, SP = SP – 2	INH	18 3C		2	5	— — — — — — — —
PULA	Pull A from Stack	SP = SP + 1, A ← Stk	A INH	32		1	4	— — — — — — — —
PULB	Pull B from Stack	SP = SP + 1, B ← Stk	B INH	33		1	4	— — — — — — — —
PULX	Pull X from Stack (Hi First)	SP = SP + 2, IX ← Stk	INH	38		1	5	— — — — — — — —
PULY	Pull Y from Stack (Hi First)	SP = SP + 2, IY ← Stk	INH	18 38		2	6	— — — — — — — —

ROL	(opr)	Rotate Left			EXT	79	hh	ll	3	6	—	—	—	—	Δ	Δ	Δ	Δ
					IND,X	69	ff		2	6								
					IND,Y	18 69	ff		3	7								
				A	INH	49			1	2								
				B	INH	59			1	2								
ROR	(opr)	Rotate Right			EXT	76	hh	ll	3	6	—	—	—	—	Δ	Δ	Δ	Δ
					IND,X	66	ff		2	6								
					IND,Y	18 66	ff		3	7								
				A	INH	46			1	2								
				B	INH	56			1	2								
RTI		Return from Interrupt	See Special Ops		INH	3B			1	12	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
RTS		Return from Subroutine	See Special Ops		INH	39			1	5	—	—	—	—	—	—	—	—
SBA		Subtract B from A	A – B → A		INH	10			1	2	—	—	—	—	Δ	Δ	Δ	Δ
SBCA	(opr)	Subtract with Carry from A	A – M – C → A	A	IMM	82	ii		2	2	—	—	—	—	Δ	Δ	Δ	Δ
				A	DIR	92	dd		2	3								
				A	EXT	B2	hh	ll	3	4								
				A	IND,X	A2	ff		2	4								
				A	IND,Y	18 A2	ff		3	5								
SBCB	(opr)	Subtract with Carry from B	B – M – C → B	B	IMM	C2	ii		2	2	—	—	—	—	Δ	Δ	Δ	Δ
				B	DIR	D2	dd		2	3								
				B	EXT	F2	hh	ll	3	4								
				B	IND,X	E2	ff		2	4								
				B	IND,Y	18 E2	ff		3	5								

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S X H I N Z V C
SEC	Set Carry	1 → C	INH	0D		1	2	— — — — — — — 1
SEI	Set Interrupt Mask	1 → I	INH	0F		1	2	— — — 1 — — — —
SEV	Set Overflow Flag	1 → V	INH	0B		1	2	— — — — — — 1 —
STAA (opr)	Store Accumulator A	A → M	A DIR A EXT A IND,X A IND,Y	97 B7 A7 18 A7	dd hh ll ff ff	2 3 2 3	3 4 4 5	— — — — Δ Δ 0 —
STAB (opr)	Store Accumulator B	B → M	B DIR B EXT B IND,X B IND,Y	D7 F7 E7 18 E7	dd hh ll ff ff	2 3 2 3	3 4 4 5	— — — — Δ Δ 0 —
STD (opr)	Store Accumulator D	A → M, B → M + 1	DIR EXT IND,X IND,Y	DD FD ED 18 ED	dd hh ll ff ff	2 3 2 3	4 5 5 6	— — — — Δ Δ 0 —
STOP	Stop Internal Clocks		INH	CF		1	2	— — — — — — — —
STS (opr)	Store Stack Pointer	SP → M:M + 1	DIR EXT IND,X IND,Y	9F BF AF 18 AF	dd hh ll ff ff	2 3 2 3	4 5 5 6	— — — — Δ Δ 0 —

STX	(opr)	Store Index Register X	IX → M:M + 1		DIR	DF	dd		2	4	—	—	—	—	Δ	Δ	0	—
					EXT	FF	hh	ll	3	5								
					IND,X	EF	ff		2	5								
					IND,Y	CD EF	ff		3	6								
STY	(opr)	Store Index Register Y	IY → M:M + 1		DIR	18 DF	dd		3	5	—	—	—	—	Δ	Δ	0	—
					EXT	18 FF	hh	ll	4	6								
					IND,X	1A EF	ff		3	6								
					IND,Y	18 EF	ff		3	6								
SUBA	(opr)	Subtract Memory from A	A – M → A	A	IMM	80	ii		2	2	—	—	—	—	Δ	Δ	Δ	Δ
				A	DIR	90	dd		2	3								
				A	EXT	B0	hh	ll	3	4								
				A	IND,X	A0	ff		2	4								
				A	IND,Y	18 A0	ff		3	5								
SUBB	(opr)	Subtract Memory from B	B – M → B	B	IMM	C0	ii		2	2	—	—	—	—	Δ	Δ	Δ	Δ
				B	DIR	D0	dd		2	3								
				B	EXT	F0	hh	ll	3	4								
				B	IND,X	E0	ff		2	4								
				B	IND,Y	18 E0	ff		3	5								
SUBD	(opr)	Subtract Memory from D	D – M:M + 1 → D		IMM	83	jj	kk	3	4	—	—	—	—	Δ	Δ	Δ	Δ
					DIR	93	dd		2	5								
					EXT	B3	hh	ll	3	6								
					IND,X	A3	ff		2	6								
					IND,Y	18 A3	ff		3	7								
SWI		Software Interrupt	See Special Ops		INH	3F			1	14	—	—	—	1	—	—	—	—
TAB		Transfer A to B	A → B		INH	16			1	2	—	—	—	—	Δ	Δ	0	—
TAP		Transfer A to CCR	A → CCR		INH	06			1	2	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
TBA	Transfer B to A	B → A	INH	17		1	2	—	—	—	—	Δ	Δ	0	—
TEST	TEST (Only in Test Modes)	Address Bus Counts	INH	00		1	*	—	—	—	—	—	—	—	—
TPA	Transfer CCR to A	CCR → A	INH	07		1	2	—	—	—	—	—	—	—	—
TST (opr)	Test for Zero or Minus	M – 0	EXT IND,X IND,Y	7D 6D 18 6D	hh ll ff ff	3 2 3	6 6 7	—	—	—	—	Δ	Δ	0	0
TSTA		A – 0	A INH	4D		1	2	—	—	—	—	Δ	Δ	0	0
TSTB		B – 0	B INH	5D		1	2	—	—	—	—	Δ	Δ	0	0
TSX	Transfer Stack Pointer to X	SP + 1 → IX	INH	30		1	3	—	—	—	—	—	—	—	—
TSY	Transfer Stack Pointer to Y	SP + 1 → IY	INH	18 30		2	4	—	—	—	—	—	—	—	—
TXS	Transfer X to Stack Pointer	IX – 1 → SP	INH	35		1	3	—	—	—	—	—	—	—	—
TYS	Transfer Y to Stack Pointer	IY – 1 → SP	INH	18 35		2	4	—	—	—	—	—	—	—	—
WAI	Wait for Interrupt	Stack Regs and WAIT	INH	3E		1	* *	—	—	—	—	—	—	—	—
XGDX	Exchange D with X	IX → D, D → IX	INH	8F		1	3	—	—	—	—	—	—	—	—
XGDY	Exchange D with Y	IY → D, D → IY	INH	18 8F		2	4	—	—	—	—	—	—	—	—

NOTES:

Cycle:

*	=	Infinity or until reset occurs
**	=	12 cycles are used beginning with the opcode fetch. A wait state is entered which remains in effect for an integer number of MPU E-clock cycle (n) until an interrupt is recognized. Finally, two additional cycles are used to fetch the appropriate interrupt vector (total = 14 + n).

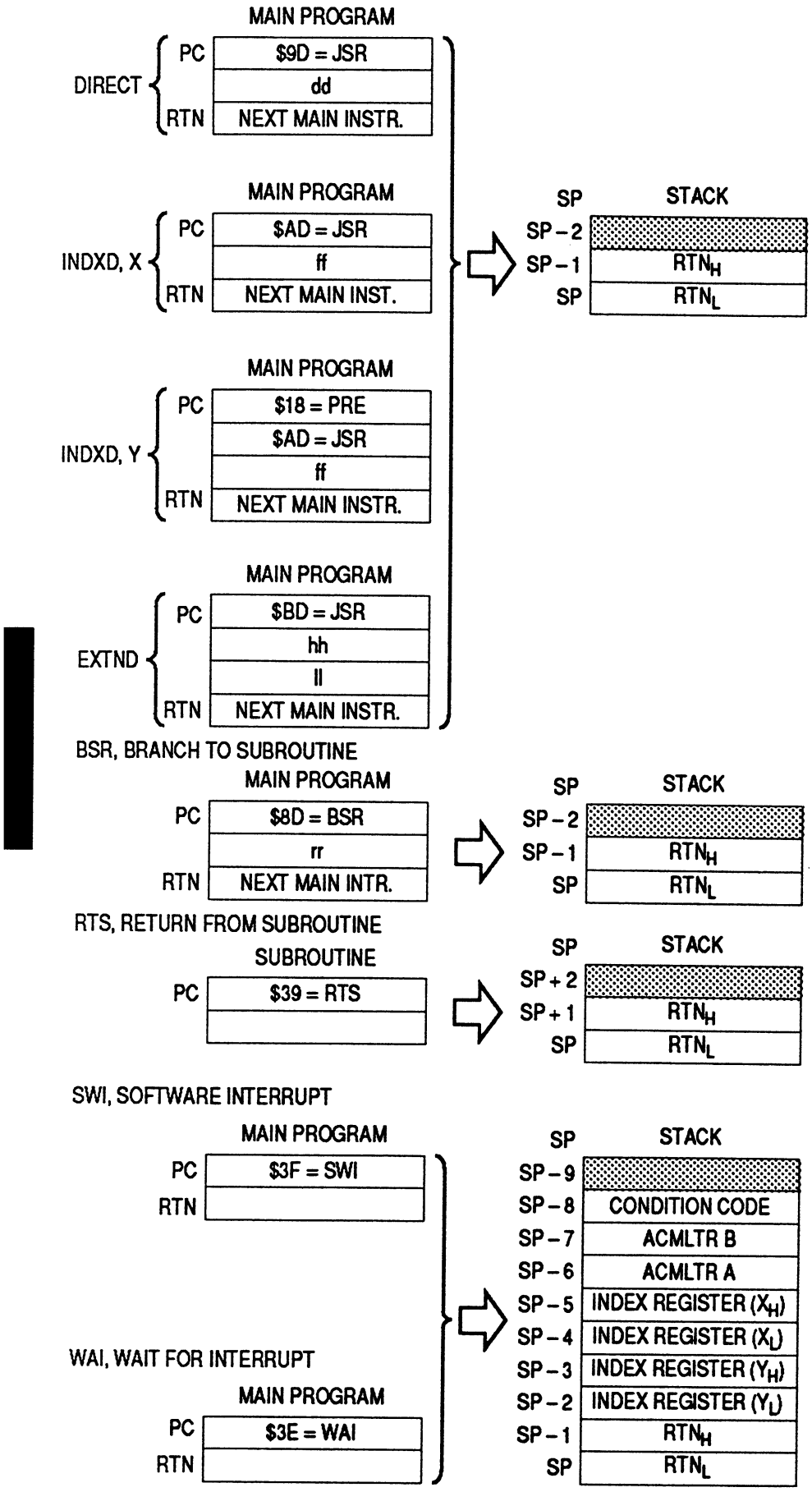
Operands:

dd	=	8-bit direct address $0000–$00FF. (High byte assumed to be $00.)
ff	=	8-bit positive offset $00 (0) to $FF (255) added to index.
hh	=	High order byte of 16-bit extended address.
ii	=	One byte of immediate data.
jj	=	High order byte of 16-bit immediate data.
kk	=	Low order byte of 16-bit immediate data.
ll	=	Low order byte of 16-bit extended address.
mm	=	8-bit mask (set bits to be affected).
rr	=	Signed relative offset $80 (–128) to $7F (+127). Offset relative to the address following the machine code offset byte.

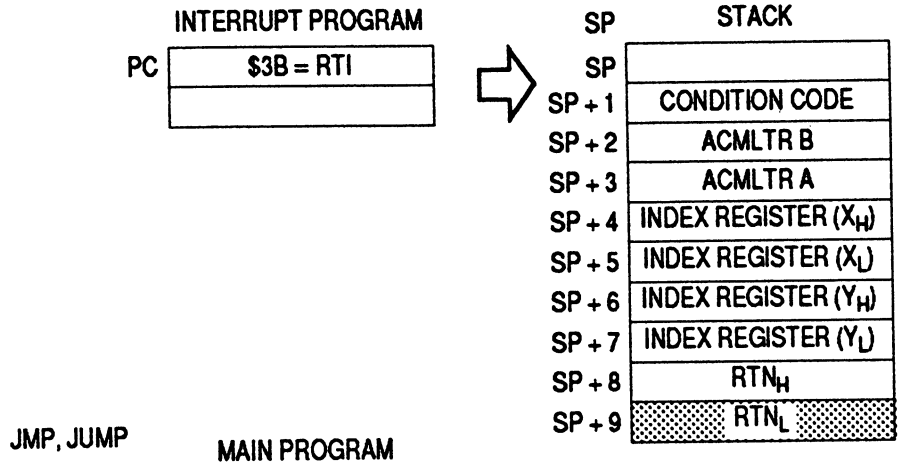
Condition Codes:

—	=	Bit not changed
0	=	Always cleared (logic 0).
1	=	Always set (logic 1).
Δ	=	Bit cleared or set depending on operation.
↓	=	Bit may be cleared, cannot become set.

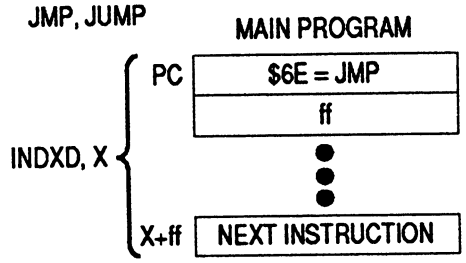
[redacted]

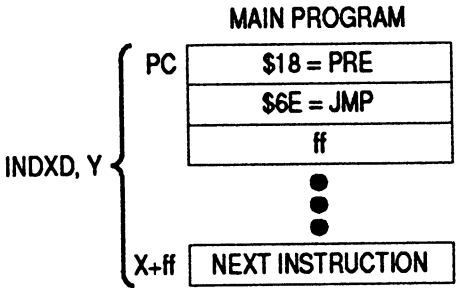


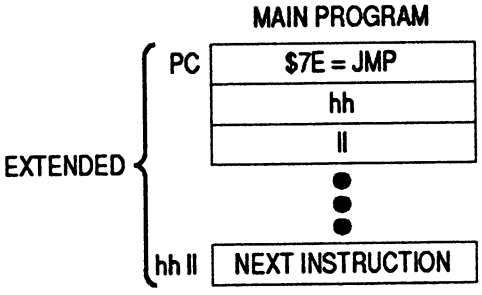
RTI, RETURN FROM INTERRUPT



JMP, JUMP







LEGEND

RTN = Address of next instruction in main program to be executed upon return from subroutine

RTN_H = Most significant byte of return address

RTN_L = Least significant byte of return address

▩ = Stack pointer location after execution

dd = 8-Bit direct address ($0000–$00FF) (high byte assumed to be $00)

ff = 8-Bit positive offset $00 (0) to $FF (256) (is added to index)

hh = High order byte of 16-bit extended address

ll = Low order byte of 16-bit extended address

rr = Signed relative offset $80 (–128) to $7F (+127)
(offset relative to the address following the machine code offset byte)

MC68HC11F1 Registers (1 of 2)

The 128-byte register block can be remapped to any 4K boundary.

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
$1002	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	PORTG
$1003	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	DDRG
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PORTF
$1006	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (Hi)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Lo)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (Hi)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Lo)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (Hi)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Lo)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (Hi)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Lo)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1 (Hi)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Lo)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (Hi)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Lo)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (Hi)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Lo)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (Hi)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Lo)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (Hi)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (Lo)
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I	TMSK1

MC68HC11F1 Registers (2 of 2)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
$1026	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$1029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR
$102A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$102C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$1035	0	0	0	PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT
$1036									Reserved
$1037									Reserved
$1038	GWOM	CWOM	CLK4X	0	0	0	0	0	OPT2
$1039	ADPU	CSEL	IRQE	DLY	CME	FCME	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	0	TEST1
$103F	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON	CONFIG
$1040 to $105B									Reserved
$105C	IO1SA	IO1SB	IO2SA	IO2SB	GSTHA	GSTHB	PSTHA	PSTHB	CSSTRH
$105D	IO1EN	IO1PL	IO2EN	IO2PL	GCSPR	PCSEN	PSIZA	PSIZB	CSCTL
$105E	GA15	GA14	GA13	GA12	GA11	GA10	0	0	CSGADR
$105F	IO1AV	IO2AV	0	GNPOL	GAVLD	GSIZA	GSIZB	GSIZC	CSGSIZ

ADCTL

A/D Control/Status

	Bit 7	6	5	4	3	2	1	Bit 0
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA
RESET:	U	0	U	U	U	U	U	U

CCF — Conversions Complete Flag
This bit is set after an A/D conversion cycle and cleared when ADCTL is written.
Bit 6 — Not implemented; always reads zero
SCAN — Continuous Scan Control
0 = Do four conversions and stop
1 = Convert four channels in selected group continuously
MULT — Multiple-Channel/Single-Channel Control
0 = Convert single-channel selected
1 = Convert four channels in selected group
CD–CA — Channel Select D through A

Channel Select Control Bits				Channel Signal	Result in ADRx if MULT = 1
CD	CC	CB	CA		
0	0	0	0	AN0	ADR1
0	0	0	1	AN1	ADR2
0	0	1	0	AN2	ADR3
0	0	1	1	AN3	ADR4
0	1	0	0	AN4	ADR1
0	1	0	1	AN5	ADR2
0	1	1	0	AN6	ADR3
0	1	1	1	AN7	ADR4
1	0	X	X	Reserved	ADR1–ADR4
1	1	0	0	V_{RH}*	ADR1
1	1	0	1	V_{RL}*	ADR2
1	1	1	0	$(V_{RH})/2$*	ADR3
1	1	1	1	Reserved*	ADR4

*Used for factory testing

A/D Results

$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4

Analog Input to 8-Bit Result Translation Table

	Bit 7	6	5	4	3	2	1	Bit 0
% (1)	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
Volts (2)	2.500	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195

(1) % of V_{RH}–V_{RL} (2) Volts for V_{RL} = 0; V_{RH} = 5.0 V

BAUD

Baud Rate

	Bit 7	6	5	4	3	2	1	Bit 0
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters (TEST)
RCKB — SCI Baud Rate Clock Check (TEST)
SCP[1:0] — SCI Baud Rate Prescaler Selects

SCP[1:0]		Divide Internal Clock By	Crystal Frequency in MHz			
1	0		8.0 MHz (Baud)	10.0 MHz (Baud)	12.0 MHz (Baud)	16.0 MHz (Baud)
0	0	1	125.0 K	156.25 K	187.5 K	250.0 K
0	1	3	41.67 K	52.08 K	62.5 K	83.33 K
1	0	4	31.25 K	38.4 K	46.88 K	62.5 K
1	1	13	9600	12.02 K	14.42 K	19.2 K

SCR[2:0] — SCI Baud Rate Selects
These bits select the receiver and transmitter bit rate based on output from the baud rate prescaler stage.

SCR [2:0]			Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table)		
				9600	19.2 K	38.4 K
0	0	0	1	9600	19.2 K	38.4 K
0	0	1	2	4800	9600	19.2 K
0	1	0	4	2400	4800	9600
0	1	1	8	1200	2400	4800
1	0	0	16	600	1200	2400
1	0	1	32	300	600	1200
1	1	0	64	150	300	600
1	1	1	128	—	150	300

BPROT

Block Protect

	Bit 7	6	5	4	3	2	1	Bit 0
$1035	0	0	0	PTCON	BPRT3	BPRT2	BPRT1	BPRT0
RESET:	1	1	1	1	1	1	1	1

Bits [7:5] — Not implemented; always read 0
PTCON — Protect for CONFIG
0 = CONFIG register can be programmed or erased normally.
1 = CONFIG register cannot be programmed or erased.
BPRT[3:0] — Block Protect Bits for EEPROM
Block protect register bits can be written to zero (protection disabled) only once within 64 cycles of a reset in normal modes, or at any time in special modes. Block protect register bits can be written to one (protection enabled) at any time.
0 = Protection disabled
1 = Protection enabled

Bit Name	Block Protected	Block Size
BPRT3	$xEE0–$xFFF	288 Bytes
BPRT2	$xE60–$xEDF	128 Bytes
BPRT1	$xE20–$xE5F	64 Bytes
BPRT0	$xE00–$xD9F	32 Bytes

CFORC

Timer Compare Force

	Bit 7	6	5	4	3	2	1	Bit 0
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET:	0	0	0	0	0	0	0	0

FOC[5:1] — Write ones to Force Compare(s)
0 = Not affected
1 = Output x action occurs.
Bits [2:0] — Not implemented; always read 0

CONFIG

COP, ROM Mapping, EEPROM Enables

	Bit 7	6	5	4	3	2	1	Bit 0
$103F	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON
RESET:	—	—	—	—	1	—	1	—

The CONFIG bits can be read at any time. The value read is the value latched into the register from the EEPROM cells during the last reset sequence. A new value programmed into this register is not readable until after a subsequent reset sequence. Unused bits always read as ones.

If SMOD = 1, these bits are writable any time. If SMOD = 0 these bits can only be written using the EEPROM programming sequence, and are neither readable nor active until latched via the next reset.

EE[3:0] — EEPROM Map Position Bits
EEPROM is located at $xE00–$xFFF, where x is the value represented by these four bits. In single-chip and bootstrap modes, EEPROM is forced to $FE00–$FFFF, regardless of the state of these bits.
Bits 3 and 1 — Not implemented; always read one
NOCOP — COP System Disable
Resets to programmed value
0 = COP enabled (forces reset on timeout)
1 = COP disabled (does not force reset on timeout)
EEON — EEPROM Enable
0 = EEPROM removed from the memory map
1 = EEPROM present in the memory map

COPRST

Arm/Reset COP Timer Circuitry

	Bit 7	6	5	4	3	2	1	Bit 0
$103A	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism. Write $AA to COPRST to reset COP watchdog.

CSCTL

Chip-Select Control

	Bit 7	6	5	4	3	2	1	Bit 0
$105D	IO1EN	IO1PL	IO2EN	IO2PL	GCSPR	PCSEN	PSIZA	PSIZB
RESET:	0	0	0	0	0	—	0	0

IO1EN — I/O Chip-Select 1 Bit Enable
- 0 = CSIO disabled
- 1 = CSIO enabled

IO1PL — I/O Chip-Select 1 Bit Polarity Select
- 0 = CSIO active low
- 1 = CSIO active high

IO2EN — I/O Chip-Select 2 Bit Enable
- 0 = CSIO disabled
- 1 = CSIO enabled

IO2PL — I/O Chip-Select 2 Bit Polarity Select
- 0 = CSIO active low
- 1 = CSIO active high

GCSPR — General-Purpose Chip-Select Priority
- 0 = Program chip select has priority over general-purpose chip selects
- 1 = General-purpose chip selects have priority over program chip select

PCSEN — Program Chip-Select Enable

Reset clears PCSEN in single-chip mode, sets PCSEN in expanded-nonmultiplexed mode.
- 0 = CSPROG disabled
- 1 = CSPROG enabled

PSIZA, PSIZB — Program Chip-Select Size (A or B)

PSIZA	PSIZB	Size (Bytes)	Address Range
0	0	64 K	$0000–$FFFF
0	1	32 K	$8000–$FFFF
1	0	16 K	$C000–$FFFF
1	1	8 K	$E000–$FFFF

CSGADR

General-Purpose Chip-Select Address Register

	Bit 7	6	5	4	3	2	1	Bit 0
$105E	GA15	GA14	GA13	GA12	GA11	GA10	—	—
RESET:	0	0	0	0	0	0	0	0

GA[15:10] — General-Purpose Chip-Select Starting Address Bits
These bits correspond to the high-order address bits ADDR[15:10]. They determine the starting address of the CSGEN valid address space. Valid register bits are determined by the address size selected.

Address Size Selected	CSGADR Bits Valid
0 Kbytes	None
1 Kbytes	GA[15:10]
2 Kbytes	GA[15:11]
4 Kbytes	GA[15:12]
8 Kbytes	GA[15:13]
16 Kbytes	GA[15:14]
32 Kbytes	GA15
64 Kbytes	None

Bits [1:0] — Not Implemented

CSGSIZ

General-Purpose Chip-Select Size Register

	Bit 7	6	5	4	3	2	1	Bit 0
$105F	IO1AV	IO2AV	—	GNPOL	GAVLD	GSIZA	GSIZB	GSIZC
RESET:	0	0	0	0	0	1	1	1

IO1AV — I/O Chip-Select 1 Address Valid
0 = CSIO1 is valid during E-clock valid time (E-clock high)
1 = CSIO1 is valid during address valid time
IO2AV — I/O Chip-Select 2 Address Valid
0 = CSIO2 is valid during E-clock valid time (E-clock high)
1 = CSIO2 is valid during address valid time
Bits 5 — Not Implemented; always reads zero
GNPOL — General-Purpose Chip-Select Polarity
0 = CSGEN is active low
1 = CSGEN is active high
GAVLD — General-Purpose Chip-Select Address Valid
0 = CSGEN is valid during E-clock valid time (E-clock high)
1 = CSGEN is valid during address valid time

GSIZA, GSIZB, and GSISC — Address Size for CSGEN

GSIZx			
A	B	C	Size (Bytes)
0	0	0	64 Kbytes
0	0	1	32 Kbytes
0	1	0	16 Kbytes
0	1	1	8 Kbytes
1	0	0	4 Kbytes
1	0	1	2 Kbytes
1	1	0	1 Kbytes
1	1	1	0 Kbytes

CSSTRH

Chip-Select Clock Stretch

	Bit 7	6	5	4	3	2	1	Bit 0
$105C	IO1SA	IO1SB	IO2SA	IO2SB	GSTHA	GSTHB	PSTHA	PSTHB
RESET:	0	0	0	0	0	0	0	0

IO1SA, IO1SB — CSIO 1 Clock Delay
IO2SA, IO2SB — CSIO 2 Clock Delay
GSTHA, GSTHB — General-Purpose Chip-Select Clock Delay
PSTHA, PSTHB — Program Chip-Select Clock Delay
The amount of clock stretching during each chip select is determined by the value of bits A and B for each type of chip select.

Bit [A:B]	Clock Stretch
0 0	None
0 1	1 Cycle
1 0	2 Cycles
1 1	3 Cycles

DDRA

Data Direction Register for Port A

	Bit 7	6	5	4	3	2	1	Bit 0
$1001	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
RESET:	0	0	0	0	0	0	0	0

DDA[7:0] — Data Direction for Port A
0 = Input
1 = Output

DDRC

Data Direction Register for Port C

	Bit 7	6	5	4	3	2	1	Bit 0
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction for Port C
0 = Input
1 = Output

DDRD

Data Direction Register for Port D

	Bit 7	6	5	4	3	2	1	Bit 0
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

Bits [7:6] — Not implemented; always read zero
DDD[5:0] — Data Direction for Port D
0 = Input
1 = Output

DDRG

Data Direction Register for Port G

	Bit 7	6	5	4	3	2	1	Bit 0
$1003	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0
RESET:	0	0	0	0	0	0	0	0

DDG7–DDG0 — Data Direction for Port G
0 = Input
1 = Output

HPRIO

Highest Priority I-Bit Interrupt and Miscellaneous

	Bit 7	6	5	4	3	2	1	Bit 0
$103C	RBOOT*	SMOD*	MDA*	IRV*	PSEL3	PSEL2	PSEL1	PSEL0
RESETS:								
Single-Chip Mode	0	0	0	0	0	1	1	0
Exp'd Nonmux'd	0	0	1	0	0	1	1	0
Bootstrap	1	1	0	0	0	1	1	0
Special Test	0	1	1	0	0	1	1	0

*RBOOT, SMOD, MDA and IRV resets depend on mode selected at power-up.

RBOOT — Read Bootstrap ROM

Valid only when SMOD is set to one (special bootstrap or special test mode). Can only be written in special modes.

0 = Bootloader ROM disabled and not in map

1 = Bootloader ROM enabled and in map at $BF00–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

These two bits can be read at any time. SMOD can only be written in special modes. MDA can be written at any time in special modes, but only once in normal mode.

Inputs		Mode	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single-Chip	0	0
1	1	Expanded Nonmultiplexed	0	1
0	0	Special Bootstrap	1	0
0	1	Special Test	1	1

PSEL[3:0] — Priority Select Bit 3 through Bit 0

Writable only while bit I in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources.

PSELx				Interrupt Source Promoted
3	2	1	0	
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	SPI Serial Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to $\overline{\text{IRQ}}$)
0	1	1	0	$\overline{\text{IRQ}}$ (External Pin)
0	1	1	1	Real-Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5/Input Capture 4

RAM and I/O Mapping

	Bit 7	6	5	4	3	2	1	Bit 0
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG4	REG1	REG0
RESET:	0	0	0	0	0	0	0	0

RAM[3:0] — Internal RAM Map Position
REG[3:0] — 128-Byte Register Block Map Position

NOTE

Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes

OC1D

Output Compare 1 Data

	Bit 7	6	5	4	3	2	1	Bit 0
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET:	0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.
Bits [2:0] — Not implemented; always read 0

OC1M

Output Compare 1 Mask

	Bit 7	6	5	4	3	2	1	Bit 0
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding port A pin(s).
Bits [2:0] — Not implemented; always read 0

OPT2

System Configuration Options 2

	Bit 7	6	5	4	3	2	1	Bit 0
$1038	GWOM	CWOM	CLK4X	0	0	0	0	0
RESET:	0	0	1	—	—	—	—	—

GWOM — Port G Wired-OR Mode
- 0 = Port G operates normally
- 1 = Port G outputs are open drain

CWOM — Port C Wired-OR Mode
- 0 = Port C operates normally
- 1 = Port C outputs are open drain

CLK4X — 4X Clock Output Enable Bit

This bit can only be written once after reset in normal modes (HPRIO register bit SMOD = 0).
- 0 = Output of 4XOUT clock is disabled
- 1 = Output of 4XOUT clock is enabled

Bits [4:0] — Not Implemented

OPTION

System Configuration Options

	Bit 7	6	5	4	3	2	1	Bit 0
$1039	ADPU	CSEL	IRQE*	DLY*	CME	FCME*	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal mode, or at any time in special modes.

ADPU — A/D Power-Up
- 0 = A/D powered down
- 1 = A/D powered up

CSEL — Clock Select

(Should be set to one if E Clock less than 1 MHz)
- 0 = A/D and EEPROM use system E clock
- 1 = A/D and EEPROM use internal RC clock

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
- 0 = Low level recognition
- 1 = Falling edge recognition

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
- 0 = No stabilization delay on exit from STOP
- 1 = Stabilization delay enabled on exit from STOP

CME — Clock Monitor Enable
- 0 = Clock monitor disabled; slow clocks can be used
- 1 = Slow or stopped clocks cause clock failure reset

FCME — Force Clock Monitor Enable
- 0 = Clock monitor follows the state of the CME bit
- 1 = Clock monitor circuit is enabled until next reset

CR[1:0] — COP Timer Rate Select

CR [1:0]	Divide E/2^{15} By	XTAL = 8.0 MHz Timeout –0/+16.4 ms	XTAL = 12.0 MHz Timeout –0/+10.9 ms	XTAL = 16.0 MHz Timeout –0/+8.2 ms
0 0	1	16.384 ms	10.923 ms	8.192 ms
0 1	4	65.536 ms	43.691 ms	32.768 ms
1 0	16	262.14 ms	174.76 ms	131.07 ms
1 1	64	1.049 sec	699.05 ms	524.29 ms
	E =	2.0 MHz	3.0 MHz	4.0 MHz

PACNT

Pulse Accumulator Counter

	Bit 7	6	5	4	3	2	1	Bit 0
$1027	Bit 7	6	5	4	3	2	1	Bit 0

Readable and writable.

PACTL

Pulse Accumulator Control

	Bit 7	6	5	4	3	2	1	Bit 0
$1026	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

Bits 7 and 3 — Not implemented; always read zero
PAEN — Pulse Accumulator System Enable
0 = Pulse Accumulator disabled
1 = Pulse Accumulator enabled
PAMOD — Pulse Accumulator Mode
0 = Event counter
1 = Gated time accumulation
PEDGE — Pulse Accumulator Edge Control
0 = Falling edges, high level enables accumulation
1 = Rising edges, low level enables accumulation
I4/O5 — Configure TI4/O5 for Input Capture or Output Compare
0 = OC5 enabled
1 = IC4 enabled
RTR[1:0] — Real-Time Interrupt (RTI) Rate

RTR [1:0]	Divide E By	XTAL = 8.0 MHz	XTAL = 12.0 MHz	XTAL = 16.0 MHz
0 0	2^{13}	4.096 ms	2.731 ms	2.048 ms
0 1	2^{14}	8.192 ms	5.461 ms	4.096 ms
1 0	2^{15}	16.384 ms	10.923 ms	8.192 ms
1 1	2^{16}	32.768 ms	21.845 ms	16.383 ms
	E =	2.0 MHz	3.0 MHz	4.0 MHz

PORTA

Port A Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	HiZ	0	0	0	HiZ	HiZ	HiZ	HiZ
Alt. Pin Func.:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

PORTB

Port B Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	ADDR 15	ADDR 14	ADDR 13	ADDR 12	ADDR 11	ADDR 10	ADDR 9	ADDR 8

PORTC

Port C Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1006	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0

PORTD

Port D Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

PORTE

Port E Data

	Bit 7	6	5	4	3	2	1	Bit 0
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	U	U	U	U	U	U	U	U
Alt. Pin Func.:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

PORTF

Port F Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1005	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

PORTG

Port G Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1002	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	R/$\overline{W}$	—	XA18	XA17	XA16	XA15	XA14	XA13

PG7 performs R/$\overline{W}$ in expanded and special test modes.

PPROG

EEPROM Programming Control

	Bit 7	6	5	4	3	2	1	Bit 0
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM
RESET:	0	0	0	0	0	0	0	0

ODD — Program Odd Rows in Half of EEPROM (TEST)
EVEN — Program Even Rows in Half of EEPROM (TEST)
Bit 5 — Not Implemented
BYTE — Byte/Other EEPROM Erase Mode
0 = Row or bulk erase mode used
1 = Erase only one byte of EEPROM
ROW — Row/All EEPROM Erase Mode (only valid when BYTE = 0)
0 = All 512 bytes of EEPROM erased
1 = Erase only one 16-byte row of EEPROM

BYTE	ROW	Action
0	0	Bulk Erase (All 512 Bytes)
0	1	Row Erase (16 Bytes)
1	0	Byte Erase
1	1	Byte Erase

ERASE — Erase/Normal Control for EEPROM
0 = Normal read or program mode
1 = Erase mode
EELAT — EEPROM Latch Control
0 = EEPROM address and data bus configured for normal reads
1 = EEPROM address and data bus configured for programming or erasing
EEPGM — EEPROM Program Command
0 = Program or erase voltage switched off to EEPROM array
1 = Program or erase voltage switched on to EEPROM array

SCCR1

SCI Control 1

	Bit 7	6	5	4	3	2	1	Bit 0
$102C	R8	T8	0	M	WAKE	0	0	0
RESET:	0	0	0	0	0	0	0	0

R8 — Receive Bit 8
If M bit is set, R8 stores the ninth bit in the receive data character.
T8 — Transmit Bit 8
If M bit is set, T8 stores the ninth bit in the transmit data character.
Bit 5 — Not implemented; always reads 0
M — Mode (Select Character Format)
0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit
WAKE — Wake-Up by Address Mark/Idle
0 = Wake-up by IDLE line recognition
1 = Wake-up by address mark (most significant data bit set)
Bits [2:0] — Not implemented; always read 0

SCCR2

SCI Control 2

	Bit 7	6	5	4	3	2	1	Bit 0
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TDRE status flag is set
TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI interrupt requested when TC status flag is set
RIE — Receiver Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set
ILIE — Idle Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set
TE — Transmitter Enable
0 = Transmitter disabled
1 = Transmitter enabled
RE — Receiver Enable
0 = Receiver disabled
1 = Receiver enabled
RWU — Receiver Wake-Up Control
0 = Normal SCI receiver
1 = Wake-up enabled and receiver interrupts inhibited
SBK — Send Break
0 = Break generator off
1 = Break codes generated as long as SBK = 1

SCDR

SCI Data Register

	Bit 7	6	5	4	3	2	1	Bit 0
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0

R[7:0]/T[7:0] — Receiver/Transmitter Data Bits [7:0]
SCI data is double buffered in both directions.

SCSR

SCI Status Register

	Bit 7	6	5	4	3	2	1	Bit 0
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag
This flag is set when SCDR is empty. Clear the TDRE flag by reading SCSR with TDRE set and then writing to SCDR.
0 = SCDR busy
1 = SCDR empty

TC — Transmit Complete Flag
This flag is set when the transmitter is idle (no data, preamble, or break transmission in progress). Clear the TC flag by reading SCSR with TC set and then writing to SCDR.
0 = Transmitter busy
1 = Transmitter idle

RDRF — Receive Data Register Full Flag
This flag is set if a received character is ready to be read from SCDR. Clear the RDRF flag by reading SCSR with RDRF set and then reading SCDR.
0 = SCDR empty
1 = SCDR full

IDLE — Idle Line Detected Flag
This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR with IDLE set and then reading SCDR.
0 = RxD line is active
1 = RxD line is idle

OR — Overrun Error Flag
OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR with OR set and then reading SCDR.
0 = No overrun
1 = Overrun detected

NF — Noise Error Flag
NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR with NF set and then reading SCDR.
0 = Unanimous decision
1 = Noise detected

FE — Framing Error
FE is set when a 0 is detected where a stop bit was expected. Clear the FE flag by reading SCSR with FE set and then reading SCDR.
0 = Stop bit detected
1 = 0 detected
Bit 0 — Not implemented; always reads 0

SPCR

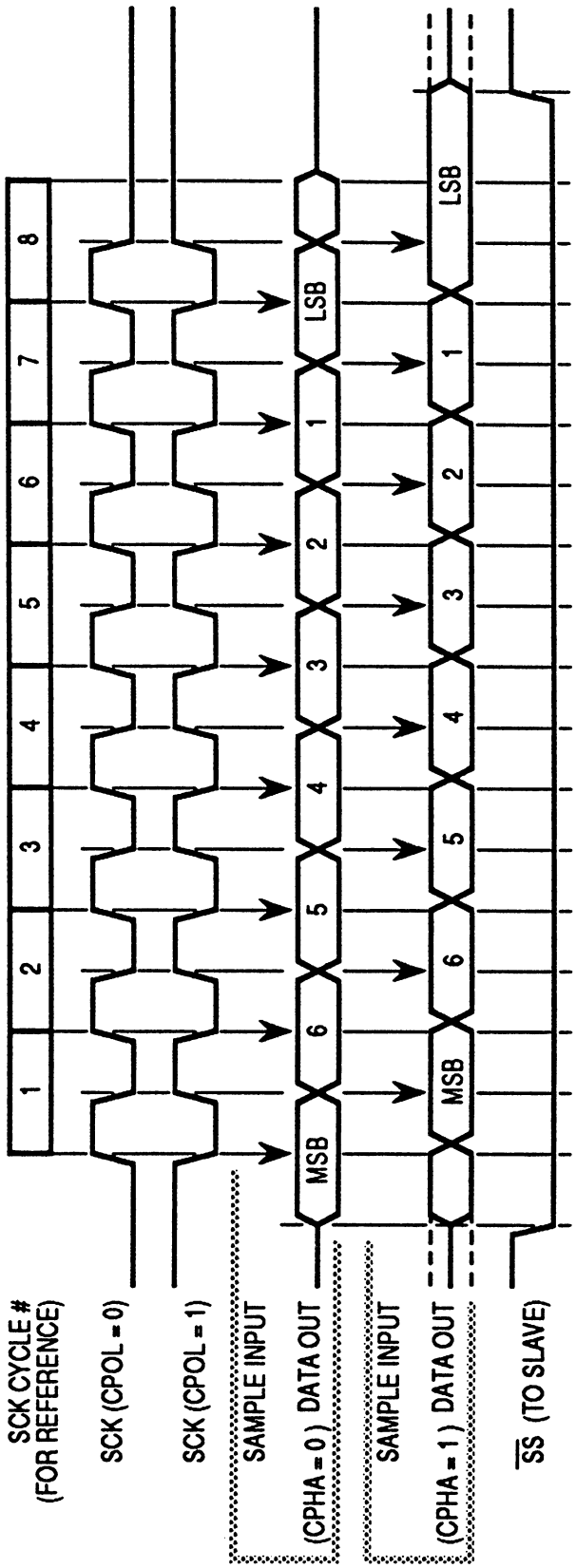
Serial Peripheral Control

	Bit 7	6	5	4	3	2	1	Bit 0
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
0 = SPI interrupts disabled
1 = SPI interrupts enabled
SPE — Serial Peripheral System Enable
0 = SPI off
1 = SPI on
DWOM — Port D Wired-OR Mode Option for SPI Pins PD5–PD2
(See also WOMS bit in SCCR2.)
0 = Normal CMOS outputs
1 = Open-drain outputs
MSTR — Master Mode Select
0 = Slave mode
1 = Master mode
CPOL, CPHA — Clock Polarity, Clock Phase
(Refer to SPI Transfer Format.)
SPR[1:0] — SPI Clock Rate Selects

SPR[1:0]	Divide E Clock By	Frequency at E = 2 MHz (Baud)
0 0	2	1.0 MHz
0 1	4	500 kHz
1 0	16	125 kHz
1 1	32	62.5 kHz

SPI Transfer Format



SPDR

SPI Data

	Bit 7	6	5	4	3	2	1	Bit 0
$102A	Bit 7	6	5	4	3	2	1	Bit 0

SPI is double buffered in, single buffered out.

SPSR

Serial Peripheral Status

	Bit 7	6	5	4	3	2	1	Bit 0
$1029	SPIF	WCOL	0	MODF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag
SPIF is set when an SPI transfer is complete. This bit is cleared by reading SPSR with SPIF set, followed by an SPDR access.
0 = Incomplete SPI transfer
1 = SPI transfer complete

WCOL — Write Collision
WCOL is set when SPDR is written while a transfer is in progress. It is cleared by reading SPSR with WCOL set, followed by an SPDR access.
0 = No write collision
1 = Write collision detected

Bits 5 and [3:0] — Not implemented; always read zero

MODF — Mode Fault (Mode fault terminates SPI operation)
MODF is set when $\overline{SS}$ is pulled low while MSTR = 1. This bit is cleared by reading SPCR with MODF set, followed by a write to SPCR.
0 = No mode fault detected
1 = Mode fault detected

TCNT

Timer Count

$100E	Bit 15	14	13	12	11	10	9	Bit 8	High	TCNT
$100F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000
In normal modes, TCNT is read-only.

TCTL1

Timer Control 1

	Bit 7	6	5	4	3	2	1	Bit 0
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM2–OM5 — Output Mode
OL2–OL5 — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to 0
1	1	Set OCx output line to 1

TCTL2

Timer Control 2

	Bit 7	6	5	4	3	2	1	Bit 0
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TFLG1

Timer Interrupt Flag 1

	Bit 7	6	5	4	3	2	1	Bit 0
$1023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag
Set each time the counter matches output compare x value.

I4/O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on which function was enabled by I4/O5 of PACTL.

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line.

TFLG2

Timer Interrupt Flag 2

	Bit 7	6	5	4	3	2	1	Bit 0
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time (Periodic) Interrupt Flag
Set periodically. Refer to RTR1 and RTR0 bits in PACTL register.

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00.

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line.

Bits [3:0] — Not implemented; always read zero

TI4/O5

Timer Input Capture 4/Output Compare 5

$101E	Bit 15	14	13	12	11	10	9	Bit 8	High	TI4/O5
$101F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TI4/O5 register pairs reset to ones ($FFFF).

TIC1–TIC3

Timer Input Capture

$1010	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC1
$1011	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1012	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC2
$1013	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1014	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC3
$1015	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TICx not affected by reset

TMSK1

Timer Interrupt Mask 1

	Bit 7	6	5	4	3	2	1	Bit 0
$1022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare x Interrupt Enable
I4/O5I — Input Capture 4 or Output Compare 5 Interrupt Enable
IC1I–IC3I — Input Capture x Interrupt Enable

TMSK2

Timer Interrupt Mask 2

	Bit 7	6	5	4	3	2	1	Bit 0
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable
RTII — Real-Time Interrupt Enable
PAOVI — Pulse Accumulator Overflow Interrupt Enable
PAII — Pulse Accumulator Input Edge Interrupt Enable
Bits [3:2] — Not implemented; always read zero
PR[1:0] — Timer Prescaler Select
In normal modes, PR1 and PR0 can only be written once, and the write must occur within 64 cycles after reset.

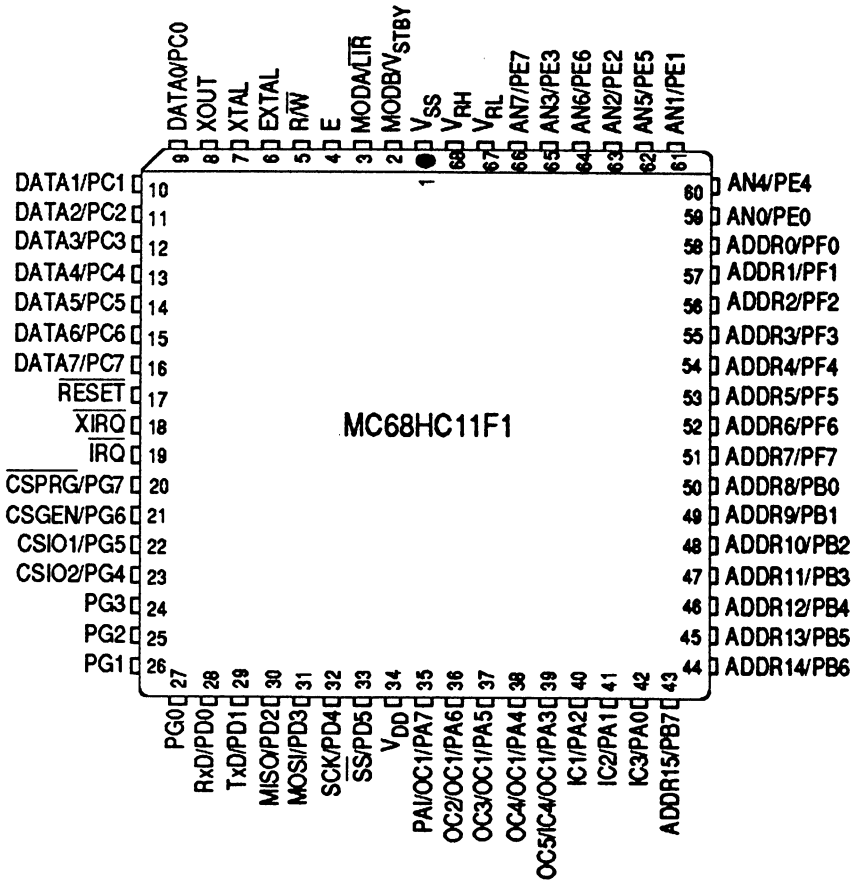
PR[1:0]	Prescaler
0 0	1
0 1	4
1 0	8
1 1	16

Timer Output Compare

$1016	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC1
$1017	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1018	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC2
$1019	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101A	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC3
$101B	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101C	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC4
$101D	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TOCx register pairs reset to ones ($FFFF).

MC68HC11F1 Pin Assignments



Hexadecimal and Decimal Conversion

How to Use:

Conversion to Decimal: Find the decimal weights for corresponding hexadecimal characters beginning with the least significant character. The sum of the decimal weights is the decimal value of the hexadecimal number.

Conversion to Hexadecimal: Find the highest decimal value in the table which is lower than or equal to the decimal number to be converted. The corresponding hexadecimal character is the most significant. Subtract the decimal value found from the decimal number to be converted. With the difference, repeat the process to find subsequent hexadecimal characters.

15 Byte 8				7 Byte 0			
15 Char 12		11 Char 8		7 Char 4		3 Char 0	
Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec
0	0	0	0	0	0	0	0
1	4,096	1	256	1	16	1	1
2	8,192	2	512	2	32	2	2
3	12,288	3	768	3	48	3	3
4	16,384	4	1,024	4	64	4	4
5	20,480	5	1,280	5	80	5	5
6	24,576	6	1,536	6	96	6	6
7	28,672	7	1,792	7	112	7	7
8	32,768	8	2,048	8	128	8	8
9	36,864	9	2,304	9	144	9	9
A	40,960	A	2,560	A	160	A	10
B	45,056	B	2,816	B	176	B	11
C	49,152	C	3,072	C	192	C	12
D	53,248	D	3,328	D	208	D	13
E	57,344	E	3,584	E	224	E	14
F	61,440	F	3,840	F	240	F	15

ASCII CHARACTER SET (7-Bit Code)								
MS Digit / LS Digit	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

PROGRAMMING MODEL
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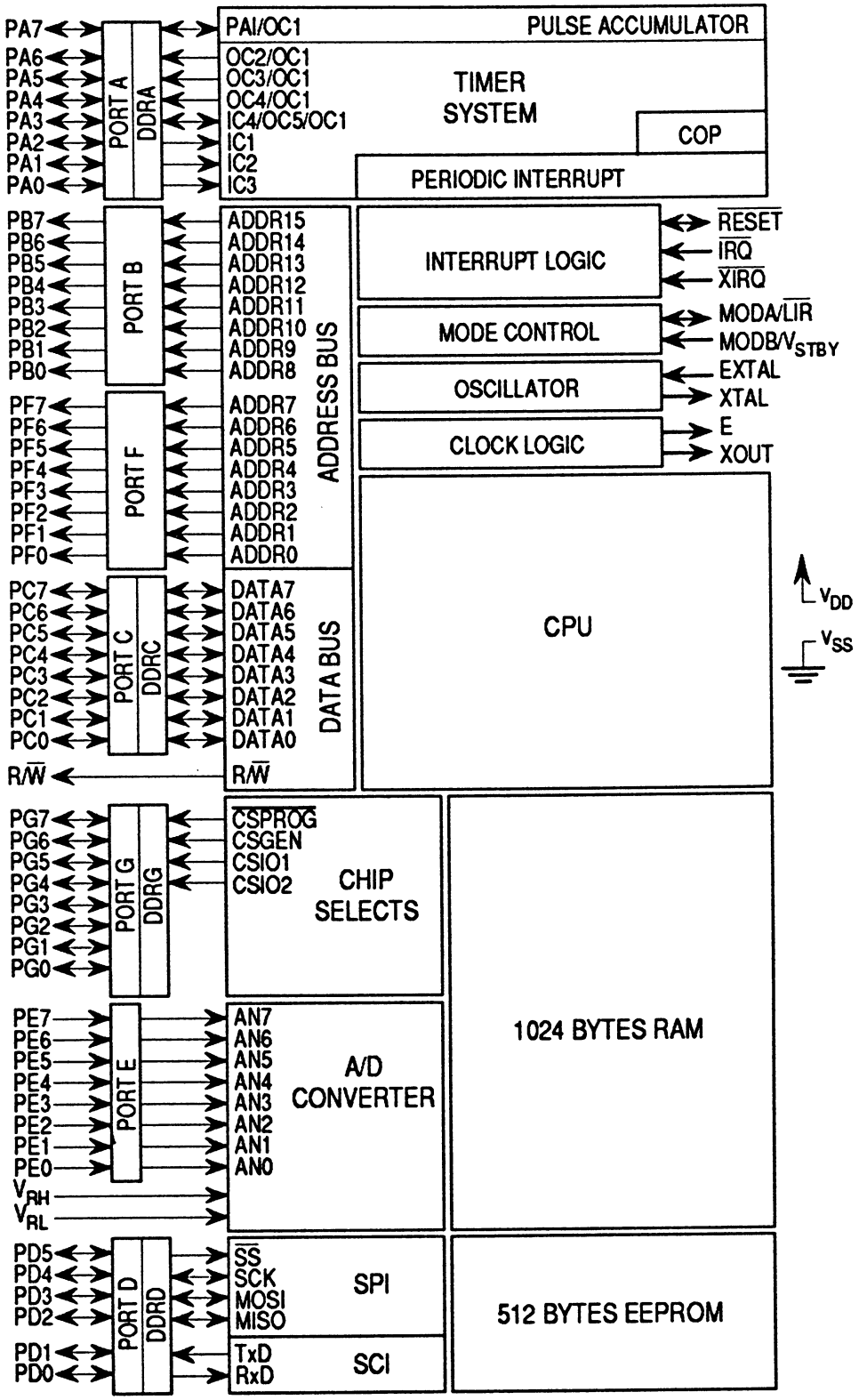
Block Diagram



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