Mask Set Errata

MSE08AZ32_0J66D
12/2002

Mask Set Errata for MC68HC08AZ32, Mask 0J66D

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Introduction

This mask set errata applies to this MC68HC08AZ32 MCU mask set:

- 0J66D

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J66D. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “0201” indicates the first week of the year 2002.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

Stop I_{DD}

SE14-STOP_IDD

Variable Stop I_{DD} currents in Stop Mode may be seen. This is due to a floating node within the A/D converter module. The effect of this floating node is that the total Stop I_{DD} current exceeds the published value of 150µA for LVI disabled over the temperature range –40°C to +125°C after a number of seconds. Typical values seen are between 150µA and 350µA. However, in the case of the LVI being enabled, the specification of 600µA over the temperature range –40°C to +125°C is not exceeded.

Typical data across full temp range worst case supply voltage for samples from 3 wafer lots:

–40°C to 85°C

Mean Stop I_{DD} 123µA
STD Dev 107µA
Mean +3 sigma 553µA
Max recorded value 559µA
Specification 600µA

–40°C to 125°C

Mean Stop I_{DD} 268µA
STD Dev 126µA
Mean +3 sigma 646µA
Max recorded value 559µA
Specification 600µA

SIM (System Integration Module)

SE15-SIM

An illegal address reset is generated when data is accessed in an unimplemented address using indexed addressing mode instructions and PUL/PSH.

This is treated as an internal reset and the RESET pin is driven low for 32 clock cycles.

ROM Security — 1H56A and 0J66D

SE16-ROM

The ROM security feature is not offered on the 68HC08AZ/AB ROM device because the operation of security in monitor mode does not match that of other HC08 family members.

MSCAN Extended ID Rejected if STUFF Bit Between ID16 and ID15

SE17-MSCAN

For 32-bit and 16-bit identifier acceptance modes, an extended ID CAN frame with a stuff bit between ID16 and ID15 can be erroneously rejected, depending on IDAR0, IDAR1, and IDMR1.

Extended IDs (ID28-ID0) which generate a stuff bit between ID16 and ID15:

Table 1.

IDAR0	IDAR1	IDAR2	IDAR3
********	***1111x	xxxxxxxx	xxxxxxxx

where x = 0 or 1 (don't care)
* = pattern for ID28 to ID18 (see following).

Affected extended IDs (ID28 - ID18) patterns:

a) xxxxxxxxx01 exceptions: 00000000001
01111100001
xxxx1000001 except 11111000001

b) xxxxx100000 exception: 01111100000

c) xxxx0111111 exception: 00000111111

d) x0111110000

e) 10000000000

f) 11111111111

g) 10000011111

When an affected ID is received, an incorrect value is compared to the 2nd byte of the filter (IDAR1 and IDAR5, plus IDAR3 and IDAR7 in 16-bit mode). This incorrect value is the shift register contents before ID15 is shifted in (i.e. right shifted by 1).

Workaround

If the problematic IDs cannot be avoided, the workaround is to mask certain bits with IDMR1 (and IDMR5, plus IDMR3 and IDMR7 in 16-bit mode).

Example 1: to receive the message IDs
xxxx xxxx x011 111x xxxx xxxx xxxx xxxx
IDMR1 etc. must be 111x xxx1, i.e. ID20,19,18,15 must be masked.

Example 2: to receive the message IDs
xxxx 0111 1111 111x xxxx xxxx xxxx xxxx
IDMR1 etc. must be 1xxx xxx1, i.e. ID20 and ID15 must be masked.

In general, using IDMR1 etc. 1111 xxx1, i.e. masking ID20,19,18,SRR,15, hides the problem.

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