Mask Set Errata

MSE08AZ32_0H56A
12/2002

Mask Set Errata for MC68HC08AZ32, Mask 0H56A

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Introduction

This mask set errata applies to this MC68HC08AZ32 MCU mask set:

- 0H56A

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0H56A. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “0201” indicates the first week of the year 2002.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

MSCAN Module

SE10-MSCAN

Correct operation of the MSCAN Receive and Transmit Error Counters cannot be assured when running at high temperature across all voltages. The counters can decrement by a count of either 1,2, 3, or 4 due to weak P-channel devices within the error counter control logic. The problem arises when between 1 and 3 errors have occurred in the system. Then after receipt or transmission of a successful message, the error counter decrements by 4 instead of 1, immediately putting the MSCAN module into Receiver Error Passive or Transmitter Error Passive mode. Normal operation will resume once the error counter count returns to below the limit of 127. The P-channel devices have been resized on the1H56A mask set. Special screen tests have been developed for the 0H56A mask set to screen for this failure mode, however samples are very limited due to excessive yield loss. Standard processing is not to screen for this failure.

Serial Peripheral Interface (SPI)

SE11-SPI

Clearing the SPE bit to disable the SPI can cause an error when transmitting in slave mode. In this situation, a race condition occurs, allowing an invalid mode fault to occur.

Mode faults occur on the SPI when the slave select ($\overline{SS}$) pin is toggled during a transmission. Mode faults also occur if $\overline{SS}$ is selected and then unselected before SPSCK returns to its idle level after the shift of the eighth data bit when CPHA = 0 while in slave mode.

When the SPI is disabled, the special port function associated with $\overline{SS}$ is also disabled and returns to a logic 1. In slave mode, $\overline{SS}$ must remain a logic 0 during a transmission. Thus, disabling the SPI causes the $\overline{SS}$ signal to go high internally, which sets up a race for the port logic to send in a logic 1 and the SPI to shut down mode fault detection internally.

Workaround

This condition can be avoided easily in software if mode faults are disabled by clearing the MODFEN bit of the SPSCR register before disabling the SPI in slave mode.

Timer Interface Module (TIM)

SE12-TIMA_AND_TIMB

When the toggle on overflow (TOV) bit is set, writing to a TCHxH register at the point of an overflow inhibits the associated pin from toggling until the TCHxL

register is written. The pin then toggles at the next overflow. Even though a toggle can be completely missed, the TOF flag will be set and an interrupt can be generated. The only way to inhibit a toggle on overflow and set the TOF bit is to write to the TMODH register until the TMODL register is written. Similarly, in buffered PWM mode, writing to the inactive registers (TCH0H:l, TCH2H:L, TCH4H:L) at this overflow point produces the same problem. Writing to the odd channels (TCH1H:L, TCH3H:L, TCH5H:L) produces no faults.

Workaround: Avoid this problem by using the overflow routine instead of writing to inactive channel registers within the output compare routine. Each output compare event occurs as a result of the last channel register written to prior to the last overflow.

Make sure that both odd and even timer channel registers are initialized. Write to the odd channels last, because the active channel register on startup is the even channel. If the inactive channel register is not written to last, then the next PWM pulse width will be exactly the same as the first, reflecting the value written to the even channel register.

MSCAN Module

SE13-MSCAN

In an ‘almost overrun’ condition, the MSCAN receive buffer can contain an incorrect message.The following sequence will cause the receive buffer to have an incorrect message. The message will be a shifted image of the true message:

1. Both foreground & background receive buffers are filled but have not yet been released by software.
2. The MSCAN begins to transmit message ‘M’
3. Software releases one or both receive buffers by clearing RXF bits
4. The MSCAN loses arbitration on the CAN bus while transmitting ‘M’
5. The next bits seen on the bus after clearing RXF will be interpreted as the beginning of the ID field. This ‘shifted’ ID happens to pass the filter configuration programmed into MSCAN

Workaround The receive driver software must process the incoming stream of messages fast enough to never have the MSCAN enter the state with both buffers filled (almost overrun). When overrun occurs (OVRIF=1), the MSCAN receive queue must be initialized by asserting/deasserting SFTRES. If the software is designed such that it can cope with maximum CAN throughput, this case will never occur.

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