Mask Set Errata

MSE08AS32_1J27F
8/2003
Rev. 1

Mask Set Errata for
MC68HC08AS32,
Mask 1J27F

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Introduction

This mask set errata applies to this MC68HC08AS32 MCU mask set:

- 1J27F

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 1J27F. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “0301” indicates the first week of the year 2003.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

EEPROM

SE1-EEPROM

The EEPROM module has a logic error in the block protect logic which may result in higher than normal current consumption in stop mode. The operating conditions where the extra current has been observed are V_{DD} = 5.5 V and TA > 70 °C. The increased current consumption ranges from 10 µA to 200 µA.

Either of the following software workarounds will ensure that the EEPROM module is configured in its lowest current state during stop mode.

Workaround 1

Program bits 0 – 3 of the EEPROM non-volatile register (EEBP0 – EEBP3 of location $FE1C) to 0s. Note that this also disables block protection for all four blocks of the EEPROM array.

Workaround 2

Execute this code immediately prior to executing the stop instruction:

```
lda #$0c
sta $fe1d
lda #$ff
sta $fe1c
```

NOTE: *Make sure to insert code to clear the EEPROM control register (location $FE1D) at the beginning of an interrupt service routine if stop mode is exited with an interrupt.*

BDLC 300 µs IFS Issue

SE18-BDLC

If two messages are received at 300 µs interframe separation (IFS) (+/– µs, as measured at the RX pin), the second message's start-of-frame (SOF) symbol generates an invalid symbol interrupt. This invalid symbol interrupt results in the second message being lost and, therefore, unavailable to the application software. This is the result of a race condition within the BDLC where it is changing states in its receive state machine at the same time a transition occurs on the RX pin (beginning of the SOF symbol of the second message).

Workarounds

- Ensure that no nodes on the J1850 network will transmit a message at 300 µs IFS separation from another message. Be certain that physical layer error is taken into account when calculating this case, as temperature changes and ground shifts can shift the timing seen at the

RX pin of the microcontroller. Motorola silicon implementations of J1850 have not been shown to retransmit any faster than 320 µs, and are, therefore, not likely to cause this behavior.

- Design messaging and application software to properly handle loss of messages in the system. This is safe programming practice in any case and will protect the integrity of the system in the event of a lost message.

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