

MCF51CN128 Reference Manual Errata

by: Microcontroller Division

This errata document describes corrections to the *MCF51CN128 Reference Manual*, order number MCF51CN128RM. For convenience, the addenda items are grouped by revision. Please check our website at <http://www.freescale.com/coldfire> for the latest updates.

The current available version of the *MCF51CN128 Reference Manual* is Revision 6.

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1 Errata for Revision 6

Table 1. MCF51CN128RM Rev 6 Errata

Location	Description																																																																																																						
Table 15-1 / Page 15-2	<p>Corrected ADC Channel Assignments table as:</p> <table border="1"> <thead> <tr> <th>ADCH</th> <th>Channel</th> <th>Input</th> <th>ADCH</th> <th>Channel</th> <th>Input</th> </tr> </thead> <tbody> <tr> <td>00000</td> <td>AD0</td> <td>PTE2/KBI2P2/$\overline{SS2}$/ADP0</td> <td>10000</td> <td>AD16</td> <td>Reserved</td> </tr> <tr> <td>00001</td> <td>AD1</td> <td>PTE1/KBI2P1/MOSI2/ADP1</td> <td>10001</td> <td>AD17</td> <td>Reserved</td> </tr> <tr> <td>00010</td> <td>AD2</td> <td>PTE0/KBI2P0/MISO2/ADP2</td> <td>10010</td> <td>AD18</td> <td>Reserved</td> </tr> <tr> <td>00011</td> <td>AD3</td> <td>PTD7RGPIO7/SPSCK2/ADP3</td> <td>10011</td> <td>AD19</td> <td>Reserved</td> </tr> <tr> <td>00100</td> <td>AD4</td> <td>PTD3RGPIO3/RXD2/ADP4</td> <td>10100</td> <td>AD20</td> <td>Reserved</td> </tr> <tr> <td>00101</td> <td>AD5</td> <td>PTD2/RGPIO2/TXD2/ADP5</td> <td>10101</td> <td>AD21</td> <td>Reserved</td> </tr> <tr> <td>00110</td> <td>AD6</td> <td>PTD1/RGPIO1/RXD1/ADP6</td> <td>10110</td> <td>AD22</td> <td>Reserved</td> </tr> <tr> <td>00111</td> <td>AD7</td> <td>PTD0/RGPIO0/TXD1/ADP7</td> <td>10111</td> <td>AD23</td> <td>Reserved</td> </tr> <tr> <td>01000</td> <td>AD8</td> <td>PTC7/SDA2/SPSCK1/ADP8</td> <td>11000</td> <td>AD24</td> <td>Reserved</td> </tr> <tr> <td>01001</td> <td>AD9</td> <td>PTC6/SCL2/MISO1/ADP9</td> <td>11001</td> <td>AD25</td> <td>Reserved</td> </tr> <tr> <td>01010</td> <td>AD10</td> <td>PTC5/MOSI1/ADP10</td> <td>11010</td> <td>AD26</td> <td>Temperature Sensor</td> </tr> <tr> <td>01011</td> <td>AD11</td> <td>PTC4/IRQ/$\overline{SS1}$/ADP11</td> <td>11011</td> <td>AD27</td> <td>Internal Bandgap</td> </tr> <tr> <td>01100</td> <td>AD12</td> <td>Reserved</td> <td>11100</td> <td>—</td> <td>Reserved</td> </tr> <tr> <td>01101</td> <td>AD13</td> <td>Reserved</td> <td>11101</td> <td>V_{REFH}</td> <td>V_{DD}</td> </tr> <tr> <td>01110</td> <td>AD14</td> <td>Reserved</td> <td>11110</td> <td>V_{REFL}</td> <td>V_{SS}</td> </tr> <tr> <td>01111</td> <td>AD15</td> <td>Reserved</td> <td>11111</td> <td>Module Disabled</td> <td>None</td> </tr> </tbody> </table>	ADCH	Channel	Input	ADCH	Channel	Input	00000	AD0	PTE2/KBI2P2/ $\overline{SS2}$ /ADP0	10000	AD16	Reserved	00001	AD1	PTE1/KBI2P1/MOSI2/ADP1	10001	AD17	Reserved	00010	AD2	PTE0/KBI2P0/MISO2/ADP2	10010	AD18	Reserved	00011	AD3	PTD7RGPIO7/SPSCK2/ADP3	10011	AD19	Reserved	00100	AD4	PTD3RGPIO3/RXD2/ADP4	10100	AD20	Reserved	00101	AD5	PTD2/RGPIO2/TXD2/ADP5	10101	AD21	Reserved	00110	AD6	PTD1/RGPIO1/RXD1/ADP6	10110	AD22	Reserved	00111	AD7	PTD0/RGPIO0/TXD1/ADP7	10111	AD23	Reserved	01000	AD8	PTC7/SDA2/SPSCK1/ADP8	11000	AD24	Reserved	01001	AD9	PTC6/SCL2/MISO1/ADP9	11001	AD25	Reserved	01010	AD10	PTC5/MOSI1/ADP10	11010	AD26	Temperature Sensor	01011	AD11	PTC4/IRQ/ $\overline{SS1}$ /ADP11	11011	AD27	Internal Bandgap	01100	AD12	Reserved	11100	—	Reserved	01101	AD13	Reserved	11101	V _{REFH}	V _{DD}	01110	AD14	Reserved	11110	V _{REFL}	V _{SS}	01111	AD15	Reserved	11111	Module Disabled	None
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Table 11-5 / Page 11-6	<p>Corrected CSCRn[MUX] bit description as:</p> <p>Multiplexed mode. Selects between multiplexed and non-multiplexed address/data bus.</p> <p>0 Non-multiplexed configuration. Address information is driven on FB_ADn and data is read/written on FB_dn.</p> <p>1 Multiplexed configuration. Address information is driven on FB_ADn, and low-order address lines (FB_AD[7:0] for byte port size or FB_AD[15:0] for word port size) must be latched using the falling edge of FB_ALE as the latch enable. Data is read/written on FB_AD[7:0] for byte port size and FB_AD[15:0] for word port size.</p>																																																																																																						

Table 1. MCF51CN128RM Rev 6 Errata (continued)

Location	Description
Table 18-3 / Page 18-6	<p>Corrected MTIMCLK[CLKS] bit field description as:</p> <p>Clock Source Select — These two read/write bits select one of four different clock sources as the input to the MTIM prescaler. Changing the clock source while the counter is active does not clear the counter. The count continues with the new clock source. Reset clears CLKS to 00.</p> <p>00 Encoding 0. Bus clock (BUSCLK) 01 Encoding 1. Fixed-frequency clock (XCLK) 10 Encoding 2. External source (TCLK pin), falling edge 11 Encoding 3. External source (TCLK pin), rising edge All other encodings default to the bus clock (BUSCLK).</p>

2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
0	Various technical and other corrections as described in Table 1 .	10/2010
1	Updated ADC Channel Assignments table.	2/2011

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