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MC33689D

Introduction

This errata sheet applies to the following device:

- MC33689D SBCLIN (System Basis Chip with LIN Transceiver)

Device Identification

All standard devices are marked with a device identification and build information code. The first line written on the package indicates the Part Number and the second line the Date Code.

- MC33689DDWB is the part marking for this device

Device Build Information / Date Code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the seven character build information code (e.g. “AWL0529”). The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “0529” indicates the 29th week of the year 2005.

Device Part Number Prefixes

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MC prefix.

MC33689D Errata - LIN Dominant Issue

PC33689DDWB or MC33689DDWB are the part numbers for the device errata, regardless of the date code.

Description

The LIN Physical Layer Specification which is part of the LIN Specification Package 2.0 defines the V_{SUP} supply voltage range between 7V and 18V (V_{BAT} range 8V to 18V). On this device, the LIN bus output can get stuck in dominant state if both conditions are present:

1. The supply voltage V_{SUP} is below 5.5V and above 4.7V ($5.5V > V_{SUP} > 4.7V$).
2. The device is in Normal Mode and the transceiver is forcing the LIN to dominant state (TXD=0V).

If V_{SUP} drops further below 4.7V (Reset threshold typical value), the device will reset and the LIN bus goes in recessive state or if the V_{SUP} is increasing above 5.5V the LIN bus goes also in recessive state (Normal Operation).

Workaround

Avoid stuck condition

To avoid the transceiver to transmit data in the critical V_{SUP} area (5.5V to 4.7V), the Low Voltage Interrupt of the Micro Controller can be used to detect the critical V_{SUP} area and to disable (by software) the transmission.

To reenable the transmission, the Low Voltage Flag can be used to detect that the supply voltage is back high enough.

Remove a stuck condition

To avoid having the stuck condition present for a longer period of time, it’s possible to detect the dominant state by monitoring the RXD signal. The stuck dominant can be removed by entering the device in Sleep or Stop Mode or by preventing the TXD communication transmission (TXD stays in Recessive State) during the V_{SUP} critical voltage range.

MC33689D Errata - Low Voltage Reset Weakness

PC33689DDWB or MC33689DDWB are the part numbers for device errata. The date code to consider starts the “0428” that means all devices manufactured the week 28 of the year 2004 and after are impacted by this errata.

Description

Sometimes, during a power up sequence, VS1/VS2 increase from 0V to nominal value and as soon as Vdd reaches 3.2V, the Reset terminal rises to 3.2V and then returns low again after few a mV.

The same behavior can be observed for a power down: when Vs1/Vs2 reaches the reset threshold (4.7V typically), the Reset pin goes low and when Vdd reaches 3.2V, the Reset pin goes to 3.2V and goes low again after few a mV.

Workaround

Enable the microcontroller LVI (Low Voltage Inhibit). The microcontroller should be configured to work with the 3V parameters specification until 5V LVI trippoint is enabled.

The behavior described above is dependent on some dynamic conditions like power up/down slew rate on Vbat line. Therefore, the following recommendations could suppress these erroneous reset pulses:

1. Use a filtering capacitor value on the regulator output up to 10µF
2. Do not add external pull up resistor on the reset line

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