56F801

Chip Errata

56F801 Digital Signal Controller

This document reports errata information on chip revision D. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number. This document is a pre-publication draft.
Note: **Differences between Chip Revisions are listed on page 7** and errata information for chip revisions prior to revision D have been archived and can be requested from Freescale Semiconductor Sales.

Chip Revision D Errata Information:

The following errata items apply only to Revision D 56F801 devices. These parts are either marked as DSP56F801 or as PC56F801 with date codes of 0139 or greater (bottom line of marking).

Errata Number	Description	Impact and Work Around
1.2	Quad Timer, when in Pulse Output Mode, at IP clock rate yields n+1 pluses.	Impact: The IP clock rate creates an extra pulse. Work Around: Program n-1 pulses only when operating at Maximum clock rate.
2.2	PWM outputs are not disabled during DEBUG mode.	Impact: Safety considerations if PWM outputs are not disabled prior to entering DEBUG mode. Work Around: Disable PWM outputs prior to entering DEBUG mode. PWM module will continue to operate while in DEBUG mode unless explicitly disabled.
3.2	Program Flash Interface Unit (PFIU) address register read returns wrong value when writing an out-of-row address.	Impact: When verifying the out-of-row write, the PFIU returns the address applied to the Flash pins, which is a concatenation of the ROW register and ADDRESS[4:0] bits. Work Around: None
4.9	Low Analog input voltages to ADC may not be measured properly.	Impact: Inputs < 250mV may yield measurements = 0. Work Around: Bias Analog inputs above 250mV.

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Errata Number	Description	Impact and Work Around
5.9	Optimal ADC setup.	Impact: Better accuracy Work Around: ADC Register ADCR2 DIV field should be set to 4,9, or 14 for optimal performance.
6.2	N register is not available the cycle immediately after it has a value change.	Impact: In the case of an index+ offset move into the N register, N is not available in the cycle immediately following the change in value. Example: move x:(r2+ 3), N lea (R2) +N Work Around: A no-operation (NOP) will need to be inserted between the two statements. As an aid the assembler will be modified to flag this as a problem.
7.2	Timer and GPIO interrupts may be cleared when clearing other interrupts.	Impact: The timer and GPIO modules may have several interrupts cleared by writing to the same register. Unfortunately, clearing one interrupt can unintentionally result in clearing an interrupt that has occurred between the time the status register is read and written back. Work Around: Do not enable multiple interrupts in a single register.
8.2	Slave Mode SPI TE (transmitter empty) flag set too early.	Impact: The problem only occurs in Slave mode when CPHA = 0. The Transmitter Empty (TE) flag may be set too early, thus allowing the user software to write a new data value into the transmit buffer before the current contents are loaded into the transmit shift register. Work Around: Use the receiver full flag as an indication of when to write new data into the transmit buffer.
9.2	Slave Mode SPI transmit shift register data corruption.	Impact: The problem only occurs in Slave mode when an external master has deselected the internal SPI ($\overline{SS}$=1) but it has provided a shift clock to the internal SPI. This scenario is expected in a SPI system with multiple slave devices. The deselected SPI slave transmitter shift register will shift in response to the applied shift clock. This action will cause the existing data in the transmitter shift register to become corrupted. Work Around: Modify communications protocol so the first word returned by the Slave after being reselected ($\overline{SS}$=1 to 0) is discarded. The second and subsequent data words after being reselected are valid.

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Errata Number	Description	Impact and Work Around
10.2	PLL Stabilization Time	Impact: Maximum PLL stabilization time is 200ms under worst case (-40°C) conditions. Typical PLL stabilization time remains at 10ms (25°C and above). Work Around: Insert a 200ms delay after power up to allow the PLL to settle or verify the Loss of Lock bits (LCK0 and LCK1) in the PLL Status Register (PLLSR) are set to 1 prior to program execution.
11.9	Erroneous data can occur at the output of the ADC while operating in the sequential conversion or simultaneous mode with an analog input at the ground potential level.	Impact: When operating the DSP56F801 ADC in the sequential mode with two or more analog inputs being actively driven, one channel at ground and the following inputs converted at another value, the expected digitized results for the input that follows the grounded input is sometimes corrupted. If analog inputs never come with 250 mV of ground the problem never occurs. Work Around: Restrict the analog input so that it never comes within 250 mV of ground OR apply a 250 mV offset to analog input signals.
12.4	SCI communication limited when using the internal relaxation oscillator as chip clock.	Impact: When using the internal relaxation oscillator as the chip clock, SCI communication is limited to a temperature range of 0 to +85 °C. This effect is due to the inherent frequency variation of the relaxation oscillator over temperature combined with frequency tolerances required for SCI communication. This Errata only applies when using the internal relaxation oscillator and does NOT apply when using an external crystal, ceramic resonator, or other clock source. Work Around: None

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Errata Number	Description	Impact and Work Around
13.4	Problem with Automatic Fault Clearing feature of the PWM block is explained below. The fault pins are used to disable any of the PWM output pins. The PWM output pins can be enabled automatically when the fault pin returns to logic zero and a new PWM half cycle begins if the FMODEx control bit is set to logic one. The only issue with this fault protection mechanism is that when the fault pin returns to logic zero, the PWM channel is enabled at the next IP clock cycle instead of the next PWM half cycle. Note that the PWM channel can always be enabled manually after it is disabled if the FMODEx bit is set to logic zero as described in the User's Manual.	Impact: The PWM automatic fault clearing is used for cycle by cycle current limiting. This requires cycle-based fault input control. Due to this issue the fault input continuously changes the voltage thus making it difficult for output devices to respond. Work Around: None
14.6	Serial Boot Loaders prior to version 1.3 do not use the internal relaxation oscillator	Impact: Prior to version 1.3, the Serial Boot Loader application programmed into Boot Flash at the factory does not use the internal relaxation oscillator and requires an external clock source or crystal input. Without the external clock or crystal input, the component will go into a shut down state and communication over the SCI port is impossible. Work Around: In products requiring an internal relaxation oscillator, use components with date codes of 0228 or after, which are programmed with Serial Boot Loader version 1.3 and use a trimmed internal relaxation oscillator. Parts with date codes before 0228 can be reprogrammed and the Serial Boot Loader can be replaced. Reprogramming can be performed with an external bulk loader or in-circuit via the JTAG port by using either the CodeWarrior tool or the JTAG product flash programming tool available on the Freescale website.

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Errata Number	Description	Impact and Work Around
15.6	Components with date codes before 0228 have no factory oscillator trimming	Impact: Factory trimming of the internal relaxation oscillator started with components with date codes of 0228 or greater. Components before this date code do not have a factory trim value stored in the flash information space. Work Around: Applications using an external clock or crystal are not affected. Applications using the internal relaxation oscillator, but not requiring trimmed oscillator accuracy, are not affected. Applications requiring trimmed internal oscillator accuracy can perform the trimming themselves or use components with date codes of 0228 or greater.
16.7	SPI halts on receiver overflow when being used to transmit only.	Impact: Same as description. Work Around: Read receiver in transmit Interupt Service Routine (ISR).
17.7	SPI misses one data word by double loading Xmit register when double buffering.	Impact: Same as description. Work Around: Use only single buffering inside ISR
18.7	Bit counter is not reset on each transmission.	Impact: Must reset part if external master malfunctions in this way. This only happens in slave mode and if external master generates extra clocks. Work Around: External, master SPI must be working correctly and not generate extra clocks.
19.7	Value from data transmit register not moved to shift register.	Impact: When using CPHA=0, the value from the data transmit register does not move to the shift register when the value has been double buffered by a previous transmission. Work Around: Use CPHA=1
20.7	SPI receiver shift register residual after overflow resulting in duplicate transmission.	Impact: Same as description. Work Around: The software should mask the value to the expected word length during access to the receive register.

Chip Revision D Errata Information:

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Errata Number	Description	Impact and Work Around
21.7	Intermittent duplicate transmission in slave mode when CPHA=0.	Impact: Same as description. Work Around: The problem can be eliminated if the SPE control bit is toggled after the SPI receiver full flag is set in the Slave mode or the baud rates are slow enough on the Master side SPI such that the $\overline{SS}$ signal can be de-asserted before the last inactive edge of the SPICK signal.
22.7	While SPI is enabled in master mode and the transmit data register (less than 16 bits) is filled, the OVRF flag stops further transmission.	Impact: This occurs since the clock is common to MOSI and MISO and “1s” are latched into the SPI data register. After transmitting two words, OVRF flag is set while the SPI receive data register is not read by the software. To re-initiate transmission, SPI needs to be disabled and then re-enabled. Clearing the OVRF flag will not re-initiate transmission at this point. Note: This does not occur with 16-bit words. Work Around: Always use read receive data, even if it is to be discarded.
23.8	The interrupt controller uses COPR bit in SIM_RSTSTS register to determine whether to use COP reset vector in the vector table.	Impact: The user must clear this bit at startup after a COP reset, or any subsequent resets will use the COP reset vector. Work Around: Clear the COP Reset bit in the SIM STATUS register.
24.10	With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed.	Impact: When the compare register matches the counter register and is updated before the next timer clock the counter increments/decrements instead of reloading. Work Around: 1. Use both compare registers, such that the compare register that is not active is updated for use in the next count period. 2. Instead of updating the compare register, architect the software so the LOAD register can be updated, with the compare register held constant. A more in depth FAQ can be found on the Freescale website. *freescale.com*
25.10	GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	Impact: Hardware designs that have asynchronous interruptable inputs on the same GPIO port cannot rely on the device to generate the interrupt. Work Around(s): 1. Use different ports for these two interrupts. 2. After writing to the IESR, read the RAW_DATA register to determine if any other inputs have occurred at this exact instant.

Differences between Chip Revisions

Chip Rev. A *Date codes = ≥ 0112 ≤ 0113*	**Chip Rev. B** *Date codes = ≥ 0113 ≤ 0138*	**Chip Rev. C** *Never distributed*	**Chip Rev. D** *Date codes = ≥ 0139*
Intermittent internal data (X memory) RAM corruption.	No intermittent internal data (X memory) RAM corruption. **Corrected**		
Intermittent incorrect data return from Data, Program and BootFLASH modules.	**Corrected**		
Internal data (X memory) RAM intermittently corrupts a memory location while another location is being written.	**Corrected**		
ADC yields incorrect data. If $V_{DDA} \leq 3.15$ volts.	**Corrected**		
Device cannot meet flash data retention specification of 10 years.	Improved flash data retention. Data retention specification of 10 years at 25°C after 10,000 program-erase cycles can be meet.		**Corrected**
Low voltage V_{DDA} may cause inaccurate ADC measurement.	Same as A		**Corrected**
Quad Timer, when in Pulse Output Mode, at IP clock rate yields n+1 pluses. *See errata item 1 for additional information.* *In rev 4.0 this errata was in error in stating it was corrected.*	Same as A		Same as B
Poor offset Voltage measurements.	Improved Offset Voltage numbers		Same as B
Devices cannot meet 80 MHz speed specification when executing program out of flash memory.	**Corrected**		
Slave Mode SPI data is corrupted on the MISO output. *In rev 4.0 this errata was in error in stating it was not corrected.*	Same as A		**Corrected**
PWM outputs are not disabled during DEBUG mode. *See errata item 2 for additional information.*	Same as A		Same as B
PFIU address register read returns the wrong value when writing an out-of-row address. *See errata item 3 for additional information.*	Same as A		Same as B
Low Analog input voltages to ADC may not be measured properly. *See errata item 4 for additional information.*	Same as A		Same as B
Optimizing ADC setup. *See errata item 5 for additional information.*	Same as A		Same as B

Differences between Chip Revisions

Chip Rev. A *Date codes = ≥ 0112 ≤ 0113*	**Chip Rev. B** *Date codes = ≥ 0113 ≤ 0138*	**Chip Rev. C** *Never distributed*	**Chip Rev. D** *Date codes = ≥ 0139*
N register is not available the cycle immediately after it has a value change. *See errata item 6 for additional information.*	Same as A		Same as B
Timer and GPIO interrupts may be cleared when clearing other interrupts. *See errata item 7 for additional information.*	Same as A		Same as B
Slave Mode SPI TE flag set too early. *See errata item 8 for additional information.*	Same as A		Same as B
Slave Mode SPI transmit shift register data corruption. *See errata item 9 for additional information.*	Same as A		Same as B
Invalid clock switch-over sequence will lock up and cannot be reset.	Same as A		**Corrected**
PLL Stabilization Time. *See errata item 10 for additional information.*	Same as A		Same as B
Slow V_{DD} ramp at Power-up (>10ms)	Same as A		**Corrected**
Erroneous data can occur at the output of the ADC while operating in the sequential conversion mode with an analog input at the ground potential level. *See errata item 11 for additional information.*	Same as A		Same as B
SCI communication limited when using the internal relaxation oscillator as chip clock. *See errata item 12 for additional information.*	Same as A		Same as B
PWM automatic fault clearing issue. *See errata item 13 for additional information.*	Same as A		Same as B
Serial Boot Loaders prior to version 1.3 do not use the internal relaxation oscillator. *See errata item 14 for additional information.*	Same as A		Same as B
The factory did not trim the oscillator on components with date codes before 0228. *See errata item 15 for additional information.*	Same as A		Same as B
SPI halts on receiver overflow when being used to transmit only. *See errata item 16 for additional information.*	Same as A		Same as B
SPI misses one data word by double loading Xmit register when double buffering. *See errata item 17 for additional information.*	Same as A		Same as B
Bit counter is not reset on each transmission. *See errata item 18 for additional information.*	Same as A		Same as B

Differences between Chip Revisions

Chip Rev. A *Date codes = ≥ 0112 ≤ 0113*	**Chip Rev. B** *Date codes = ≥ 0113 ≤ 0138*	**Chip Rev. C** *Never distributed*	**Chip Rev. D** *Date codes = ≥ 0139*
Value from data transmit register not moved to shift register. *See errata item 19 for additional information.*	Same as A		Same as B
SPI receiver shift register residual after overflow resulting in duplicate transmission. *See errata item 20 for additional information.*	Same as A		Same as B
Intermittent duplicate transmission in slave mode when CPHA=0. *See errata item 21 for additional information.*	Same as A		Same as B
While SPI is enabled in master mode and the transmit data register (less than 16 bits) is filled, the OVRF flag stops further transmission. *See errata item 22 for additional information.*	Same as A		Same as B
The interrupt controller uses COPR bit in SIM_RSTSTS register to determine whether to use COP reset vector in the vector table. *See errata item 23 for additional information.*	Same as A		Same as B
With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed. *See errata item 24 for additional information.*	Same as A		Same as B
GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written. *See errata item 25 for additional information.*	Same as A		Same as B

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
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Denver, Colorado 80217
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Fax: 303-675-2150
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