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Differences Between the MSC8144 and the MSC815x DSPs

MSC814x and MSC815x are members of the Freescale family of high-end multicore programmable digital signal processors (DSPs). The fourth-generation SC3850 core in the MSC815x DSPs is an evolutionary, binary-compatible enhancement of the SC3400 core used in the MSC814x family. Improvements are also made to the MSC815x DSP core subsystem and peripheral blocks to deliver high performance for targeting the wireless markets, such as 3GPP, TD-SCDMA, 3G-LTE and WiMAX.

This engineering bulletin discusses the differences between the DSP cores and subsystems and the peripheral blocks used in the DSP devices. Unless otherwise noted, MSC814x includes the following devices:

- MSC8144
- MSC8144E

MSC815x includes the following devices:

- MSC8156
- MSC8156E

Contents

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1 Summary of Differences

Table 1 summarizes the differences between the device families. Figure 1 and Figure 2 show block diagrams of the MSC814x and MSC815x device families, respectively.

Table 1. Differences Between the MSC8144 and MSC815x DSP Families

Feature	MSC8144	MSC8144E	MSC8156	MSC8156E
Target Market	– Packet telephony – Wireless – Video transcoding		– Wireless • 3GPP • TD-SCDMA • 3G-LTE • WiMAX • HSPA+	
Technology	– 90 nm SOI		– 45 nm SOI	
Package	– 29 mm x 29 mm FC-PBGA		– 29 mm x 29 mm FC-PBGA	
DSP Cores	– Four SC3400 cores – Up to 1 GHz – Each core has 4 ALUs, each capable of 16 x 16 MAC operations		– Six SC3850 cores – Up to 1 GHz – Each core has 4 ALUs, each capable of two 16 x 16 MAC operations (dual multipliers) – New instructions • Dual multiply support • Improved extended precision multiplication • Complex arithmetic • FFT support • Improved comparing • Improved cache control – New numerical formats • 20-bit packed fractional • Byte fractional – Several microarchitectural improvements, including: • Enlarged BTB • Improvements in hardware loops • Enhanced speculation	
L1 ICache	– 16 KB per core – 8 way set associative – 256 byte cache line		– 32 KB per core – 8 way set associative – 256 byte cache line – Touch loading support – Hardware next line prefetch for instruction only	
L1 DCache	– 32 KB per core – 8 way set associative – 256 byte cache line		– 32 KB per core – 8 way set associative – 256 byte cache line – Touch loading support – Cache maintenance instructions	

Table 1. Differences Between the MSC8144 and MSC815x DSP Families (continued)

Feature	MSC8144	MSC8144E	MSC8156	MSC8156E
L2 Cache/ M2 Memory	– Separate L2 ICache and M2 memory outside DSP subsystem – L2 ICache • 128 KB shared by all cores • 8 way set associative • 256 byte cache line • Pseudo-least recently used line replacement – M2 memory • 512KB shared by all cores • Supports atomic operation – 400 MHz operation – ECC protection		– Unified 512KB L2 Cache/M2 memory per DSP subsystem • M2 can be allocated in 64 KB blocks up to 512 KB • Remaining portion used as L2 Cache – L2 Cache • Unified for instruction and data • 8 way set associative • 64 bytes per cache line • Pseudo-random line replacement • Multichannel software prefetch • Cache partitioning by way and address • Read-with-intent-to-write – M2 memory • up to 512 KB private per core • No atomic operation – 1 GHz operation – ECC protection	
M3 Memory	– 10 MB eDRAM on separate die – Operates at 400 MHz – ECC protection – No atomic operation		– 1056 KB internal SRAM – Operates at 500 MHz – 1024 KB can be turned off for power savings – ECC protection – Supports atomic operation	
DDR SDRAM Controller	– Single DDR controller – 400 MHz data rate – DDR1 and DDR2 support – 32/40-bit or 16/24-bit data bus – x8 or x16 memory devices – 2 chip selects (physical banks) – 16 MB to 1 GB physical bank size – 4 simultaneous open pages – 4 beat burst		– Dual DDR controllers – 800 MHz data rate – DDR2 and DDR3 support – 64/72-bit or 32/40-bit data bus – x8, x16 or x32 memory devices – 2 chip selects per controller, 4 total (physical banks) – 16 MB to 4 GB physical bank size – 32 simultaneous open pages – 4 or 8 beat burst – Chip select interleaving – Write leveling for DDR3	
Memory Management Unit (MMU)	– Memory attributes and translation table • 20 data segment descriptors • 12 program segment descriptors		– Memory attributes and translation table • 20 data segment descriptors • 12 program segment descriptors – Improved query mechanism – New flexible segment model – New memory region attributes including L2 cache instruction/data policy	
Clocks	– Shared (CLKIN) – Global (PCI_CLK_IN) – Differential serial RapidIO® clocks		– Shared (CLKIN) – 2 sets of differential serial RapidIO clocks	
PLL	– Core PLL – Global PLL – System PLL – SerDes PLL		– 3 system PLLs – 2 SerDes PLLs	
Boot ROM and Boot Modes	– 96 KB – Boot from • I^2C • Serial RapidIO interface • Ethernet • PCI		– 96 KB – Boot from • I^2C • Serial RapidIO interface • SPI • Ethernet – Simple Ethernet	

Table 1. Differences Between the MSC8144 and MSC815x DSP Families (continued)

Feature	MSC8144	MSC8144E	MSC8156	MSC8156E
Debug and Profiling Unit (DPU)	– Basic DPU defined as part of the SC3400 core subsystem		– Adds L2 cache event profiling	
On-Chip Emulation Port (OCE)	– OCE functionality defined as part of the SC3400 core subsystem		– Adds address detection of data cache instructions	
Baseband Algorithm Accelerator	None		– Multi-Accelerator Platform Engine for Baseband (MAPLE-B) • Turbo decoding with CRC, rate de-matching • Viterbi decoding • FFT/iFFT processing – DFT/iDFT processing	
Security Engine Controller (SEC)	– None	– Supports SEC 2.1 – Up to 200 MHz	– None	– Supports SEC 3.1.0 – Up to 250 MHz – SNOW algorithm
Chip-Level Arbitration and Switching System (CLASS)	– 3 CLASS interconnects • Two 128-bits 400 MHz • One 64-bits 200 MHz – 14 initiators, 11 slaves		– Single CLASS interconnect – 128-bits wide at 500 MHz – 12 initiators, 8 slaves	
Interrupts	– 4 non-maskable virtual interrupts		– 8 non-maskable virtual interrupts – Fast intercore interrupts – Virtual interrupts to QUICC Engine subsystem and MAPLE-B – TDM interrupts to QE subsystem – RapidIO interrupts to MAPLE-B – MAPLE-B interrupts to DSP subsystem	
Direct Memory Access Controller (DMA)	– Data transfer to/from M2, M3, DDR – 16 bidirectional channels – Full-duplex operation – 400 MHz operation		– Data transfer to/from M2, M3, DDR – 16 bidirectional channels – Full-duplex operation – 500 MHz operation – Two sets of DMA external request and DMA external done indication pins	
Ethernet Controller	– Dual Gigabit Ethernet controllers • SGMII • RGMII • RMII • SMII • MII		– Dual Gigabit Ethernet controllers • SGMII • RGMII	
ATM Controller	– UTOPIA level II supports 8/16 bits – ATM adaptation layers support AAL0, AAL2, AAL5 protocols in hardware		– None	
SPI Controller	– Full-duplex operation – Master or slave mode – Multimaster environment		– Full-duplex operation – Master or slave mode – Multimaster environment	
TDM Interface	– 8 TDM modules – Up to 256 bidirectional channels per TDM – Up to 256 Mbps for all TDM modules		– 4 TDM modules multiplexed with the RGMII interfaces – Up to 256 bidirectional channels per TDM – Up to 64 Mbps for all TDM modules	
PCI Controller	– PCI rev. 2.2 compliant – 33 MHz and 66 MHz – 32-bit PCI interface		– None	

Table 1. Differences Between the MSC8144 and MSC815x DSP Families (continued)

Feature	MSC8144	MSC8144E	MSC8156	MSC8156E
High Speed Serial Interface (HSSI)	– Not included as a separate module		– Supports two Serial RapidIO controllers, one remote messaging unit, two DMA units, two DMA to OCN bridges,.PCI Express interface, and two 4-channel SerDes ports. – Dual 4-channel SerDes ports multiplexing two 1x/4x Serial RapidIO interfaces, one 1x/2x/4x PCI Express interface, and two SGMII interfaces (controlled by the QUICC Engine™ subsystem).	
Serial Rapid IO Controller	– Single serial RapidIO controller – 1x or 4x 3.125 Gbaud – One RMU – One DMA controller – One DMA-to-OCN bridge – One SerDes PHY multiplexed with SGMII		– Two serial RapidIO controllers with one RMU – 1x or 4x 3.125 Gbaud – Pass-through between the two ports	
PCI Express Controller	None		– 1x, 2x, or 4x 2.5 GHz serial interface – Configurable as RC or EP – Software message generation	
Software Watchdog	– 4 software watchdog timers		– 8 software watchdog timers	
Power Supplies	– 1.0 V for core, PLL – 1.2 V for M3 – 1.8 V for DDR2 mode – 2.5 V and 3.3 V for I/O		– 1.0 V for core, PLL, M3, RapidIO controller, MAPLE-B – 1.5 V for DDR3 mode – 1.8 V for DDR2 mode – 2.5 V for I/O	

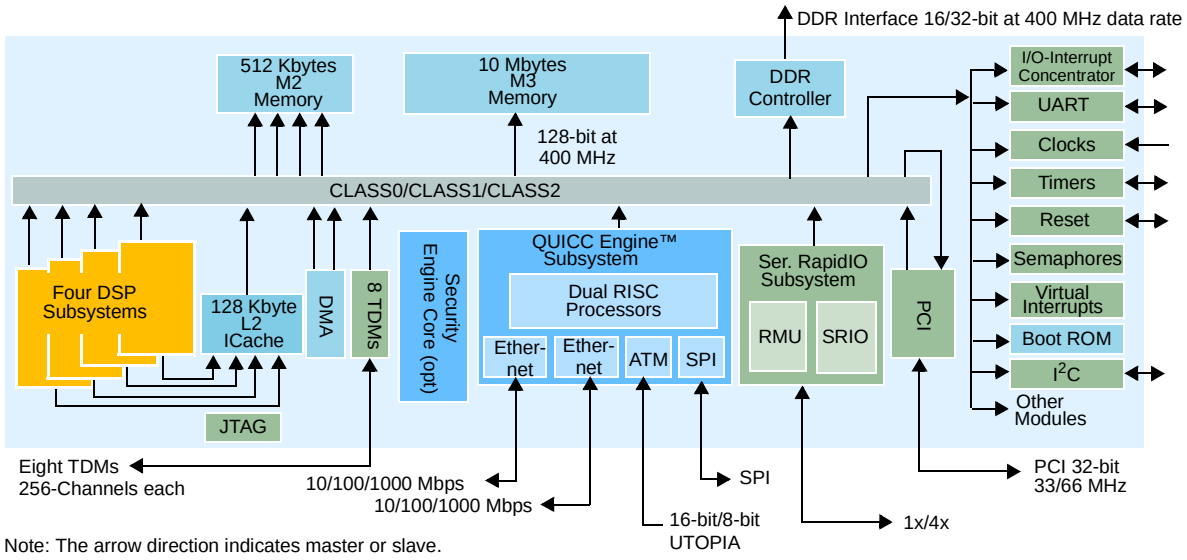

Figure 1. MSC814x Block Diagram

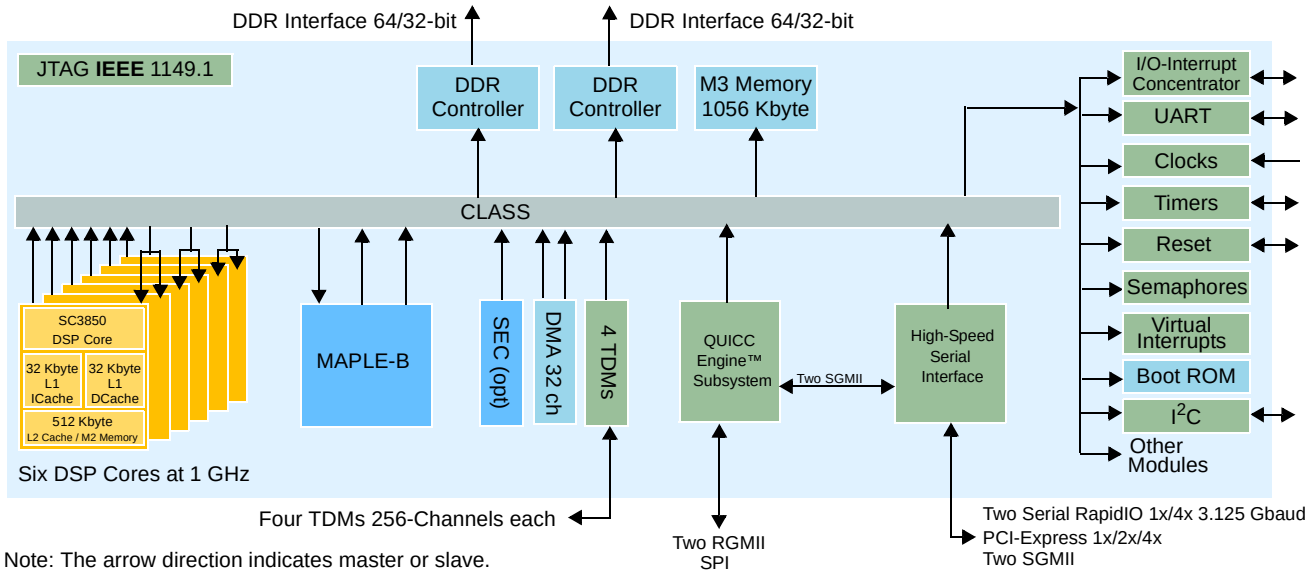

Figure 2. MSC815x Block Diagram

2 Target Markets

The MSC814x multicore DSPs high voice and video channel densities are optimized for targets the packet telephony, wireless, and video transcoding applications. The MSC815x devices are designed to support expanding wireless markets, such as 3GPP, TD-SCDMA, 3G-LTE, WiMAX and HSPA+.

3 Process Technology

The MSC814x is manufactured in CMOS 90 nm silicon-on-insulator (SOI) process technology while the MSC815x is manufactured in CMOS 45 nm SOI process technology for power and cost reduction and performance increase.

4 Package

Both the MSC814x and MSC815x come in a 29 mm x 29 mm Flip Chip Ball-Grid Array (FC-BGA) package.

5 Core Differences

The MSC815x SC3850 core is an evolutionary, binary-compatible enhancement of the MSC814x SC3400 core. This section summarizes the changes and enhancements of the SC3850 over the SC3400 core. For detailed information, see the following documents:

- *SC3400 DSP Core Reference Manual*
- *SC3850 DSP Core Reference Manual*

NOTE

These documents are only available under NDA. Contact your local representative or sales office to access these documents. Appendix C in the SC3850 DSP Core Reference Manual is a detailed list of differences between the two cores.

5.1 Performance

The MSC814x devices features four StarCore® SC3400 DSP cores operating up to 1 GHz. The four cores deliver a peak performance of up to 16 GMAC operations (16-bit × 16-bit) per second.

The MSC815x devices feature six StarCore SC3850 cores, respectively, both operating up to 1 GHz. With the new dual-multiplier feature, the six SC3850 cores deliver up to 48 GMACs per second.

5.2 Dual Multipliers

The SC3400 supports a single multiplier in each ALU and allows up to four 16-bit x 16-bit MAC operations per cycle. The SC3850 dual multipliers in each ALU double the throughput of MAC operations per cycle over the SC3400 core. Four dual multiply-accumulate MACD instructions can be performed in parallel by each core, resulting in a throughput of eight 16 × 16 MAC operations per cycle as shown in **Table 2**.

A dual multiply instruction can accumulate the two 16-bit × 16-bit multiplications in the same 40-bit destination register, or it can accumulate the two multiplications independently in two 20-bit portions of the destination in SIMD2 fashion. Specialized variants of multiplication instructions double the performance of complex multiplication and extended precision operations.

Table 2. SC3850 Dual Multiply Performance

Operation	Precision	Results per Cycle	
		SC3400	SC3850
Real Multiply	16 × 16	4	8
	16 × 32	2	4
	32 × 32	1	2
Complex Multiply	16 × 16	1	2
	16 × 32	0.5	1

5.3 New Dual 20-bit Packed Fractional Format

The SC3850 adds a new dual 20-bit packed fractional format in which a data register holds two 16-bit fractional operands. Each operand uses 4-bits of the extension portion of the data register as guard bits. The resulting 20-bits are referred as the wide-high (WH) and wide-low (WL) portions as shown in Figure 3. This format can also be used to store a complex number. By convention, the WH portion holds the real part and the WL portion holds the imaginary part of a complex number.

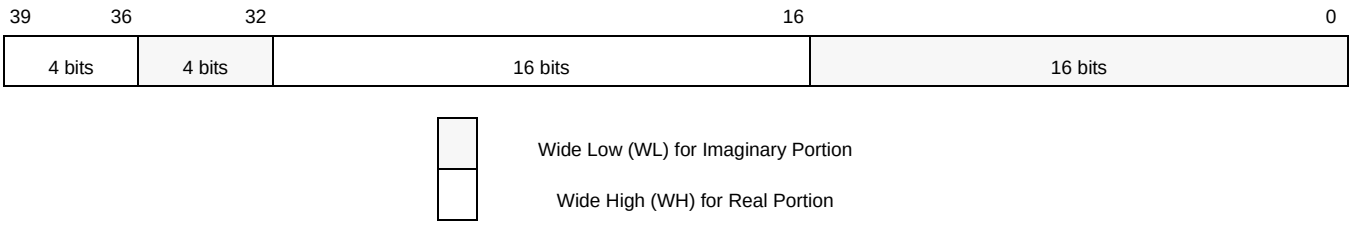

Figure 3. Dual 20-bit Packed Format

5.4 New and Expanded SIMD2 Instructions

The SC3850 adds new SIMD2 instructions to support the new dual-multiplier capability. These instructions generate two independent results that are stored in packed 20-bit format in the destination register.

5.5 New Instructions for Complex Arithmetic

The SC3850 adds efficient support for complex multiplication, generally doubling the performance of the SC3400. The complex numbers are packed as 20-bit real part and 20-bit imaginary part in the WH and WL portions, respectively, of the same register.

5.6 New Instructions for Extended Precision Multiplication

The SC3850 adds support for accelerating extended precision multiplication for mixed precision (16×32 bits) and double precision (32×32 bits) multiplication of both fractional and integer data types (signed and unsigned), generally doubling the performance of the SC3400 for these operations.

5.7 New Instructions for FFT Support

To improve cycle performance and better signal-to-noise ratio over the SC3400, the SC3850 adds instructions for FFT calculations of the real and imaginary portions of a butterfly result.

5.8 Instructions for Improving Control Code Performance

In the SC3850 core, several new instructions were added to improve control code performance, including instructions for more efficient condition processing and faster pointer-relative access.

5.9 New Byte-Fractional Format

The SC3850 adds a new byte fractional format which is supported by MOVE instructions marked with a .BF suffix. The fractional byte is aligned to the right of the decimal point as shown in Figure 4. When loading a fractional byte from memory, the data register is sign-extended into the extension bits and zero padded to the right.

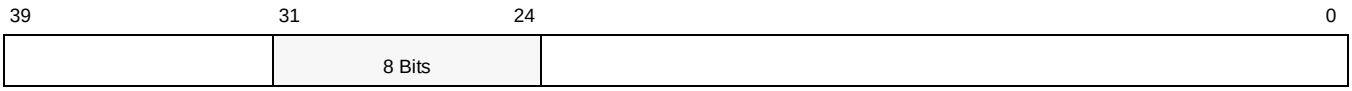

Figure 4. Fractional Byte Format

5.10 New Instructions for Accessing Byte Fractional Format Data

The SC3850 also adds several MOVE instruction variants for moving of a single or multiple fractional bytes between memory and data registers.

5.11 New Instructions for Cache Control

The SC3850 adds new data and program cache control instructions to allow cycle-efficient control of prefetching, cache coherency management and memory management.

5.12 Microarchitecture Improvements

The SC3850 core has several micro-architecture improvements that enhance its cycle performance, including:

- Improvements in the hardware loop mechanism
- Enlargement of the BTB
- Deeper execution speculation

6 DSP Subsystem Differences

The SC3400 and SC3850 DSP subsystems are platforms built around the cores and allow to be integrated into a broad range of SoCs. Figure 5 and Figure 6 show the block diagrams of the SC3400 and SC3850-based DSP subsystems.

In the MSC814x, the DSP subsystem includes the SC3400 core, the instruction and data caches, the memory management unit (MMU) for task protection and address translation, the Embedded Programmable Interrupt Controller (EPIC) for interrupt processing, the Timer, the On-Chip Emulator (OCE) and Debug and Profiling Unit (DPU), and the interface that links to the other functional blocks in the MSC8144E.

The DSP subsystem in the MSC815x differs mainly in that it includes the SC3850 core and a unified M2 RAM/L2 Cache, and supports touch loading to the caches. This section will discuss the differences between the two subsystems.

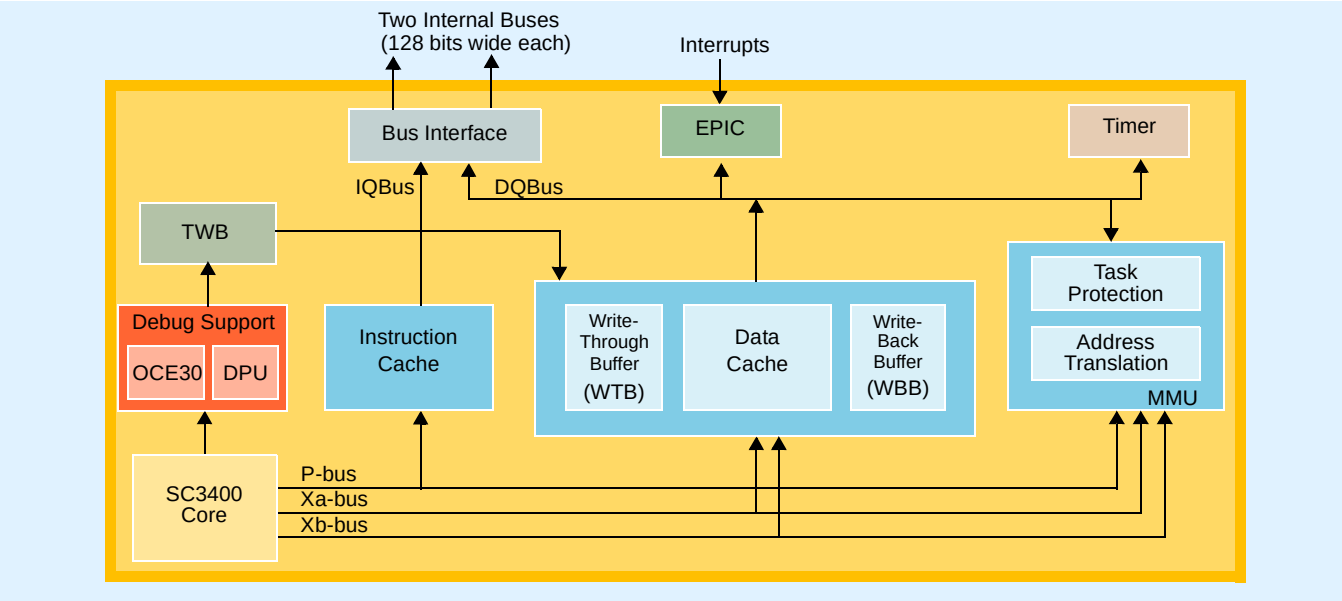

Figure 5. StarCore SC3400 DSP Subsystem Block Diagram

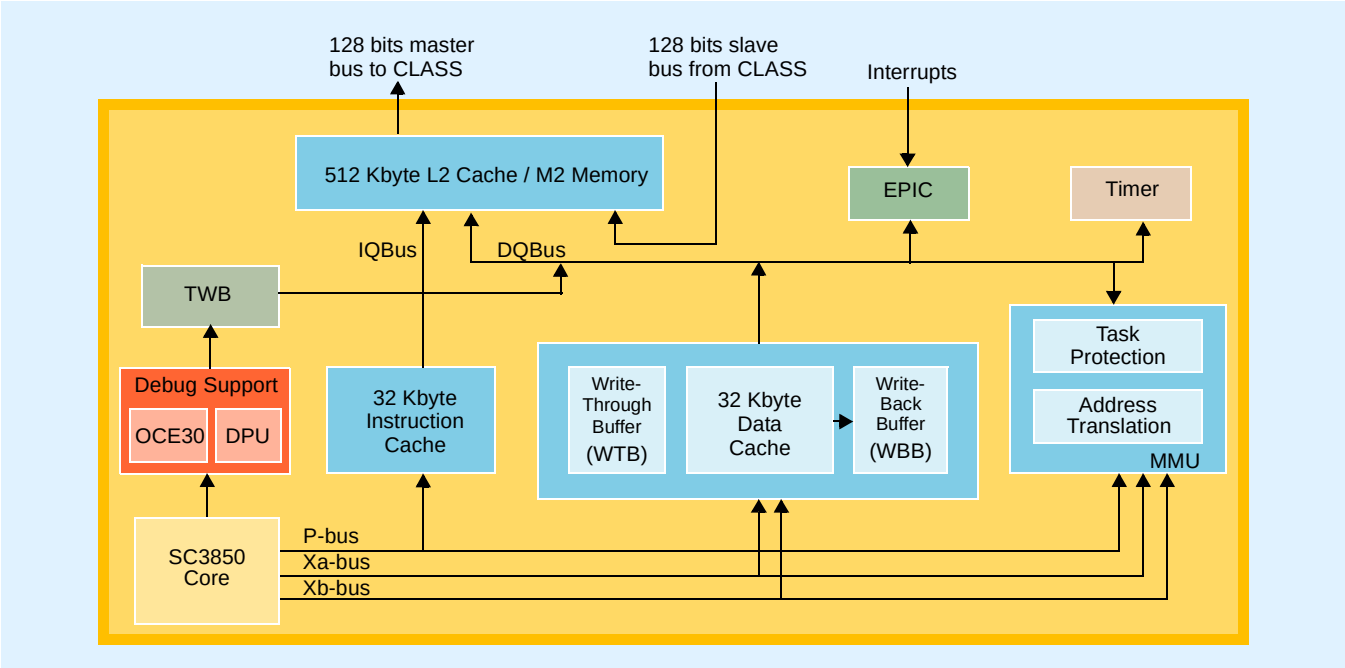

Figure 6. StarCore SC3850 DSP Subsystem Block Diagram

6.1 L1 Instruction Cache

The SC3400 DSP subsystem L1 instruction cache is 16 KB in size and is 8-way set associative with 8 lines per way. The SC3850 DSP subsystem L1 ICache is double in size at 32 KB and is also 8-way set associative with 16 lines per way. The SC3850 DSP subsystem adds several instructions for maintenance and support of the instruction cache.

6.2 L1 Data Cache

Both the SC3400 and SC3850 DSP subsystems L1 data caches are organized in the same way, with a size of 32 KB and 8-way set associativity. However, the SC3850 DSP subsystem adds support for several data cache maintenance instructions.

6.3 Memory Management Unit (MMU)

In the SC3400 DSP subsystem MMU, the Aligned Segment model supports segment sizes of 256 bytes up to 4 GB and restricts the base address to be aligned to the segment size which can result in wasted memory.

The SC3850 DSP subsystem MMU offers more flexible mapping of segment descriptors with the new Flexible Segment model. Segment descriptors now also hold the L2 caching policy. In addition, some core instructions were added to help in the maintenance of the MMU.

6.4 New L2 Unified Cache/M2 Memory

In the MSC814x, the M2 memory is outside of the SC3400 DSP subsystem and it is accessible to any of the DSP core subsystems or other initiators, including the L2 ICache, DMA controller, TDM, QUICC Engine subsystem, serial RapidIO subsystem and the PCI controller. The M2 memory is 512 KB in size, 128-bits wide, and can be accessed at 400 MHz. The shared 128 KB, 8-way set associative L2 ICache fetches code from a higher level memory and enables the cores to fetch code from level 2 cache with reasonable degradation, instead of the high miss penalty to access higher level memory directly.

In the MSC815x, each SC3850 DSP subsystem includes a 512 KB L2 unified cache/M2 memory which can be configured as a full M2 memory, as full L2 cache or combinations of L2/M2. This feature allows flexibility between the DMA and cache software models. Allocation of M2 memory is done in 64 KB blocks from 0 to the full 512 KB memory space. Memory space not allocated as M2 memory is used as L2 cache. Address partitioning can be done in run-time to maximize user flexibility. When configured as M2 memory, this area is accessible from the DMA port.

The L2 cache is organized as 8-way set associative with 64 bytes per cache line. It is shared between instruction and data. The L2 fetch unit fetches cacheable accesses from the M3 and DDR memories. The L2 cache controller supports non-cacheable, cacheable write-through, cacheable write back, adaptive write policies. It also supports ECC by adding seven check bits to each 64-bit memory word.

6.5 On-Chip Emulator (OCE)

The OCE blocks of the SC3400 and SC3850 DSP subsystems provide debug capabilities such as stepping through code, examining core and peripheral registers and memory locations, setting breakpoints, and tracing of program execution.

In both subsystems, the Address Detection Unit in the OCE allows debug events to be generated when the it detects data accesses by the core or when it detects program accesses from a specified address. The SC3850 subsystem adds a new feature that allows detection of data cache instructions.

6.6 Debug and Profiling Unit (DPU)

The DPU supports debugging and profiling of the SC3400 and SC3850 DSP subsystems and can work in cooperation with the OCE block. It allows counting of system events such as clock cycles, stalls, instruction and data cache hits and misses, and more. The DPU includes six counters, organized into two groups of three counters. The virtual trace buffer (VTB) allows trace data to be written to user-defined memory.

The SC3850 DSP subsystem DPU adds event counting features for the L2 cache controller. The following events can be profiled:

- Instruction access misses and hits to L2 cache
- Data access misses and hits to L2 cache
- Software prefetch hits and misses to L2 cache
- DMA access hits and misses to L2 cache

7 Reset

The reset and control signals provide different options for the MSC814x by configuring various modes and features during power-on reset. Most of these features are configured by loading reset configuration words to the device and sampling configuration inputs during the reset sequence.

When the MSC814x is configured to load the reduced reset configuration word (RCW) from external pins, it latches some of the bits of the RCW from the RC0:RC16 pins which are sampled during the assertion of $\overline{\text{PORESET}}$. The other bits of the RCW are loaded from default hard-coded values. When the MSC815x is configured to load the reduced RCW from external pins, some of the RCW bits are loaded from pins RC0:RC21 and the other bits are loaded from default hard-coded values. However, if the MSC815x is configured to load multiplexed RCW from external pins, all of the RCW bits are latched from the pins RC0:RC15. The 64 bits of the RCW are loaded in four passes using RC0:RC15. The $\overline{\text{RCW\_LSEL}}$[3:0] pins select the loading of each of the 16-bit lane.

The RCFG_CLKIN_RNG signal in the MSC814x is sampled at the deassertion of $\overline{\text{PORESET}}$ to identify the range of the CLKIN input. When loading the RCW bits from a I^2C EEPROM, the frequency is specified by the value of RCFG_CLKIN_RNG. The MSC815x does not have the RCFG_CLKIN_RNG pin.

8 Clocks

The MSC814x has three input clocks:

- CLKIN is the shared input clock to the system PLL and can also be input to the core and global PLLs.
- PCI_CLK_IN is the global input clock and can be input to the global PLL.
- SRIO_REF_CLK/$\overline{\text{SRIO\_REF\_CLK}}$ are the differential serial RapidIO reference clocks.

Since the MSC815x does not have a PCI controller, it does not have a PCI_CLK_IN. However, it has two sets of SRIO_REF_CLK/$\overline{\text{SRIO\_REF\_CLK}}$ differential serial RapidIO reference clocks as well as the CLKIN primary clock input.

9 PLL

The MSC814x has four PLLs:

- System PLL that generates the clocks for the CLASS, QUICC Engine subsystem, and PCI clock source.
- Core PLL that generates clocks to the DSP core subsystems
- Global PLL that generates clocks to the DDR controller, M3 and PCI.
- SerDes PLL generates the SerDes clock.

The MSC815x has three system PLLs and two SerDes PLLs.

10 Boot Modes

The MSC814x supports booting via I^2C, serial RapidIO port, PCI, and Ethernet interfaces. The MSC815x supports booting via I^2C, SPI, serial RapidIO port and Ethernet interfaces.

The MSC815x also adds a new simple Ethernet boot mode in which an Ethernet master waits for a handshake packet from the MSC815x boot loader. The Ethernet master sends a block of data in simple Ethernet block format which maps the data content to a memory location in the MSC815x. The boot code processes the data block and places it in its destination in memory. The Ethernet master signals the end of the transfer by writing to a specific memory.

11 Boot ROM

Both the MSC814x and MSC815x includes a 96 KB boot ROM.

12 M3 Memory

The MSC814x M3 memory is 10 MB and can be used for both program and data. It is 128-bits wide and runs at 400 MHz. The M3 memory is ECC protected for soft errors. Atomic accesses are not supported in M3 memory. M3 memory must be initialized after reset deassertion.

The MSC815x M3 memory is 1056 KB and can be used for storing critical program and data shared between the cores and the device peripherals. The M3 memory is 128-bits wide and runs at 500 MHz. It supports ECC protection for soft errors.

1024 KB of M3 can be powered down to decrease power consumption. The other 32 KB remains enabled to support hardware semaphores. This portion of memory also supports atomic accesses.

13 DDR Controller

The MSC814x includes a DDR controller that supports x8 or x16 DDR1 or DDR2 memory devices. The interface is 16/32-bits wide and supports ECC. It supports up to 400 MHz data rate. Two chip select signals support up to two physical banks of memory, each from 16 MB to 1 GB in size. Page mode support of up to 4 simultaneous open pages can reduce access latencies for page hits. Read and write accesses to memory are burst-oriented, with four beats per burst.

The MSC815x provides dual DDR controllers that support x8, x16 or x32 DDR2 or DDR3 memory devices. The interface is 32/64-bits wide and supports ECC. For DDR3 memory devices, the write leveling feature is supported to correct data alignment at the destination. Data rate is increased to 800 MHz. A total of four chip select signals (two chip selects per DDR controller), each supporting up to four physical banks of memory from 16 MB to 1 GB in size. The number of simultaneous open pages is increased to 32 to dramatically reduce access latencies for page hits. Pread and write accesses to memory are burst-oriented, wit four or eight beats per burst.

14 CLASS

The MSC814x features the CLASS interconnect between various initiators and targets. It is composed of three CLASS modules. CLASS0 and CLASS1 are both 128-bits wide and operate at 400 MHz. CLASS2 is 64-bits wide and operates at 200 MHz.

The MSC815x uses a single CLASS interconnect. In contrast to the MSC8144E in which each of the DSP core subsystem, a CLASS0 initiator, needs to go through CLASS1 to access the higher system M3 and DDR memories, the MSC815x allows each of the SC3850 subsystems to go through a single interconnect and hence latency is reduced.

The MSC815x CLASS is 128-bits wide and operates at 500 MHz. The initiators include

- 4 or 6 SC3850 subsystems
- 2 MAPLE-B bridges
- 2 DMA ports
- SerDes bridge shared by the 2 Serial RapidIO, PCI Express, 2 SGMIIs
- Peripheral bridge shared by the 4 TDMs, SPI, RGMII, SGMII and JTAG

The targets include:

- MAPLE-B
- CCSR
- 2 or 3 SC3850 subsystem bridges (two DSP subsystems per bridge)
- 2 DDR controllers
- M3 memory

15 DMA Controller

Both the MSC814x and MSC815x support 16 bidirectional channels and full-duplex operation. The MSC815x adds DMA external request DRQ0:DRQ1 and DMA external done indication DDN0:DDN1 pins. Each DRQ pin can be used by an external requestors to request access from each of the source or destination DMA channel. Each DDN pin can be driven by any of the source or destination DMA channel.

16 High Speed Serial Interface (HSSI)

The MSC814x family does not have a separate subsystem to manage the SerDes interface. The management functionality for this port is includes as part of the Serial RapidIO controller block.

The MSC8156x family provides the high speed serial interface subsystem that incorporates two Serial RapidIO controllers, one remote messaging unit (RMU), two dedicated DMA controllers, two DMA-to-OCN bridges, a PCI Express controller, and dual 4-channel SerDes ports that are shared by the two RapidIO interfaces, the PCI Express interface, and the two SGMII ports.

17 Serial RapidIO

The MSC814x includes a Serial RapidIO controller, one remote messaging unit (RMU), one dedicated DMA controller, and one SerDes port that supports 1x/4x RapidIO operation up to 3.125 Gbaud and is multiplexed with the two SGMII ports. The RapidIO controller connects to the CLASS2 system through a 64-bit port.

The MSC815x includes two Serial RapidIO controllers and one RMU within the HSSI. The dual HSSI ports support 1x/4x RapidIO operation up to 3.125 Gbaud. The HSSI includes pass-through support between the two RapidIO ports to eliminate the need for a an on-board serial RapidIO switch.

18 PCI Express

The MSC814x does not support PCI Express. Instead, it supported PCI rev 2.2 at 33 MHz or 66 MHz.

The MSC815x HSSI subsystem includes a PCI Express controller that connects to a 2.5 GHz serial interface configurable for 1x, 2x, or 4x data transfer. It can be configured to operate as a root complex (RC) or an endpoint (EP) device. Software message generation is supported in both RC and EP modes. The PCI Express controller supports three inbound and four outbound windows.

19 Ethernet Controller

The MSC814x QUICC Engine subsystem includes two Ethernet controllers to support 10/100/1000 Mbps operations via MII/RMII/SMII/RGMII/SGMII protocols. The serial data rate at 1000 Mbps is supported through the RapidIO SerDes port.

The MSC815x QUICC Engine subsystem includes two identical Gigabit Ethernet controllers. Each controller supports 1000 Mbps RGMII (multiplexed with the TDM signal lines) and 1000 Mbps SGMII interface through the HSSI SerDes ports.

20 Asynchronous Transfer Mode (ATM) Controller

The MSC814x QUICC Engine subsystem includes an ATM controller that supports UTOPIA level II 8/16 bits at 25/50 MHz in UTOPIA/POS mode with adaptation layer support for AAL0, AAL2, and AAL5.

The MSC815x QUICC Engine subsystem does not include an ATM controller.

21 Serial Peripheral Interface (SPI) Controller

Both the MSC814x and MSC815x families include an SPI controller as part of the QUICC Engine subsystem with a four-wire interface and supports full-duplex operation. It can operate in master or slave mode and supports multi-master environment. It can also be used for booting the devices from an EEPROM.

22 Time Division Multiplex (TDM) Interface

The MSC814x supports eight independent TDM modules with programmable word size of 2/4/8/16-bits, hardware-based A-law/µ-law conversion, and up to 256 channels per TDM. The interface operates up to 128 Mbps for all TDM modules.

The MSC815x has four TDM modules with the same features as the MSC814x TDM. The signals are multiplexed with the RGMII signal lines.

23 Multi-Accelerator Platform Engine—Baseband (MAPLE-B)

The MAPLE-B baseband accelerator is a new block on the MSC815x. It consists of a programmable system interface (PSIF) with DMA capabilities and accelerators for Turbo, Viterbi, FFT/iFFT, DFT/iDFT, and CRC algorithms. The PSIF has two 64-bit wide MBus master ports to transfer input and output data to and from system memory. It also has a 64-bit MBus slave port to allow any core to access the PSIF internal memory. To reduce overall power consumption, the MAPLE-B power can be disabled internally.

24 Security Engine (SEC)

The MSC8144E/EC SEC version 2.1 performs computationally intensive security functions including key generation and exchange, authentication and bulk encryption. It operates at up to 200 MHz. It is optimized to process all algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS and 3GPP.

In addition to the above protocols, the MSC815xE SEC version 3.1.0 also includes the SNOW algorithm which is essential for 3GLTE applications.

25 Interrupts

The MSC815x has four more virtual non-maskable interrupts over the MSC814x for a total of 8 VNMIs. The MSC815x also features a mesh of fast intercore interrupts to enhance communication between the DSP core subsystems. Two interrupts from each of the SC3850 core subsystems connect to each of the DSP core subsystems, including itself.

The MSC815x adds TDM interrupts and two virtual interrupts that connect to the QUICC Engine subsystem. It also adds two Rapid I/O interrupts and two virtual interrupts that connect to the MAPLE-B. Two Rapid I/O inbound mail box interrupts allow the MAPLE-B to communicate directly with the Rapid I/O on inbound traffic. A Rapid I/O outbound doorbell interrupt also connects to the MAPLE-B. Interrupts from MAPLE-B’s processing elements (PE) also directly connect to the DSP subsystem.

26 Software Watchdog Timers

The MSC8144E includes four identical watchdog timers for asserting a hardware reset or machine-check interrupt. The MSC8156E includes eight software watchdog timers.

27 Power Supplies

Neither the 1.2 V nor 3.3 V power supply is required for the MSC815x family. The MSC815x M3 memory requires 1.0 V which also powers the core, PLL, Rapid I/O and MAPLE-B blocks. The MSC815x only uses 2.5 V for I/O. The MSC815x dual DDR controllers require a 1.5 V power supply when running in DDR3 mode. For DDR2 mode, the MSC815x requires 1.8 V.

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