Migrating from the GB60 series to the GB60A series

by: Scott Pape
Systems and Applications Engineering
Microcontroller Division

Overview

This document will explain the differences to be aware of when migrating from the MC9S08GB60, MC9S08GB32, MC9S08GT60, and MC9S08GT32 devices to the MC9S08GB60A, MC9S08GB32A, MC9S08GT60A and MC9S08GT32A devices. For the remainder of this document, GB60 series will refer to the original non-"A" devices and GB60A series will refer to the newer "A" suffix devices.

Much of the functionality and performance of the GB60 series and the GB60A series will be identical. However, there are several differences designers should understand when migrating to the GB60A series.

FLASH Programming Voltage

The GB60 series has a minimum V_{DD} requirement for erasing and programming the FLASH, equal to 2.1 V. The GB60A series eliminates this minimum V_{DD} requirement. On the GB60A series, the FLASH can be programmed and erased across the full operating voltage range of the MCU, or 1.8 V to 3.6 V.

Flash Block Protection: 60K Devices Only

The GB/GT60 FLASH block protection has a redundant setting. On the GB/GT60A, the redundant setting is used to add a new protection option.

On the GB/GT60, when protection is enabled by setting the FPDIS bit, setting the FPS2:FPS1:FPS0 bits to 1:1:1 protects the same range as 1:1:0, which is locations $8000 to $FFFF.

On the GB/GT60A, setting the FPS2:FPS1:FPS0 bits to 1:1:0, protects the same range as on the GB/GT60. However, setting the bits to 1:1:1 protects locations $182C to $FFFF, leaving locations $1080 to $17FF open to reprogramming.

This new protection option is useful for protecting the main user program area while leaving a small section of 1920 bytes available for data storage.

freescale™ semiconductor

Internal Clock Generator: High Gain Oscillator Option

The GB60 series only has a low-power external oscillator, designed for the low current consumption. The GB60A series has a second external oscillator option: a high gain external oscillator which provides improved noise immunity in the oscillator circuit. The low-power oscillator is also available for power-sensitive applications.

This new oscillator option available on the GB60A series is selected by a new control bit in the ICG control register 1 (ICGC1): the HGO bit. HGO is bit 7 of the ICGC1 register, formerly an unimplemented bit that always read ‘0’. The reset value is ‘0’, which selects the low-power oscillator option—which is consistent with the GB60 series external oscillator.

Setting HGO to ‘1’ selects the high gain external oscillator which increases the voltage swing across the external crystal or resonator, making it more immune to external noise.

The values of the feedback and series resistors for the external oscillator will be different in most cases between HGO=0 and HGO=1. Consult the ICG DC Electrical Specifications table in the MC9S08GB60A data sheet for the proper values.

Internal Clock Generator: Low-Power Oscillator Maximum Frequency

On the GB60 series, the external oscillator’s maximum frequency is 10 MHz when in FEE mode and 16 MHz when in FBE mode.

On the GB60A series, when HGO=1, the same maximum frequencies apply. However, when HGO=0, the maximum frequency is 8 MHz in FEE and FBE modes.

Internal Clock Generator: Loss-of-Clock Disable Option

The ICG module has a clock monitor which will generate a loss-of-clock signal when either the reference clock or the DCO clock does not meet minimum frequency requirements. This signal is used to generate either a reset or an interrupt, depending on the settings in the ICGC2 register.

On the GB60 series, this clock monitor cannot be turned on or off by the user. The on/off status of the clock monitor is determined by the state of the ICG module.

On the GB60A series, an option has been added to allow the user to disable the clock monitor. A new control bit, LOCD, has been added to the ICGC1 register at bit position 1, formerly an unimplemented bit. The reset state is ‘0’, which enables the clock monitor. Setting LOCD = 1 will disable the clock monitor and thereby eliminate any loss-of-clock resets or interrupts.

The advantage of disabling the clock monitor is to reduce the current draw of the ICG module. Disabling the clock monitor when running in stop3 mode with a low-range external oscillator enabled will save approximately 9 µA of current. With LOCD=0 in this configuration, the stop3 I_{DD} is about 14 µA. When LOCD=1 in this configuration, the stop I_{DD} is about 5 µA.

For the best combination of power conservation and system protection, Freescale Semiconductor recommends setting the LOCD=0 whenever the MCU is in active run mode and then setting LOCD=1 just before entering stop3 mode when OSCSTEN=1. If OSCSTEN=0, then the LOCD bit will not make a difference in the stop3 current.

System Device Identification Register

The system device identification register (SDIR) is a 16-bit value that contains a 12-bit part identification number and a 4-bit mask revision number. Both the GB60 series and the GB60A series have the same part identification number, $002.

The mask revision number for the last production version of the GB60 series is $4. The first mask revision number for the GB60A series is $8.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

EB652
Rev. 0.01, 08/01/2005

freescale™
semiconductor