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Programming the Channel Control Registers on the Time Processor Unit

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Introduction

The time processor unit (TPU) has several control registers that are shared by all 16 channels. Some of these registers, such as the channel interrupt enable register and channel interrupt status register, are not always used.

However, four registers must always be initialized:

- Channel function select registers
- Host sequence registers
- Host service request registers
- Channel priority registers

General Information

Channel Function Select Registers

The channel function select registers (CFSR1–CFSR3) contain the function numbers assigned to each individual channel. Each register holds the function numbers for four of the channels. These function numbers determine the TPU function assigned to each channel. They are mask set dependent because they are determined by the microcode assembly.

Host Sequence Registers

The host sequence registers (HSQR0 and HSQR1) contain the host sequence bits for the function running on a particular channel. Each host sequence register contains the host sequence bits for eight channels. The host sequence bits determine the mode of a particular function. For example, a function counting input transitions may operate in a single-shot mode or a continuous mode. Or, a function generating a square wave may or may not request other channels to synchronize to it.

The host sequence bits are different for each function because they are determined by the microcode for each function. The author of the microcode for a particular function determines what different combinations of the host sequence bits will mean for that function.

Host Service Request Registers

The host service request registers (HSRR0 and HSRR1) contain the service request bits for each channel. Each service register contains the service request bits for eight channels. The service request bits ask the TPU microengine to service a particular channel. Usually, the first service request is for initialization. Another common service request is for that of an immediate update.

Like the host sequence bits, the host service bits are different for each function because they are determined by the microcode for each function.

However, the host service bits are different from other control bits because, while the CPU can set the service bits, only the TPU can clear

them. In fact, clearing the bits to 0 is how the TPU tells the CPU that it has serviced the channel.

The host service request register should not be written unless:

1. All of the other parameters and control bits are already initialized or the channel is currently disabled via the channel priority register, and
2. The current state of the host service request register is 0. The program must wait until a previous service request has been cleared to 0 before issuing a new service request.

If the TPU is running two or more channels that share a host service request register and that are not going to be given simultaneous service requests, the most prudent way to enable them for initialization is to first disable all channels via the channel priority registers and then write to the service request registers.

Finally, enable each channel as needed via the channel priority registers. This method ensures that conflicts do not occur within the host service request registers.

Channel Priority Registers

The channel priority registers determine how often each channel is serviced.

The three priority levels are:

- High
- Medium
- Low

If the priority bits are set to 0, then a channel has no priority and is disabled. The TPU microengine will not service the channel at all unless it has a non-0 priority level. The priority scheme is discussed further in the TPU reference manual.

Summary

In summary, there are three possible situations for which a host service request may be issued:

1. Initializing a channel out of reset — Disable the channel via the channel priority register, initialize the parameter RAM and other control registers, and give the host service request for initialization. The final step is to enable the channel via the channel priority register.
2. Changing the function operating on a particular channel — Follow the same steps as for initialization out of reset.
3. Giving a channel a host service request other than that for initialization — Do not disable the channel. Instead, wait for the TPU to clear the previous host service request. Then, issue a new request. Usually, this would be for an immediate update or to force an output state on a particular pin.

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