

Motorola Semiconductor Engineering Bulletin

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Which Pins on the MC68331/332 and MC68HC16Z1 Need Pullup Resistors

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General Information

These pins should use a 10-k Ω resistor to five volts:


- BR/CS0 — To prevent unexpected bus request
- BERR — The bus error signal (BERR) is asserted in the absence of DSACK to indicate a bus error condition. The pullup resistor prevents unexpected assertion of bus error.
- HALT — To prevent erroneous bus halt
- IRQ[1:7] — To prevent erroneous interrupt requests
- DSACK0, DSACK1 — During normal bus transfer, external devices assert the data and size acknowledge signals DSACK1 and DSACK0 to indicate port width to the MC68HC16. The pullups prevent accidental assertion of DSACK[0:1] during reset.
- AVEC — The autovector signal AVEC can be used to terminate external interrupt acknowledge cycles. Assertion of AVEC causes the MC68HC16 to generate vector numbers to locate an interrupt handler routine. The pullup prevents unexpected assertion of the AVEC pin.
- TSTME/TSC — The test mode is entered if the signal line TSTME is held low and if the enter test mode bit in one of the special test registers is written. The pullup prevents the M68HC16 from



enabling test mode. However, test mode could be entered only if the software became corrupted and accidentally wrote the special test register. Consult your user's manual for what to do with this pin if you have anything other than a 68331, 68332, or 68HC16Z1.

NOTE: *This pin behaves differently for other MCUs.*

- R/W — To prevent accidental writes to memory during reset
- MODCLK — If using the internal PLL to generate the system clock, this pin must be pulled up or driven high during reset. If using an external clock source and bypassing the PLL, connect this pin to ground or drive it low during reset. PCLK, PAI should be pulled up with 10 k on MCUs with a GPT.
- RESET — The reset pullup resistor should be 820. If RESET does not rise within 10 system clocks, the MCU will re-drive reset and it will get stuck in this state.
- BKPT/DSCLK — Put a 4.7-k pullup resistor on this pin. Background debug mode operation is enabled when BKPT is asserted at the rising edge of the RESET signal. BDM remains enabled until the next system reset. If BKPT is at a logic level 1 on the trailing edge of RESET, BDM is disabled. BKPT is relatched on each rising transition of RESET. BKPT is synchronized internally, and must be asserted for at least two clock cycles prior to negation of RESET. A pullup resistor will ensure that the BDM is not unexpectedly enabled upon reset.

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