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Programming Priority Bits in the Interrupt Controller Current Priority Register for MPC56xx and MPC57xx Families

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1 Introduction

This engineering bulletin provides guidance on programming Priority(PRI) bits of the Interrupt Controller Current Priority Register(INTC_CPRn[PRI]) to ensure coherency of shared resource between Interrupt Services Routines(ISRs) for the MPC56xx and MPC57xx family of devices.

2 Programming

The PRI field in the INTC_CPRn register is elevated in the OSEK(Offene Systeme und deren Schnittstellen für die Elektronik in Kraftfahrzeugen) priority ceiling protocol to the top of all the priorities of the Interrupt Service Routines(ISRs) that share a common resource. This protocol therefore allows coherent accesses of the ISRs to that shared resource. For faster execution, below is the most-efficient procedure to modify the PRI bits in the INTC_CPRn register to prevent corruption of the shared data block.

OSEK uses the *GetResource* and *ReleaseResource* system services to manage access to a shared resource.

```
GetResource:
    wrteei 0              # disable external interrupts to the Processor
    raise PRI             # Write to CPR, cache inhibit, guarded
    mbar                  # flush out writes from store buffer
    wrteei 1              # enable external interrupts to the Processor
    isync                 # re-fetch Processor pipeline
ReleaseResource:
    Mbar                  # flush out writes from store buffer
    wrteei 0              # disable external interrupts to the Processor
    lower PRI             # Write to CPR, cache inhibit, guarded
    wrteei 1              # enable external interrupts to the Processor
```

However, MPC5676R, MPC567xK, MPC5775B/E and MPC5777C devices reference manuals mention method to add “delay of 5 core clock” before accessing the coherent data block. This method is also a valid method for these devices.

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