

NXP 5-bit multiplexed / 1-bit latched 6-bit I²C-bus EEPROM PCA9559

I²C-bus EEPROM DIP switch for easy system management

A simple way to implement open-drain buffer, jumperless configurations. The device provides four sets of potential outputs — logic high, logic lows, outputs that reflect the part's parallel inputs, or outputs configured by the I²C-bus.

Key features

- ▶ Supports 5-bit, 2-to-1 multiplexing
- ▶ One channel with flow-through inputs
- ▶ One channel with inputs configurable via the I²C-bus
- ▶ Supports one-bit, non-multiplexed latch for select pin control
- ▶ Open-drain outputs support voltages up to 3.6 V
- ▶ Two address pins enable up to four devices per bus
- ▶ Active-low override drives multiplexer outputs low
- ▶ Active-high write-protect disables EEPROM tampering
- ▶ Glitch-free operation on power-up and power-down
- ▶ 28-pin TSSOP (PW) package

Applications

- ▶ Configuration of processor frequency
- ▶ Configuration of voltage identification (VID)
- ▶ Dual-bios selection

The NXP PCA9559 is used to multiplex a default parallel input with an alternative set of inputs provided by the I²C-bus or SMBus. It is a derivative of the popular NXP PCA8550 device, with the addition of open-drain outputs for driving different voltage loads. It also adds two address pins to allow for up to four PCA9559 devices per bus.

Typical applications for the PCA9559 include processor frequency configuration, system clock generator frequency selection (FS), voltage identification (VID) configuration, and dual-BIOS selection.

The PCA9559 makes it possible to perform Intel processor frequency configuration using non-Intel chipsets such as those provided by ServerWorks and Via Technologies.

The PCA9559 also enables processor VID configuration and system clock generator FS by all chipsets. Processor VID indicates to the voltage regulator module (VRM) which voltage is required by the processor. Its five-bit value is usually provided by the processor, but, in special applications like

Mobile SpeedStep and Desktop Overclocking, can also be provided by the chipset.

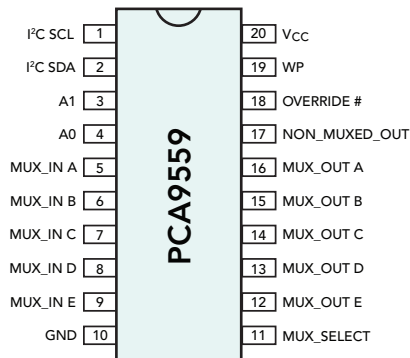
System clock generation FS indicates to the clock generator which frequency is required to accommodate a change in VID. For example, in Desktop Overclocking, the chipset provides a VID value greater than that provided by the processor. This increases processor voltage to increase the speed of the processor and maximize performance. However, a consistent ratio of processor to system bus frequency must be maintained, so the system clock frequency must also be increased.

Mobile SpeedStep does not require a change in system clock frequency, since it uses a proprietary ASIC to handle clocking differences.

The parallel inputs of the PCA9559 can be left unconnected so that the outputs either pass the default values of chipset-written values. If logic-low levels are required, an override pin is available to default the outputs to zeroes. This is especially useful in dual-BIOS selection for systems with multiple configurations.

Application Note AN250 provides more uses of the PCA9559 and PCA8550 devices.

For more information please visit www.nxp.com/i2c.



PCA9559 pin configuration



www.nxp.com



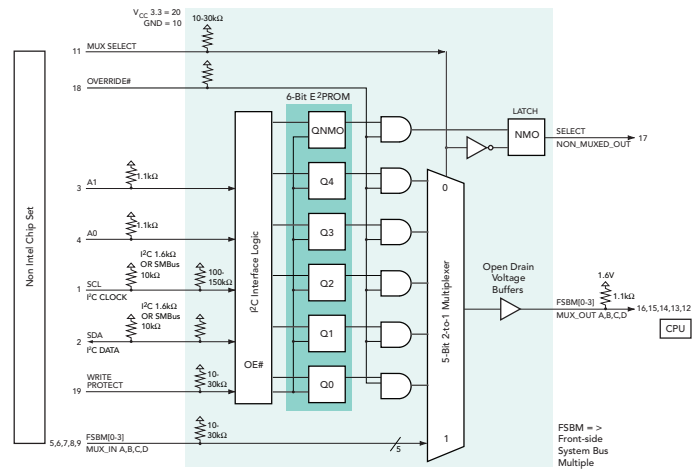
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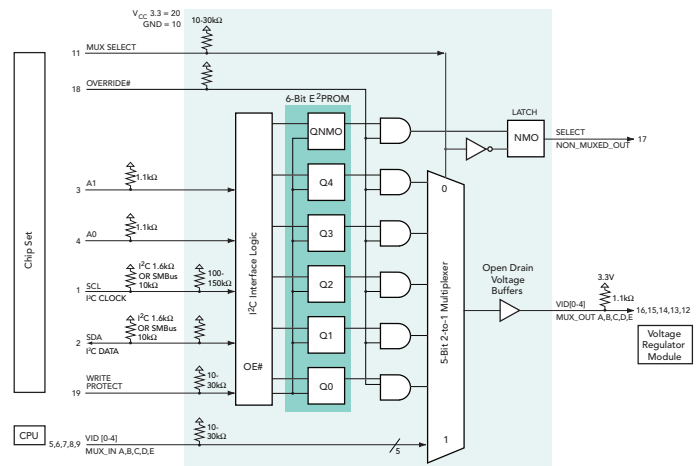
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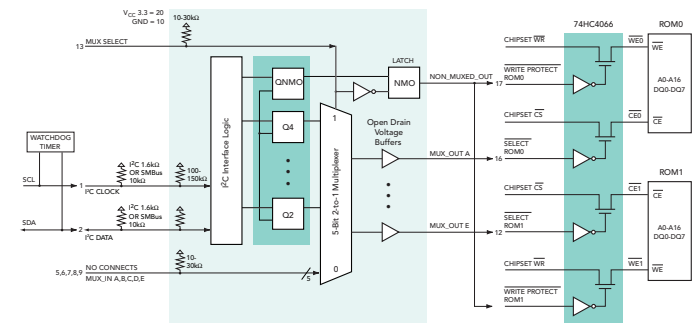
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The PCA9559 used for processor frequency configuration



The PCA9559 used for voltage identification (VID) configuration



The PCA9559 used for dual-BIOS selection with multiple system configurations