Using the CodeTEST Probe with Freescale™ MPC565/566 Processors

This document describes the requirements for connecting the CodeTEST Probe to the external bus of MPC56x processors.

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and the external bus of an MPC56x processor and to configure the Probe with the CodeTEST Manager.

Hardware Connections

The CodeTEST Probe supports targets with 100 MHz bus clocks with no wait states and 100-133 MHz clocks with one wait state.

The Probe supports 16- and 32-bit port sizes. You will need to identify data and address tag ports to be used for data transfers to the Probe.

Non-dedicated or no chip select

Use this connection method if there is not a chip select dedicated for use with the CodeTEST Probe. The chip select that controls the Probe port region can be connected to the extended bus to further qualify the bus cycles.

The following connections are required:

Probe	Processor	Notes
D31:0	D0:D31	Note the bit-wise inversion of the bus.
A31:24	NC	Address bits not available externally.
A23:0	A8:A31	Note the bit-wise inversion of the bus.
X15:0	NC	
X7:0	CS7:0*	Connect as needed to further qualify bus cycles.
C0	VCC or NC	VCC – not required
C1	CLKOUT	CLK
C2	TA*	DS

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C3	TS*	AS
C4	HRESET*	RST2
C5	SRESET*	RST1
C6	NC	CYC
C7	RD/WR*	WS

Dedicated CodeTEST chip select

Use this connection method when a chip select is dedicated for use with the CodeTEST Probe. The chip select used for the Probe port must be configured so that it meets the requirements of the Probe AS signal.

The following connections are required:

Probe	Processor	Notes
D31:0	D0:D31	Note the bit-wise inversion of the bus.
A31:24	NC	Address bits not available externally.
A23:0	A8:A31	Note the bit-wise inversion of the bus.
X15:0	NC	
C0	VCC or NC	VCC – not required
C1	CLKOUT	CLK
C2	NC	
C3	CSx*	AS
C4	HRESET*	RST2
C5	SRESET*	RST1
C6	NC	CYC
C7	RD/WR*	WS

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

Non-dedicated or no chip select

Use the Universal Probe type and select the following settings:

Field	Setting	Notes
Port Address		Enter address of the Probe tag port.
Port Address Mask	0xFF000000	
Extended Bus	0x0000	
Extended Bus Mask	0xFFFF	See Note.

Bus Type	Non-multiplexed	
Port Size	16 bit or 32 bit	Set according to bus width.
Reset Configuration		Set according to available resets.
Strobe Configuration	1 Strobe + internal data strobe	Can use 2 Strobe mode if TA* is connected.
Address Strobe Polarity	Low	
Write Strobe Polarity	Low	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set according to frequency of clock being monitored.
Phase Shift		Adjust as necessary to obtain accurate data.
Invert Clock	No	
Router Image		Select appropriate routing image.

Note: The extended bus mask must be set to allow qualification of the cycle with the appropriate chip select if necessary. For example, if the Probe ports reside in a region of memory controlled by chip select ‘0’ (CS0*), then the mask must be set to 0xFFFE; if the ports reside in a region of memory controlled by chip select ‘1’ (CS1*), then the mask must be set to 0xFFFD, and so on.

Dedicated CodeTEST chip select

Use the Universal Probe type and select the following settings:

Field	Setting	Notes
Port Address		Enter address of the Probe tag port.
Port Address Mask	0xFFFFFFFF	
Extended Bus	0x0000	
Extended Bus Mask	0xFFFF	
Bus Type	Non-multiplexed	
Port Size	16 bit or 32 bit	Set according to bus width.
Reset Configuration		Set according to available resets.
Strobe Configuration	1 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Disabled	
Bus Arbitration Polarity	Disabled	
Endianess	Big	

Word Swap	No	
Frequency Range		Set according to frequency of clock being monitored.
Phase Shift		Adjust as necessary to obtain accurate data.
Invert Clock	No	
Router Image		Select appropriate routing image.

Limitations

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.