ANE416

MC68HC05B4 RADIO SYNTHESIZER

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The MC68HC05B4 is a general purpose single-chip microcomputer with 4K of ROM. It shares with the other members of the M6805 family of devices a powerful instruction set including versatile bit-manipulation instructions. It incorporates an SCI which is used in this application to control a six digit LCD-driver and a standby mode in which the clock is stopped. This mode has the dual benefits of saving power and, in this application, eliminating the problem of interference with the radio. When a key is pressed the microprocessor "wakes", performs the required function and then goes back into the standby mode. The synthesizer software is included in the mask programmed code in parts marked MC68HC05B4 DEMO. Alternatively it could be programmed into an MC68HC805B6.

Other members of the MC68HC05B family include the 68HC05B6 with 6K of ROM and 256 bytes of EEPROM and the 68HC805B6 which is similar to the 68HC05B6 but with the ROM replaced with EEPROM. The 68HC805B6 is thus suitable for prototyping and small volume production not justifying a mask ROM part.

Synthesis of the local oscillator (LO) in a superheterodyne radio provides many advantages over mechanical tuning. The main benefits are tuning accuracy, stability and the storing of often used frequencies. The accuracy and stability result from the fact that the oscillator is phase locked to a crystal oscillator. Prior to the availability of synthesizers, crystals were used to obtain this degree of accuracy but with the disadvantage that a separate crystal was required for each frequency. Using a PPL synthesizer similar performance can be achieved with an unlimited number of frequencies using only one crystal. The accurate drift-free tuning is particularly important for standby use when nobody is on hand to provide fine tuning.

A synthesizer can be added to almost any design of radio by replacing the tuning capacitor with a varicap diode as shown in figure 1. The voltage biasing this varicap is supplied by the synthesizer and can also be used to provide RF tuning. A simpler solution is to leave the existing tuning control, at least initially, as an RF "preselector." This means that tracking, which can be a problem with multi-band designs, need not be considered.

SYNTHESIZER

The Motorola MC145157 CMOS synthesizer is one of a series offering a variety of options including serial or parallel interfacing and single or dual modulus prescaling. In this synthesizer only single modulus prescaling is used. Serial interfacing was chosen to minimize the number of interconnections required to control the MC145157 from the MC68HC05B4.

Figure 2 shows a block diagram of the MC145157. The counters are both 14 bits long and are loaded from shift registers which are loaded from the microprocessor

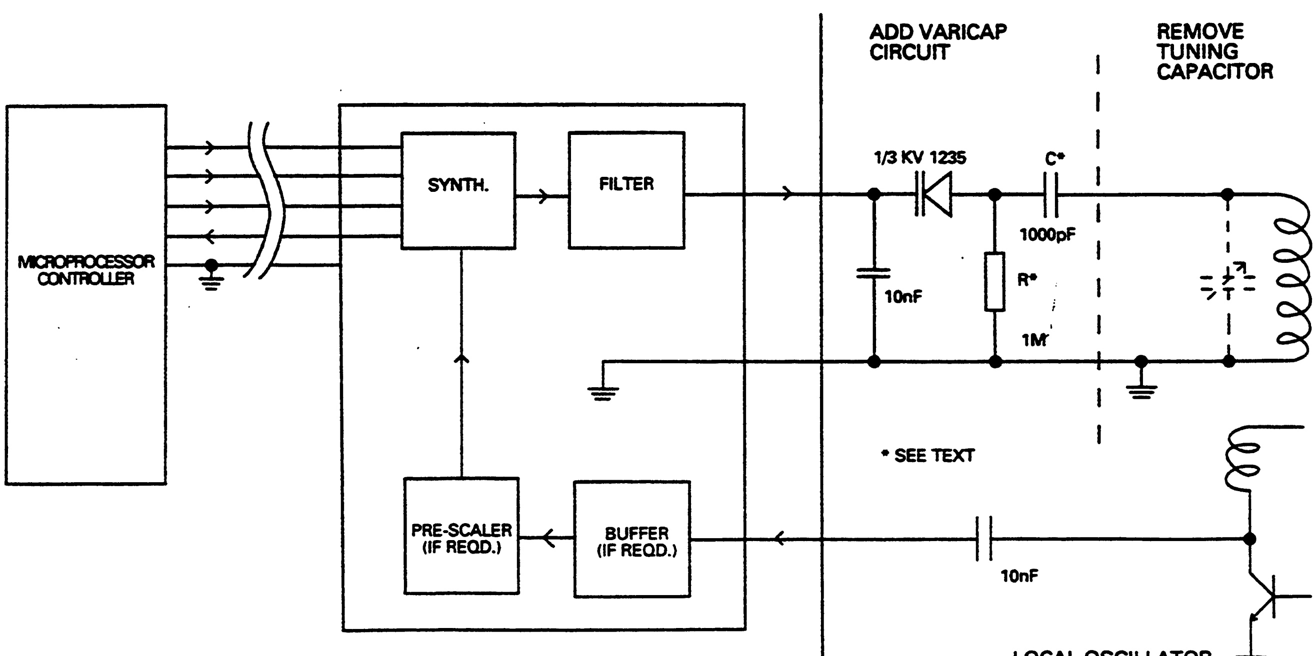

Figure 1. Synthesizer block diagram

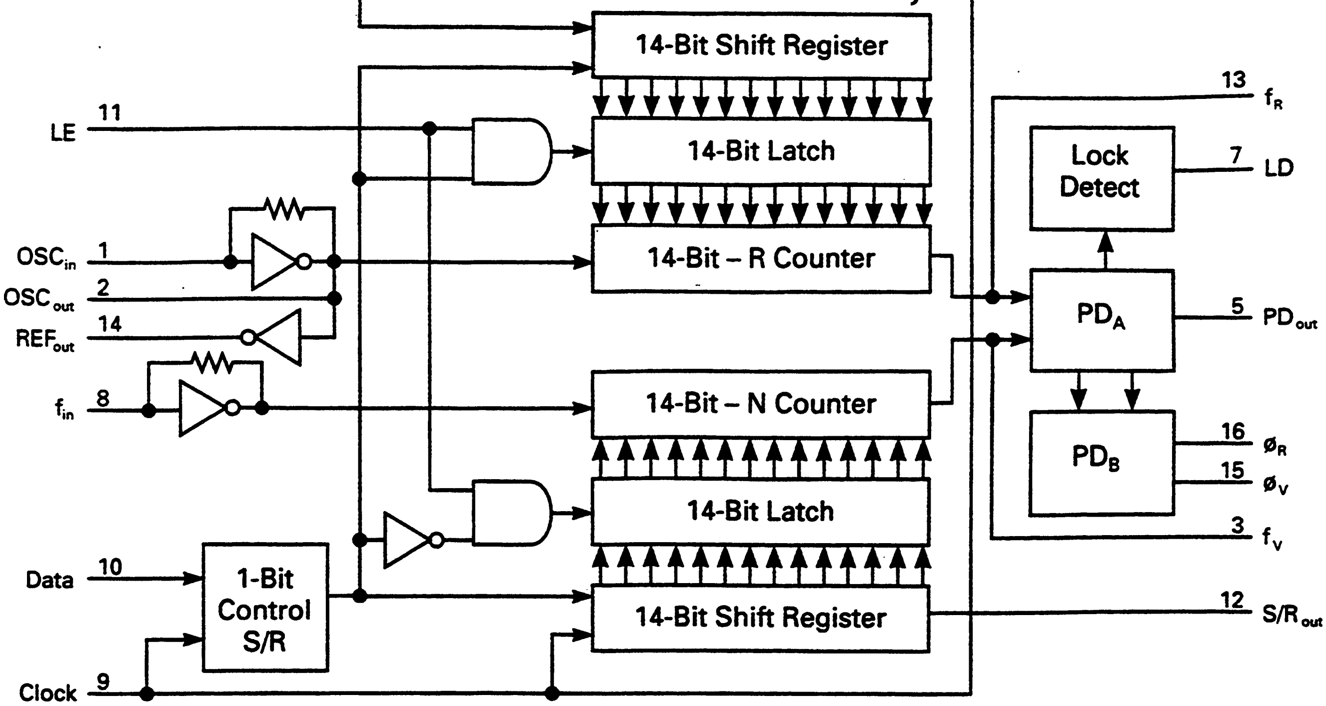

Figure 2. MC145157 block diagram

starting with the MSB. After loading the 14 data bits a 15th control bit is loaded and the information is transferred to the selected latch using LE (latch enable). If the control bit is a one then the reference divider latch is loaded, if it is zero the variable divider latch is loaded.

The reference counter divides the crystal oscillator down to the reference frequency (in this case 1kHz) at which the comparison is made with the (also divided down) local oscillator and the filtered output of the phase comparator supplies the tuning voltage to the local oscillator. The numbers chosen as the divide ratios determine the frequency at which this oscillator stabilises. The equation below shows the relationship between the various frequencies where P is the LO prescaler. The received frequency can be changed by altering the LO divide ratio. The microprocessor takes care of the decimal to binary conversion, IF offset and the other required arithmetic.

$$\text{LO freq.} = \text{RF} + \text{IF} = \text{P} \times \frac{\text{Xtal freq.}}{\text{ref. div. ratio}} \times \text{LO div. ratio}$$

REFERENCE FREQUENCY

The synthesizer's 10 MHz crystal oscillator is divided down by 10,000 to obtain the reference frequency at which the phase comparator operates. By choosing a high reference the filter design is made simpler. The disadvantage is that the minimum step size of the synthesizer is determined by this reference frequency. A reference of 1 kHz is a reasonable compromise for a broadcast receiver.

The MC145157 is specified to operate up to 20 MHz so pre-scaling is required on FM and SW (10.7 MHz IF). For this SW band divide by 5 pre-scaling is used and for FM divide by 10 is used. This increases the minimum step size to 10 kHz of FM which is ideal for this band and to 5 kHz on SW which is suitable for most broadcast stations but too large for some short wave applications. This can, however, be alleviated by the use of an RIT (receiver incremental tuning) control. The low IF SW options do not use prescaling and thus have a step of 1 kHz but a maximum frequency of just under 16 MHz (2 to the power 14 – IF).

The RIT adjustment is made by slightly changing the reference frequency. This is accomplished by replacing the usual trimming capacitors on the crystal pins of the MC145157 with varicap diodes. Adjustment is thus by a DC voltage allowing the control to be placed remote from the synthesizer. This type of adjustment necessarily gives a control range which is dependant on the tuned frequency but a high IF ensures that this is not too significant. The circuit shown gives the required range of +/–2.5kHz at the bottom of the SW band (1.6 MHz) and just over twice this range at 15 MHz.

If an RIT control is not required, pins 1 & 2 should have a 47pF capacitor and a 30pF trimmer respectively. The trimmer should be adjsuted to provide a reference frequency of 1kHz. This adjustment can be made with a frequency meter or simply by tuning into a strong broadcast of known frequency and adjusting for optimum reception or symmetric off-channel response.

FILTER

An important part of any phase locked loop is the loop filter. The filter shown in figure 3 is an active filter using the double ended phase detector output from the MC145157 feeding a 741 operational amplifier. An active filter has the advantage of increasing the available voltage swing beyond the supply rail of the MC145157.

The combination of active filter and double ended phase detector outputs makes it simple to select the correct relationship between voltage and frequency. Usually the fixed side of the varicap diode is earthed so increased

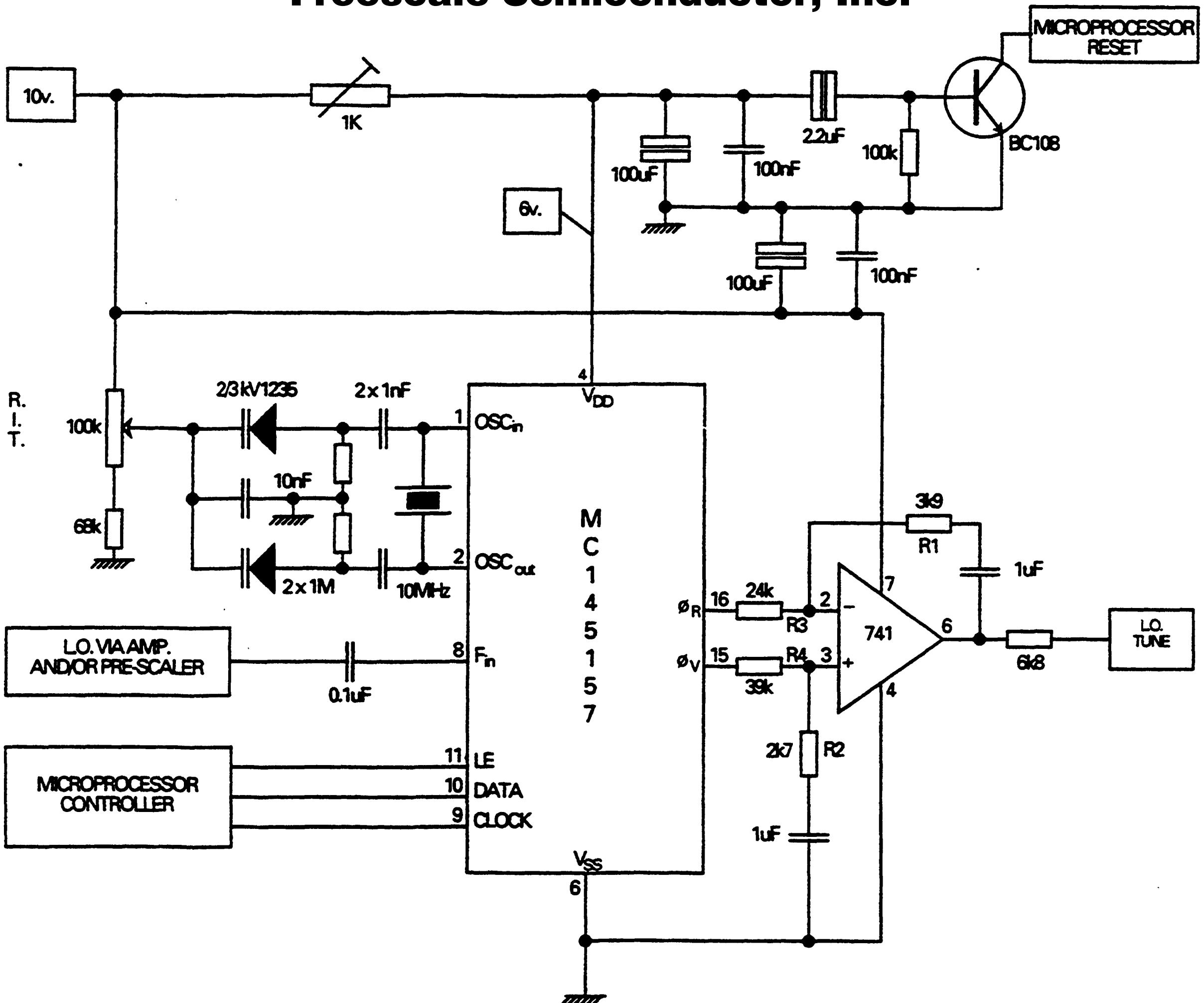

Figure 3. Synthesizer module

voltage increases the frequency of the oscillator but in some oscillator designs, where the varicap is already installed, the fixed side may be taken to the supply rail and increasing the voltage will decrease the frequency. With the filter design shown the choice can be made simply by switching the connections to pins 15 and 16 on the MC145157.

Resistors R1 through R4 may need to be adjsuted empirically to stabilize the loop and eliminate any trace of the reference frequency from the output of the radio.

DISPLAY

The software controls a 6-digit LCD display (Hamlin type 4200) via an MC145000 display driver. This display indicates the current frequency and memory number and assists with the entry of new frequencies. The MC145000 is fed serially with 48 bits corresponding to 6 digits of 8 segments (including the decimal point). It formats this data into the four backplane and 12 front-plane waveforms required to drive the LCD. This type of display (figure 4) has the advantage of using only one 24-pin driver employing only 16 connections between the display and the driver.

More readily available static displays require about 45 connections and thus normally uses more than one driver IC. The MC144115 driver is based on a shift register and can thus be configured to be compatible in software with the MC145000. The only difference is that it requires an LE (latch enable) signal, but this function can be derived from the clock using the circuit shown in figure 5. The static display also has the advantages of improved contrast and reduced current consumption. The consumption reduces from about 70μa (using an MC145000) to about 40μa (using 3 MC144115s). The 5v supply can be used directly with the static display, there being no need for a contrast adjustment. If the rightmost digit on the display does not have a decimal point this output from the display driver should be connected to an un-used segment, eg. a colon or the decimal point of the next digit. Any un-used segments, eg. colons, should be connected to the backplane.

There are advantages in also incorporating a frequency display module (eg. FC177), as it will show frequency changes due to the use of an RIT control and may also prove useful during fault-finding.

If a frequency display module is used the microprocessor controlled display can be omitted, the main disadvantage being that entered numbers in the direct frequency mode are not seen until the radio has moved to the new frequency.

PRINCIPLE OF OPERATION

The keyboard has 16 keys which perform the following functions:

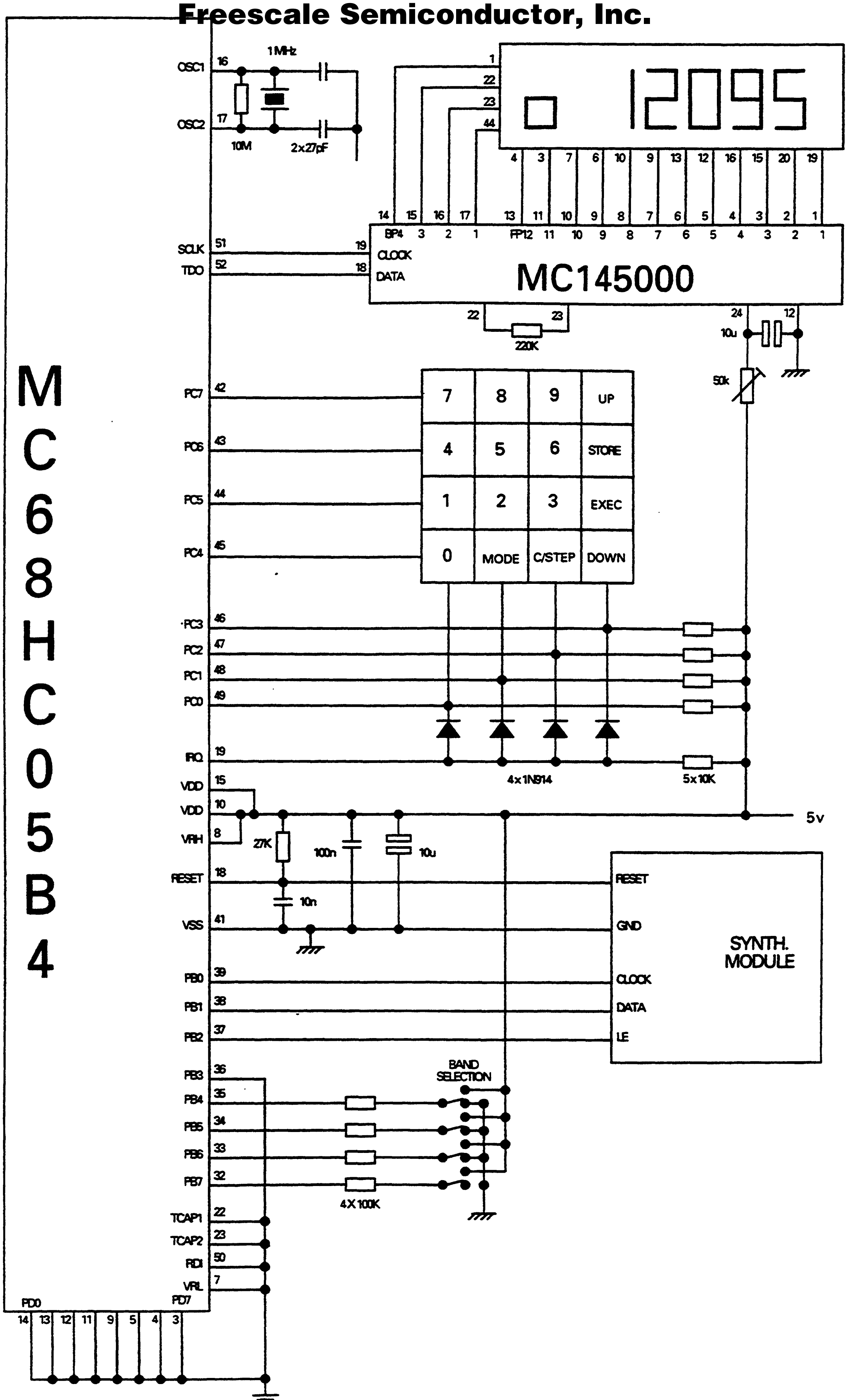

Figure 4. Microprocessor controller

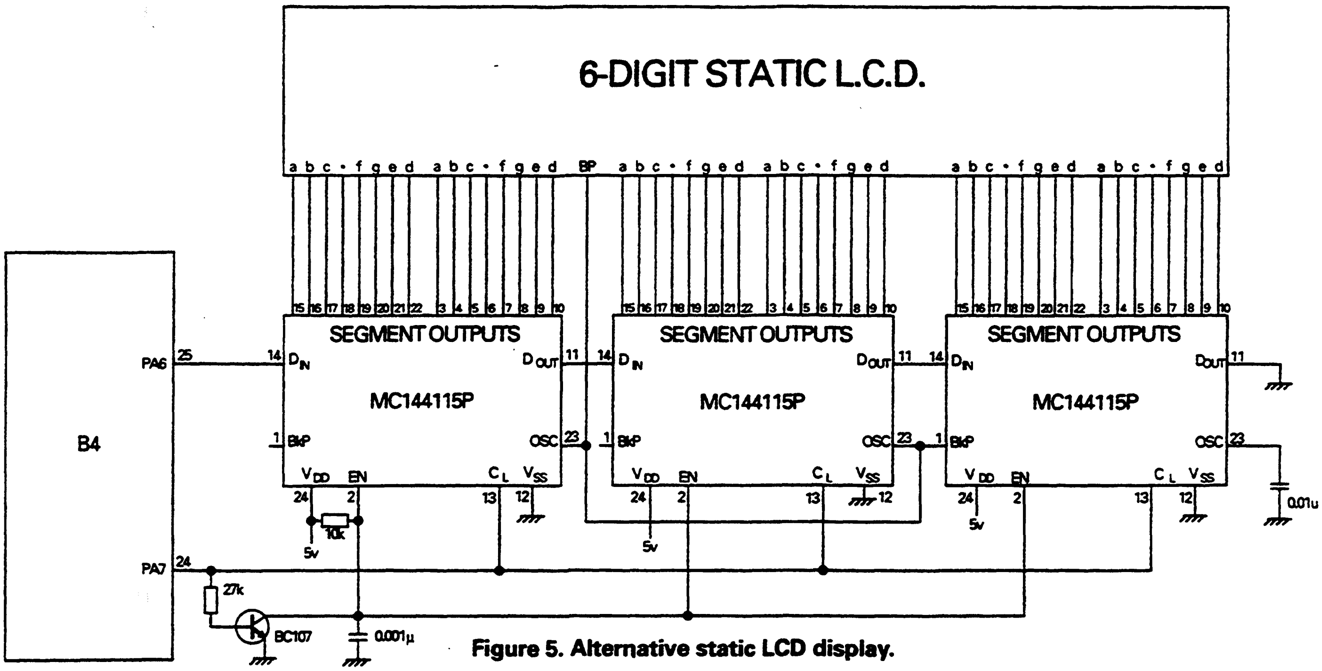

Figure 5. Alternative static LCD display.

0-9	These keys are used both for direct frequency entry and for recalling (or storing) the ten frequencies available on each band (thirty in total)
UP	Increment by one channel (5kHz SW, 9kHz MW, 50kHz FM) or 1kHz (10kHz on FM, not applicable to 10.7MHz SW)
DOWN	Decrement by one channel (5kHz SW, 9kHz MW, 50kHz FM) or 1kHz (10kHz on FM, not applicable to 10.7MHz SW)
STORE	Next key (0-9) stores current frequency at that key, (indicated by a decimal point on the left-most digit)
CLEAR	Clear display (frequency mode). Also toggles between channel steps and 1kHz steps in station mode (indicated by the right-most decimal point)
MODE	Change between frequency and station mode
EXECUTE	Go to frequency, but stay in current mode.

The leftmost digit in the display indicates which mode is current. In the direct frequency mode it is blank, in the station mode it shows the last station stored or recalled or if the current frequency has not been written into or recalled from memory it displays:- "o". A choice of 2 modes permits the minimum number of keystrokes regardless of method of use. In the station mode previously memorised stations can be recalled by pressing only the required button, there is no RECALL button. Storing a frequency requires two presses namely STORE (indicated by a decimal point on the left-most digit) and the memory number.

If direct frequency entry is required first press MODE to enter frequency mode, then enter the required frequency. There is now a choice, press MODE again to jump to the new frequency and return to station mode. Alternatively press EXECUTE to jump to the selected frequency but stay in frequency mode, new frequencies can then be selected with only the EXECUTE button required after each new frequency entered. The store facility also works in the frequency mode.

If it is required to change back from frequency mode to station mode without retuning the radio press STORE then MODE and to display current frequency press EXECUTE. In station mode EXECUTE updates the synthesizer and the display with the current frequency. This can be used when the radio is newly switched on to retune the frequency which was in use when it was switched off even if that

Band	PB7	6	5	4	IF offset	Step	Memory	Use	P-S
0	0	0	0	0	455 kHz	5, 1 kHz	1	SW	–
1	0	0	0	1	468 kHz	5, 1 kHz	1	SW	–
2	0	0	1	0	470 kHz	5, 1 kHz	1	SW	–
3	0	0	1	1	10,700 kHz	5 kHz	1	SW	5
4	0	1	0	0	–10,700 kHz	50,10 kHz	2	FM	10
5	0	1	0	1	0 kHz	50,10 kHz	2	FM	10
6	0	1	1	0	–70 kHz	50,10 kHz	2	FM	10
7	0	1	1	1	10,700 kHz	50,10 kHz	2	FM	10
8	1	0	0	0	455 kHz	9*,1 kHz	3	MW	–
9	1	0	0	1	468 kHz	9*,1 kHz	3	MW	–
10	1	0	1	0	470 kHz	9*,1 kHz	3	MW	–
11	1	0	1	1	10,700 kHz	5 kHz	3	SW	5

Note:- A high on PB3 changes the MW channel spacing to 10kHz for use in the USA.

...uency was not stored. Th... ...matically be designing the hardware to reset the microprocessor whenever the radio is switched on, thus allowing unattended recording etc. A method of achieving this is illustrated in figure 3. When the supply to the MC145157 is rising the BC108 switches on and momentarily pulls the microprocessor's reset low.

BANDS

Four of the MC68HC05B4's port B lines are used to provide band information to the CPU. These lines can be tied to the required level if only one band is required, this one band can constitute all the bands which use the same oscillator but select frequency range by switching coils. If however more than one oscillator has to be tuned or the step size has to be changed (eg. between MW and SW) the port lines can be switched using a separate switch or the same switch as that used for switching the other functions required within the radio (if spare contacts are available). Additionally the local oscillator feed to the MC145157 may need to be switched. The DC tuning voltage does not need to be switched as it can be fed in parallel to all varicaps. The following bands are available:

Bands 0, 1 & 2 are intended for single-conversion (low IF) SW radios and band 3, which assumes an external divide by 5, for dual-conversion (10.7MHz offset) designs. Bands 4-7 are intended for FM and assume an external divide by 10, IFs available are –10.7MHz (oscillator low) for front ends such as the LP1186, 10.7MHz (oscillator high) for ... (eg. Toko 5803/4 or 5402 or Larsholt 8319 or 7254) and –70kHz for the low IF TDA7000 FM radio IC.

A selection of 0, 1 & 1 in bits 6, 5 and 4 will select 10.7MHz IF short wave regardless of the state of line 7 so two banks of memory (1 & 3) giving a total of 20 stations can be used provided that the third bank is not being used for medium wave. A control to switch line 7 high is required to utilise this feature. This will also work for the low IF short wave options in which the raising of line 7 will select medium wave with the same IF offset. The only significant difference other than selecting the other bank is a switch to 9kHz steps (if large steps are selected) but this only applies while line 7 is being held high.

SYNTHESIZER CIRCUIT

The circuit is in two distinct parts. The circuit of the synthesizer is shown in figure 3, and that of the microprocessor controller in figure 4. The synthesizer board can be made very small and is the only part of the circuit which need actually go into (or close to) the radio. The local oscillator tuning capacitor is replaced with a varicap diode biased by the PLL via the filter (as shown in fig 1). If the LO coil provides a DC ground for the varicap and C is not required as a padder then C and R can be omitted from fig 1 .

The only other modification to the radio is the addition of an oscillator output to supply the MC145157. This should be taken from a low impedance point so that the oscillator

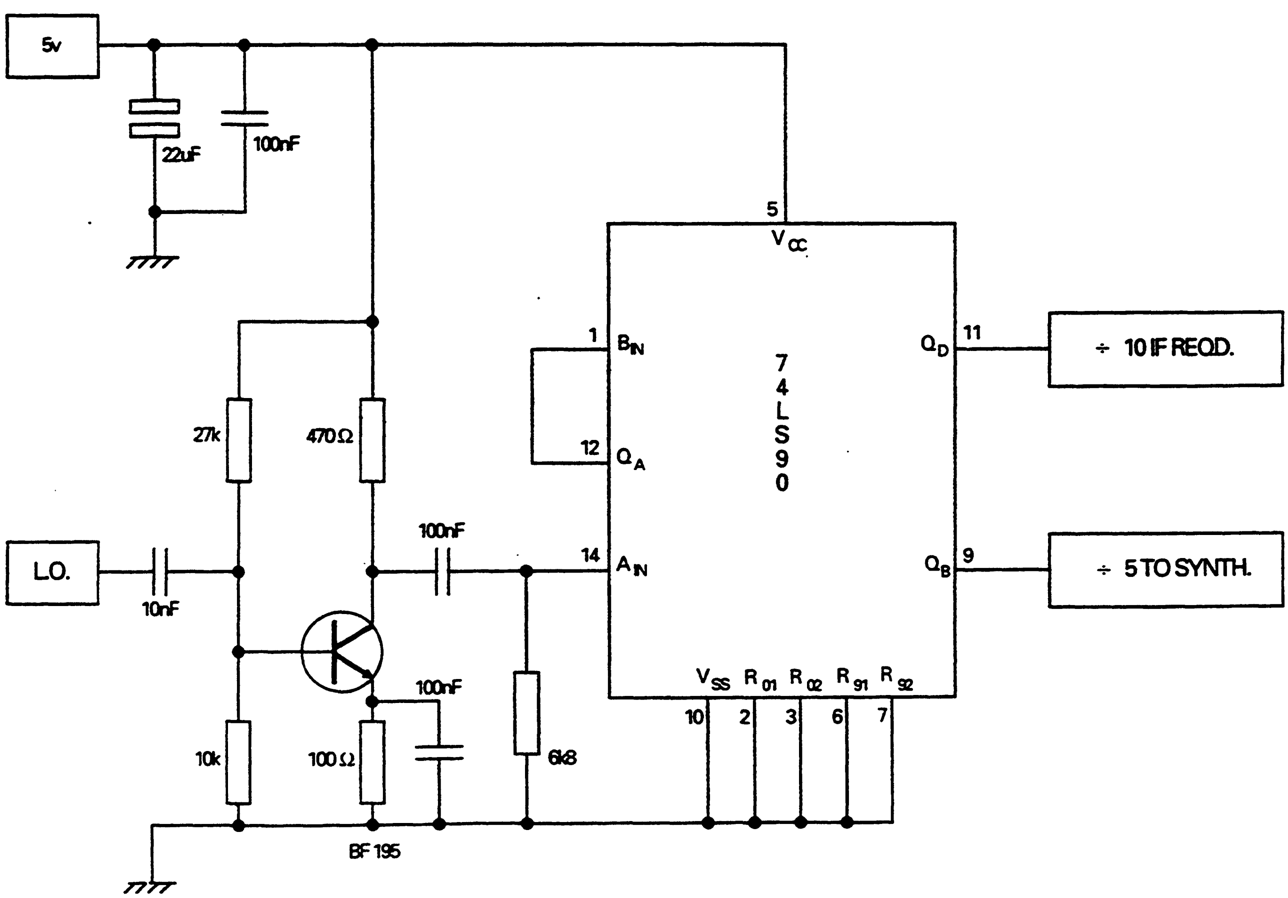

Figure 6. Band 3 (10.7MHz IF SW0 Amplifier and Pre-scaler

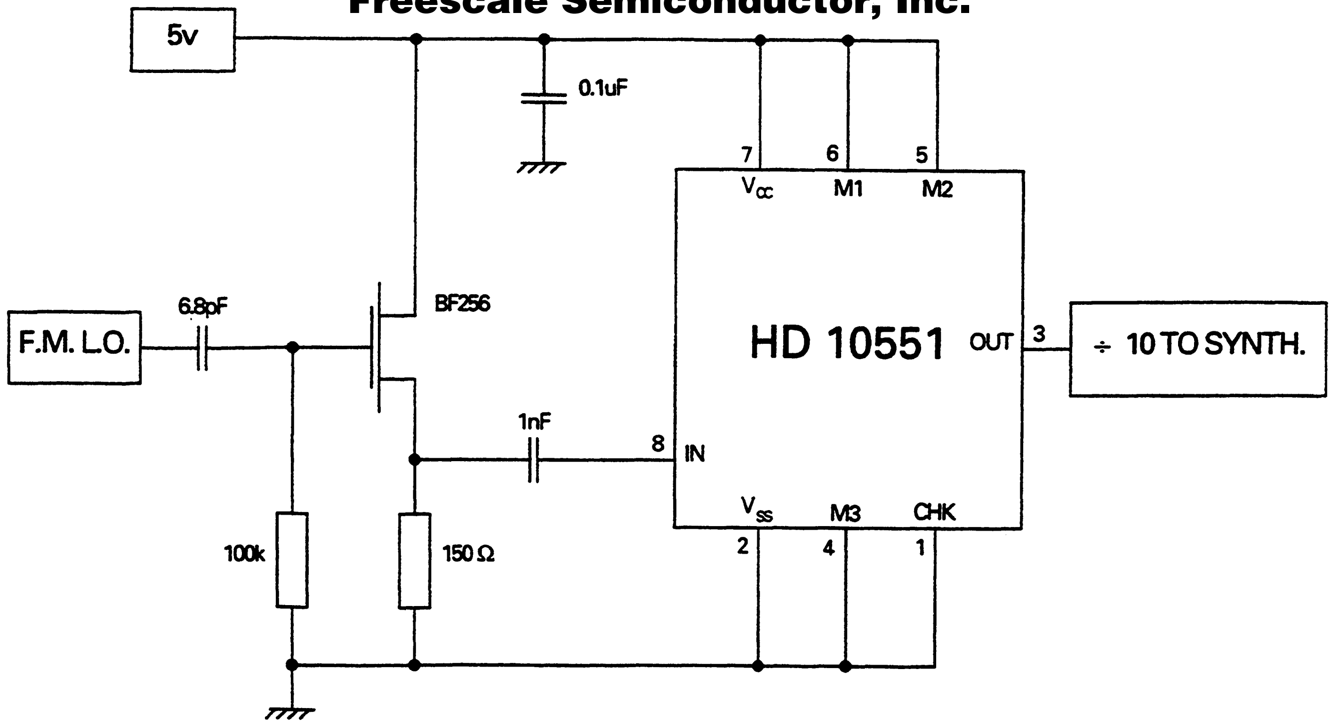

Figure 7. FM Buffer and Pre-scaler

is not significantly loaded. Pulling of the oscillator frequency is not a problem as the PLL circuitry will compensate but loading the tuned circuit itself is not recommended unless a high impedance buffer is included to prevent affecting the tuning range or the "Q" of the oscillator.

The local oscillator take-off may need to be buffered close to its source in order to further reduce circuit loading and to increase the signal to at least 500mV. Much of the debugging of the prototype was carried out using a simple LW/MW/SW radio based on the TDA1083 one-chip radio IC. This chip operated satisfactorily with pin 5 AC coupled directly to the MC145157 with no buffering.

For FM use a 100MHz divide by ten prescaler is required. Suitable devices include the SP8660 and the HD10551. The FC177 frequency display module requires divide by 100 for FM and 10 for short wave. This can be achieved in either case by using a divide by 10 as it can be cascaded with the 100MHz divider on FM. Both 74LS90s and 74HC160s were found suitable for this role. Figure 6 shows the circuit which was used with the 74LS90 to provide this divide by 10 and the divide by 5 pre-scaling required on band 3.

The supply voltage on the active filter determines the maximum voltage available to the varicap diodes. 10V is suitable for KV1235/6 diodes. The MC145157 will perform best at the required frequencies at a supply voltage slightly higher than the 5v used for the controller but should be chosen so that no special interfacing with the microprocessor is necessary. In practice anything between 5.5v and 6v is suitable. The 1k potentiometer in figure 3 should be adjusted to give this voltage, with the RIT control, if fitted, at its mid position.

For FM the LO output from most tuners can be AC coupled directly to the 100MHz pre-scaler. The standard LP1186 does not have an LO take-off but it can be taken, without other modification, from the emitter of the oscillator BF195 (near the center of the PCB).

Figure 7 shows a high-impedance amplifier suitable for use with the TDA7000 IC. This is necessary as the LO signal must be taken directly from the tuned circuit. This could be used with any other front end not equipped with an LO output.

MICROPROCESSOR CONTROLLER CIRCUIT

Bits 4-7 on port A are programmed as outputs which scan the keyboard when the microprocessor is interrupted via one of the diodes (see figure 4). When the row which caused the interrupt is identified one of bits 0-3, which are programmed as inputs, indicates which key has been pressed.

Bits 0, 1 and 2 on port B control the synthesizer and bits 4, 5, 6 and 7 input the band information to the microprocessor. Bit 3 on port B selects the channel step size for MW. When it is low the channel spacing is 9kHz as required in Europe, when it is high it selects 10kHz for the USA.

The SCI is used to send serial data to the MC145000 LCD driver. The SCI included in MC68HC05B4/6 devices has the clock required for this type of peripheral. As the MC145000 accepts data into a shift register a clock is required with every data bit. The SCI has a control bit which adds a clock for the last bit in each byte. This is described in more detail below. For comparison the software includes code to drive the MC145000 using port pins and the LCD can also be connected to I/O lines 6 & 7 on port A.

The MC145157 synthesizer is also controlled serially but requires a latch enable pulse to load the counters from the shift register. This cannot be supplied from the SCI which has only data and clock outputs. Port pins were consequently used to communicate with this chip.

The 5v supply to the controller should not be switched off if the station memories are to survive. The supply does not need to be regulated and a battery of 4 zinc-carbon or

Ɔad cells will do. The LCD display driver can be switched off if required to increase battery life. When the LCD is subsequently switched on it will display random data but will be written to when any key is pressed (use of the EXECUTE key restores the display to its previous data) or automatically if a reset circuit type shown in figure 3 is used.

SOFTWARE

An assembled listing of the section of code associated with the synthesizer, which is contained in the MC68HC05B4 DEMO, appears at the end of this application note. The MC68HC05B4 is a mask programmed chip and this code is only present in parts marked "DEMO". This B4 also includes a monitor and some test software. The pin numbers in fig 4 refer to the 52-pin FN part.

The first page of the listing contains no executable code but only hardware address definitions and the allocation of RAM. The B4 has 176 bytes of static RAM of which 108 are used in this application. 62 bytes are used for frequency storage, 2 bytes per frequency. There are 30 stored frequencies the additional one being the current frequency. 31 bytes are used for miscellaneous temporary storage and 15 bytes for the stack.

The second page of the listing contains the main program loop and the code which is executed after power-up or when an external reset occurs. On reset the program starts at address $137C. The ports and the SCI are initialised and the frequency stored in RAM locations SMEM & SMEM+1 is sent to the MC145157 and converted to decimal for displaying on the LCD. If the reset is the result of a power-up this frequency will be meaningless. The B4 then goes into the STOP mode in which the clock and all processing stops.

When a key is pressed the micro is wakened by the interrupt line, the clock is started and program execution commences at address $1354. The routine, KEYSCN, which determines which key has been pressed is executed and the function appropriate to that key is executed via the indexed jump at address $1375. After completion of this function the RTI instruction returns the program counter to the address following the STOP instruction from which the micro resumes a standby condition by executing the STOP instruction again.

The third page comprises KEYSCN and a table which associates the code of each key with an address. This is the start address of the subroutine required for that key. The routines for particular keys appear on the next four pages.

The PROG routine performs the calculations required to program the MC145157 with the correct divide ratio. Firstly the displayed frequency in BCD is added to the current IF offset. If band 3 is in use this result is divided by five to take the external prescaller into account. This is accomplished by first multiplying by two by adding the frequency to itself and then dividing it by ten by moving all digits down one place. The frequency is then converted to binary and sent to the synthesizer chip along with the reference divide ratio. In the case of band 3 this procedure discards the remainder when the divide by five is carried out. This is because the resolution on this band is 5kHz. If 5977kHz is requested the receiver will tune to 5975kHz. So that the user is aware of this having happened the actual binary frequency used is converted back to BCD and displayed on the LCD. Thus an entry of 5977 will change to 5975 when the receiver is tuned by pressing MODE or EXEC.

The MC145157 synthesizer chip is controlled by a 3-line serial bus. This is a common method of control as few pins are required and several chips can be controlled with only one enable line unique to each chip. The other two lines, clock and data can be common as the data is ignored if no enable is received. The SQRT routing sends data to the MC145157 using bits 0 & 1 on port B for the clock and data. It first sends the binary reference divide ratio (14 bits starting with the MSB) followed by a one for the control register (see fig 2). A one in the control register indicates that it is the reference divider which has to be loaded. This register is loaded by a latch enable signal from bit 2 on port B. The same procedure is repeated for the variable divide ratio except that this time the control bit is a zero.

The MC145000 LCD display driver is also serially controlled but has no enable pin. It can also be controlled by I/O lines and an example of how this can be done is shown on the last page of the listing. This routine is similar to that used for the MC145157. The B4, however, has a versatile serial port well suited to sending data to this type of peripheral. The second routine on the last page shows how this can be done using little more than half the bytes required for the I/O port method. The six bytes are sent by loading them in sequence into the SCI's data register. A wait loop monitoring the TDRE (transmit data register empty) flag is included so that each byte is written to this register only when the previous byte has been transferred to the transmit serial shift register. Once the last byte has been loaded a second wait loop monitoring the TC (transmit complete) flag ensures that transmission is complete before the program procedes as a return to the STOP mode terminates all processing including that of the SCI. Serial transmission often does not require a clock on the last bit of each byte but this is required for shift-register type peripherals like the MC145000. This is ensured by setting the LBCL (last bit clock) control bit in the SCR1 register. This is done by sending $01 to SCR1 after a reset. The reset code also sets up the baud rate and enables SCI transmission. If the alternative static display is used then port A should be used to drive it as the timing used on the SCI is not appropriate for the MC144115 display drivers.

The remainder of the code consists of subroutines for IF selection, BCD to binary and binary to BCD conversion, and addition and subtraction of BCD numbers.

DEBUG

On reset the left hand digit should display "o" and the other 5 digits should display random numbers. Pressing MODE should blank all but the rightmost digit which should display a zero. The LCD contrast should be adjusted using the 50k potentiometer in figure 4. With the LCD on, the standby current should be about 70μA and with it off, less than 1μA.

The only problems usually experienced with the synthesizer are instability of the LO frequency and audible reference frequency on the output of the radio. Either of these problems should be resolved by empirically adjusting R1 through R4. R1 & R2 should normally be in the range 1k to 10k, and R3 & R4 in the range 10k to 50k. Accurate values cannot be predicted as they depend on factors which vary between oscillators. The most significant of these factors is the tuning rate expressed in MHz per volt. The values shown in figure 3 were used with a dual conversion shortwave receiver with a tuning rate of about 1MHz/v.

An effective method of faultfinding a PLL circuit is to initially do the tuning with a potentiometer, leaving the output of the filter disconnected from the VCO. As the radio is tuned through the frequency set up in the synthesizer the filter output should switch from one extreme to the other. Until this test passes it is not useful to close the loop as it is very hard to distinguish the cause of a problem from its effects.

If, after adjusting R1 through R4, the reference frequency can still be heard, the tuning rate may need to be reduced by using a smaller valued C (figure 1) and adding a fixed capacitor across the oscillator coil. This will increase the Q of the oscillator and reduce the phase noise. If the tuning range becomes too small it can be restored by switching oscillator coils.

```
                    ***********************************************
                    *                                             *
                    *   This program enables the  MC68HC05B4 to   *
                    *   synthesize  the  local oscillator  of a   *
                    *   superhet  radio  with  MW/LW, SW and FM   *
                    *   bands each with a choice of IF offsets.   *
                    *   It utilises an MC145157 synthesizer and   *
                    *   an MC145000 LCD driver with a six-digit   *
                    *   four backplane display.                   *
                    *                                             *
                    *   P. Topping                    23-11-87    *
                    *                                             *
                    ***********************************************

                            OPT     noc

0000                PORTA   EQU     $00     PORT A ADDRESS
0001                PORTB   EQU     $01       "  B    "
0002                PORTC   EQU     $02       "  C    "
0004                PORTAD  EQU     $04     PORT A DATA DIRECTION REG.
0005                PORTBD  EQU     $05       "  B    "     "     "
0006                PORTCD  EQU     $06       "  C    "     "     "
000D                BAUD    EQU     $0D     SCI BAUD RATE REGISTER
000E                SCR1    EQU     $0E      "  CONTROL REG. No. 1
000F                SCR2    EQU     $0F      "     "     "     " 2
0010                SCSR    EQU     $10      "   STATUS   "
0011                SDAT    EQU     $11      "   DATA     "

0050                        ORG     $0050

0050                Q       RMB     6       DISPLAYED NUMBER
0056                P       RMB     6       WORKING NUMBER 1
005C                R       RMB     6       WORKING NUMBER 2

0062                W1      RMB     1       W
0063                W2      RMB     1       O
0064                W3      RMB     1       R
0065                W4      RMB     1       K
0066                W5      RMB     1       I
0067                W6      RMB     1       N
0068                KEY     RMB     1       CODE OF PRESSED KEY
0069                CARRY   RMB     1       BCD CARRY
006A                COUNT   RMB     1       LOOP COUNTER
006B                NUM1    RMB     1       1ST No. POINTER (ADD & SUBTRACT)
006C                NUM2    RMB     1       2ND No. POINTER (ADD & SUBTRACT)
006D                LOGO    RMB     1       STATION MODE INDICATOR/NUMBER

006E                STAT    RMB     1       STATUS BYTE :-
                    *                       0: MODE 1: STATION, 0: FREQ
                    *                       1: STEP 1: 1KHZ, 0: CHANNEL
                    *                       2: CLRQ 1: CLEAR IF NO. KEYED
                    *                       3: STOR 1: STORE, 0: RECALL

006F                SMEM    RMB     62      CURRENT FREQ. + 30 MEMORIES
00AD                        RMB     68      UNUSED
00F1                STACK   RMB     14      15 BYTES USED (1 INTERRUPT (5)
00FF                SP      RMB     1       AND 5 NESTED SUBROUTINES (10))
```

```
                                    ************************************************
                                    *                                              *
                                    *       A hardware interrupt  occurs with every *
                                    *       keystroke  and  is  vectored  to  start *
                                    *       here.  The B4 is wakened from  STOP and *
                                    *       the appropriate function for the key is *
                                    *       performed.  After the  RTI  instruction *
                                    *       the micro returns to the STOP mode.     *
                                    *                                              *
                                    ************************************************

1354                                        ORG     $1354

1354 2E 01                          STIRQ   BIL     REAL      INTERRUPT REAL ?
1356 80                                     RTI               NO, ABORT
1357 CD 13 A9                       REAL    JSR     KEYSCN    KEY PRESSED ?
135A 24 1F                                  BCC     AB        NO, ABORT
135C 5F                                     CLRX
135D B7 68                                  STA     KEY       CODE OF PRESSED KEY
135F A6 27                                  LDA     #$27      STATION MODE
1361 B7 6D                                  STA     LOGO      INDICATOR
1363 D6 13 CD                       RJ      LDA     CTAB,X    FETCH KEYCODE
1366 B1 68                                  CMP     KEY       WAS IT THIS ONE ?
1368 27 0A                                  BEQ     PJ        YES
136A A1 77                                  CMP     #$77      NO, LAST CHANCE ?
136C 27 0D                                  BEQ     AB        YES, ABORT
136E 5C                                     INCX              NO
136F 5C                                     INCX              TRY
1370 5C                                     INCX              THE
1371 5C                                     INCX              NEXT
1372 20 EF                                  BRA     RJ        ONE
1374 5C                             PJ      INCX
1375 DD 13 CD                               JSR     CTAB,X
1378 CD 16 75                               JSR     DQ        DISPLAY Q
137B 80                             AB      RTI

                                    ************************************************
                                    *                                              *
                                    *       Reset routine initialises ports and SCI *
                                    *       and puts the micro into STOP mode.      *
                                    *                                              *
                                    ************************************************

137C A6 FF                          START   LDA     #$FF      DISPLAY
137E B7 04                                  STA     PORTAD    OUTPUTS
1380 A6 07                                  LDA     #$07      BITS 0-2 OUTPUTS - SYNTH
1382 B7 05                                  STA     PORTBD    BITS 3-7 INPUTS  - BANDS
1384 A6 F0                                  LDA     #$F0      KEYBOARD
1386 B7 06                                  STA     PORTCD    I/O
1388 3F 02                                  CLR     PORTC
138A 3F 01                                  CLR     PORTB
138C 3F 00                                  CLR     PORTA
138E 3F 0D                                  CLR     BAUD      MAXIMUM BAUD RATE
1390 A6 01                                  LDA     #$01
1392 B7 0E                                  STA     SCR1      CLOCK ON ALL 8 BITS
1394 A6 08                                  LDA     #$08
1396 B7 0F                                  STA     SCR2      SET TRANSMIT ENABLE
1398 3F 6E                                  CLR     STAT
139A A6 27                                  LDA     #$27      STATION MODE
139C B7 6D                                  STA     LOGO      INDICATOR
139E CD 14 C2                               JSR     NEW       PROGRAM 145157
13A1 10 6E                                  BSET    0,STAT    STATION MODE
13A3 CD 16 75                               JSR     DQ        DISPLAY Q
13A6 8E                             STP     STOP              STANDBY
13A7 20 FD                                  BRA     STP
```

```
                                     ***********************************************
                                     *                                             *
                                     *      The  keyboard routine  returns the code *
                                     *      of the pressed key in the accumulator. *
                                     *      CTAB points to the required subroutine. *
                                     *                                             *
                                     ***********************************************

13A9 A6 F7                           KEYSCN LDA    #$F7      SET UP FOR FIRST COLUMN
13AB 48                              KEY1   LSLA             TRY EACH COLUMN
13AC 24 12                                  BCC    KEY2      COLUMN NOT FOUND
13AE B7 02                                  STA    PORTC     SET UP COLUMN
13B0 2F F9                                  BIH    KEY1      NOT THIS ONE
13B2 98                                     CLC
13B3 B6 02                           COLUMN LDA    PORTC     READ KEYBOARD
13B5 AD 0C                                  BSR    DBOUNC    WAIT
13B7 2F 07                                  BIH    KEY2      STILL PRESSED ?
13B9 2E FE                           RELSE  BIL    RELSE     WAIT FOR RELEASE
13BB AD 06                                  BSR    DBOUNC    WAIT
13BD 2E FA                                  BIL    RELSE     STILL RELEASED ?
13BF 99                                     SEC              SET FLAG
13C0 3F 02                           KEY2   CLR    PORTC     PREPARE LINES FOR IRQ
13C2 81                                     RTS

13C3 AE FF                           DBOUNC LDX    #$FF      PAUSE
13C5 21 FE                           DLOOP  BRN    *         256X12
13C7 21 FE                                  BRN    *         CYCLES
13C9 5A                                     DECX
13CA 26 F9                                  BNE    DLOOP
13CC 81                                     RTS

13CD EE                              CTAB   FCB    $EE       0  CODE OF KEY
13CE CC 14 0D                               JMP    DIGIT        SUBROUTINE
13D1 DE                                     FCB    $DE       1
13D2 CC 14 0D                               JMP    DIGIT
13D5 DD                                     FCB    $DD       2
13D6 CC 14 0D                               JMP    DIGIT
13D9 DB                                     FCB    $DB       3
13DA CC 14 0D                               JMP    DIGIT
13DD BE                                     FCB    $BE       4
13DE CC 14 0D                               JMP    DIGIT
13E1 BD                                     FCB    $BD       5
13E2 CC 14 0D                               JMP    DIGIT
13E5 BB                                     FCB    $BB       6
13E6 CC 14 0D                               JMP    DIGIT
13E9 7E                                     FCB    $7E       7
13EA CC 14 0D                               JMP    DIGIT
13ED 7D                                     FCB    $7D       8
13EE CC 14 0D                               JMP    DIGIT
13F1 7B                                     FCB    $7B       9
13F2 CC 14 0D                               JMP    DIGIT
13F5 ED                                     FCB    $ED       F MODE
13F6 CC 14 FA                               JMP    MOD
13F9 D7                                     FCB    $D7       E PROGRAM
13FA CC 14 9C                               JMP    PROG
13FD E7                                     FCB    $E7       D DOWN
13FE CC 14 6C                               JMP    DOWN
1401 EB                                     FCB    $EB       C CLEAR ENTRY/STEP SIZE
1402 CC 15 0B                               JMP    CLEAR
1405 B7                                     FCB    $B7       B STORE
1406 16 6E                                  BSET   3,STAT
1408 81                                     RTS
1409 77                                     FCB    $77       A UP
140A CC 14 5F                               JMP    UP
```

```
***********************************************************
*                                                         *
*      Number entry routine.                              *
*      If in station mode  a frequency is read            *
*      or written (if the store flag is set).             *
*      In frequency mode the entered number is            *
*      placed in the  least significant  digit            *
*      and existing digits are moved up.                  *
*                                                         *
***********************************************************

140D 9F             DIGIT  TXA
140E 44                    LSRA
140F 44                    LSRA
1410 00 6E 1E              BRSET  0,STAT,SKP STATION MODE ?
1413 06 6E 1B              BRSET  3,STAT,SKP STORING ?
1416 B7 64                 STA    W3
1418 05 6E 05              BRCLR  2,STAT,SHIFT CLEAR Q ?
141B 15 6E                 BCLR   2,STAT    YES, CLEAR FLAG
141D CD 16 55              JSR    CLQ       AND CLEAR Q
1420 CD 16 6C       SHIFT  JSR    DR1       W1: MSD, W2: LSD
1423 BE 62                 LDX    W1
1425 E6 01          AGS    LDA    1,X       MOVE ALL DIGITS
1427 F7                    STA    0,X       UP ONE PLACE
1428 5C                    INCX
1429 B3 63                 CPX    W2
142B 26 F8                 BNE    AGS       DONE ?
142D B6 64                 LDA    W3        YES, RECOVER NEW DIGIT
142F F7                    STA    0,X       AND PUT IT IN LSD
1430 81                    RTS

1431 97             SKP    TAX              X < MEMORY No.
1432 D6 16 62              LDA    STABL,X   REPLACE LOGO WITH
1435 B7 6D                 STA    LOGO      MEMORY NUMBER
1437 9F                    TXA
1438 4C                    INCA             ADD 1 TO SKIP CURRENT FREQ.
1439 0F 01 04              BRCLR  7,PORTB,MW6
143C AB 14                 ADD    #20       THIRD BANK OF 10
143E 20 05                 BRA    MW4       STATIONS
1440 0D 01 02       MW6    BRCLR  6,PORTB,MW4
1443 AB 0A                 ADD    #10       SECOND BANK OF 10
1445 48             MW4    LSLA             2 BYTES PER MEMORY
1446 97                    TAX              BACK TO X
1447 07 6E 0B              BRCLR  3,STAT,RECALL

144A B6 6F          STORE  LDA    SMEM      WRITE CURRENT
144C E7 6F                 STA    SMEM,X    FREQUENCY INTO
144E B6 70                 LDA    SMEM+1    SELECTED STATION
1450 E7 70                 STA    SMEM+1,X  MEMORY
1452 17 6E                 BCLR   3,STAT    CLEAR FLAG
1454 81                    RTS

1455 E6 6F          RECALL LDA    SMEM,X    RECALL
1457 B7 6F                 STA    SMEM      SELECTED
1459 E6 70                 LDA    SMEM+1,X  STORED
145B B7 70                 STA    SMEM+1    STATION
145D 20 63                 BRA    NEW
```

```
**************************************************
*                                                *
*       Increment and decrement routine.         *
*       Step size is 1kHz if the step flag is 1  *
*       but 9kHz for MW and 5kHz for SW if 0.    *
*       FM steps are 10kHz and 50kHz.            *
*       Band 3 is always 5kHz.                   *
*       If PB3 is high MW channel step is 10kHz  *
*       for use in the US of A.                  *
*                                                *
**************************************************

145F AD 1A          UP     BSR    LDXR
1461 3C 6F          IF     INC    SMEM      INCREMENT LSB
1463 26 02                 BNE    T1        DID IT WRAP ROUND
1465 3C 70                 INC    SMEM+1    YES, INCREMENT MSB
1467 5A             T1     DECX
1468 26 F7                 BNE    IF        ALL DONE ?
146A 20 56                 BRA    NEW

146C AD 0D          DOWN   BSR    LDXR
146E 3D 6F          DF     TST    SMEM      IS LSB ZERO
1470 26 02                 BNE    T2        IF NOT LEAVE MSD
1472 3A 70                 DEC    SMEM+1    DECREMENT MSB
1474 3A 6F          T2     DEC    SMEM      DECREMENT LSB
1476 5A                    DECX
1477 26 F5                 BNE    DF        ALL DONE ?
1479 20 47                 BRA    NEW

147B AE 02          LDXR   LDX    #2        1 KHZ (FM: 10KHZ)
147D 02 6E 12              BRSET  1,STAT,SRT
1480 AD 11                 BSR    BAND
1482 A1 03                 CMP    #3
1484 27 0C                 BEQ    SRT
1486 AE 0A                 LDX    #10       5 KHZ (SW, FM: 50KHZ)
1488 0F 01 07              BRCLR  7,PORTB,SRT
148B AE 12                 LDX    #18       9 KHZ (MW)
148D 07 01 02              BRCLR  3,PORTB,SRT
1490 AE 14                 LDX    #20       10 KHZ (US MW)
1492 81             SRT    RTS

**************************************************
*                                                *
*       Read band from port B .                  *
*                                                *
**************************************************

1493 B6 01          BAND   LDA    PORTB     FIND BAND
1495 A4 70                 AND    #$70      USE BITS 4, 5 & 6
1497 44                    LSRA             MOVE
1498 44                    LSRA             DOWN
1499 44                    LSRA             INTO
149A 44                    LSRA             LS BITS
149B 81                    RTS
```

```
*************************************************
*                                               *
*       PROG is executed when  EXEC or MODE  is *
*       pressed.  The displayed number is added *
*       to the  IF offset,  converted to binary *
*       and stored in SMEM & SMEM+1.            *
*       NEW takes the binary  working frequency *
*       in  SMEM & SMEM+1  and  sends it to the *
*       synthesizer chip  using the  subroutine *
*       SQRT.  It also converts it to  BCD  for *
*       the display.                            *
*                                               *
*************************************************

149C 00 6E 23     PROG   BRSET  0,STAT,NEW STATION MODE ?
149F CD 15 49            JSR    IFO       P < IF OFFSET
14A2 AE 50               LDX    #Q
14A4 BF 6B               STX    NUM1
14A6 CD 15 EE            JSR    ADD       Q < FREQ + IF

14A9 AD E8               BSR    BAND
14AB A1 03               CMP    #3        BAND 3 ?
14AD 26 10               BNE    ONE       NO
14AF AE 50               LDX    #Q        YES, DIVIDE BY FIVE
14B1 BF 6C               STX    NUM2
14B3 CD 15 EE            JSR    ADD       Q < 2 X (FREQ + IF)
14B6 AE 05               LDX    #5
14B8 E6 4F        LPP    LDA    Q-1,X     MOVE ALL DIGITS
14BA E7 50               STA    Q,X       IN Q DOWN ONE
14BC 5A                  DECX             PLACE TO DEVIDE
14BD 26 F9               BNE    LPP       BY 10 (Q < Q/5)

14BF CD 15 9E     ONE    JSR    BCON      CONVERT Q TO BINARY

14C2 A6 21        NEW    LDA    #$21      1 KHZ ( 10MHZ/10,000 )
14C4 B7 5C               STA    R         "
14C6 A6 4E               LDA    #$4E      "
14C8 B7 5D               STA    R+1       "
14CA AD 53               BSR    SQRT      SEND NEW FREQUENCY
14CC CD 16 24            JSR    DCON      CONVERT TO BCD IN Q

14CF AD C2               BSR    BAND
14D1 A1 03               CMP    #3        BAND 3 ?
14D3 26 19               BNE    STIF      NO
14D5 AE 50               LDX    #Q        YES, MULTIPLY BY 5
14D7 BF 6B               STX    NUM1
14D9 BF 6C               STX    NUM2
14DB AE 56               LDX    #P
14DD CD 15 EE            JSR    ADD       P < 2Q
14E0 AE 56               LDX    #P
14E2 BF 6B               STX    NUM1
14E4 AE 50               LDX    #Q
14E6 CD 15 EE            JSR    ADD       Q < 3Q
14E9 AE 50               LDX    #Q
14EB CD 15 EE            JSR    ADD       Q < 5Q

14EE CD 15 49     STIF   JSR    IFO       P < IF OFFSET
14F1 AE 50               LDX    #Q
14F3 BF 6B               STX    NUM1
14F5 14 6E               BSET   2,STAT
14F7 CC 15 D5            JMP    SUB       Q < (RATIO X STEP) -IF
```

```
                   ***************************************************
                   *                                                 *
                   *      Mode change routine.                       *
                   *                                                 *
                   ***************************************************

14FA 06 6E 02      MOD     BRSET   3,STAT,SKIP STORE FLAG SET ?
14FD AD 9D                 BSR     PROG        NO, SEND DISPLAYED FREQUENCY
14FF 17 6E         SKIP    BCLR    3,STAT      CLEAR STORE FLAG
1501 01 6E 04              BRCLR   0,STAT,SK FREQUENCY MODE ?
1504 11 6E                 BCLR    0,STAT      NO, SET TO FREQUENCY MODE
1506 20 06                 BRA     CLAL        CLEAR
1508 10 6E         SK      BSET    0,STAT      YES, SET TO STATION MODE
150A 81                    RTS

150B 00 6E 05      CLEAR   BRSET   0,STAT,SM STATION MODE ?
150E CD 16 55      CLAL    JSR     CLQ         NO, CLEAR Q
1511 20 09                 BRA     CLP
1513 02 6E 04      SM      BRSET   1,STAT,KHZ
1516 12 6E                 BSET    1,STAT      KHZ STEPS
1518 20 02                 BRA     CLP
151A 13 6E         KHZ     BCLR    1,STAT      CHANNEL STEPS
151C 17 6E         CLP     BCLR    3,STAT      CLEAR STORE FLAG
151E 81                    RTS

                   ***************************************************
                   *                                                 *
                   *      Routine to send the reference and local    *
                   *      oscillator divide ratios to the 145157.    *
                   *                                                 *
                   ***************************************************

151F B6 5D         SQRT    LDA     R+1
1521 AD 11                 BSR     SQU         SEND REFERENCE MSB
1523 B6 5C                 LDA     R
1525 AD 06                 BSR     SQU2        AND LSB
1527 B6 70                 LDA     SMEM+1      LOCAL  OSC. MSB
1529 AD 09                 BSR     SQU
152B B6 6F                 LDA     SMEM        AND LSB
152D AD 05         SQU2    BSR     SQU
152F 14 01                 BSET    2,PORTB     LATCH
1531 15 01                 BCLR    2,PORTB     IT
1533 81                    RTS

1534 AE 08         SQU     LDX     #8
1536 3F 01                 CLR     PORTB       ALL ZEROS
1538 48            S1      LSLA                MOVE 1 BIT INTO "C"
1539 24 02                 BCC     S2          ZERO ?
153B 12 01                 BSET    1,PORTB     NO
153D 10 01         S2      BSET    0,PORTB     CLOCK
153F 11 01                 BCLR    0,PORTB     IT
1541 13 01                 BCLR    1,PORTB
1543 5A                    DECX
1544 26 F2                 BNE     S1          ANY MORE ?
1546 17 6E                 BCLR    3,STAT
1548 81                    RTS
```

```
                    ***********************************************
                    *                                             *
                    *      The IF offset is selected according to *
                    *      the required band and placed in "P".   *
                    *                                             *
                    ***********************************************

1549 CD 14 93       IFO    JSR    BAND       FIND BAND
154C 48                    LSLA              X2
154D B7 62                 STA    W1
154F 48                    LSLA              X4
1550 DB 62                 ADD    W1         TIMES 6 AND ADD 5
1552 AB 05                 ADD    #5         TO REACH LAST DIGIT
1554 B7 63                 STA    W2         OF SELECTED IF
1556 A6 06                 LDA    #6
1558 B7 6A                 STA    COUNT
155A BE 63          LP6    LDX    W2
155C D6 15 6E              LDA    IFS,X      TRANSFER
155F 3A 63                 DEC    W2         SELECTED
1561 BE 6A                 LDX    COUNT      INTERMEDIATE FREQUENCY
1563 E7 55                 STA    P-1,X      INTO P
1565 3A 6A                 DEC    COUNT
1567 26 F1                 BNE    LP6        DONE ?
1569 AE 56                 LDX    #P         SET-UP POINTER
156B BF 6C                 STX    NUM2
156D 81                    RTS

156E 00 00 00 04 05 05 IFS FCB    0,0,0,4,5,5    455 KHZ SW/MW
1574 00 00 00 04 06 08     FCB    0,0,0,4,6,8    468  "    "
157A 00 00 00 04 07 00     FCB    0,0,0,4,7,0    470  "    "
1580 00 01 00 07 00 00     FCB    0,1,0,7,0,0  10.70 MHZ SW (EXT/5)
1586 09 09 08 09 03 00     FCB    9,9,8,9,3,0 -10.70  "  FM (EXT/10)
158C 00 00 00 00 00 00     FCB    0,0,0,0,0,0      0  "   "    "
1592 09 09 09 09 09 03     FCB    9,9,9,9,9,3    -70 KHZ "    "
1598 00 00 01 00 07 00     FCB    0,0,1,0,7,0  10.70 MHZ "    "
```

```
                          ***************************************************
                          *                                                 *
                          *     BCD to binary conversion. No. in "Q" is     *
                          *     converted to binary in SMEM & SMEM+1.       *
                          *                                                 *
                          ***************************************************

159E 3F 6F                BCON   CLR    SMEM      CLEAR WORKING
15A0 3F 70                       CLR    SMEM+1    FREQUENCY LOCATIONS
15A2 5F                          CLRX
15A3 B6 6F                L2     LDA    SMEM      LS BYTE
15A5 48                          LSLA             2xLSB
15A6 B7 62                       STA    W1        SAVE 2xLSB
15A8 39 70                       ROL    SMEM+1    2xMS BYTE
15AA B6 70                       LDA    SMEM+1
15AC B7 63                       STA    W2        SAVE 2xMSB
15AE B6 62                       LDA    W1        2xLSB
15B0 48                          LSLA             4xLSB
15B1 39 70                       ROL    SMEM+1    4xMSB
15B3 48                          LSLA             8xLSB
15B4 39 70                       ROL    SMEM+1    8xMSB
15B6 BB 62                       ADD    W1        10xLSB
15B8 B7 6F                       STA    SMEM
15BA B6 70                       LDA    SMEM+1
15BC B9 63                       ADC    W2        10xMSB
15BE B7 70                       STA    SMEM+1
15C0 5C                          INCX             FETCH
15C1 E6 50                       LDA    Q,X       NEXT
15C3 BB 6F                       ADD    SMEM      DIGIT
15C5 B7 6F                       STA    SMEM      AND
15C7 4F                          CLRA             ADD IT TO
15C8 B9 70                       ADC    SMEM+1    WORKING
15CA B7 70                       STA    SMEM+1    FREQUENCY
15CC A3 05                       CPX    #5        DONE ?
15CE 26 D3                       BNE    L2
15D0 38 6F                       LSL    SMEM      MOVE UP ONE BIT TO
15D2 39 70                       ROL    SMEM+1    INCLUDE 145157 CONTROL BIT
15D4 81                          RTS
```

```
                    ************************************************************
                    *                                                          *
                    *      Addition and subtraction of BCD numbers             *
                    *                                                          *
                    ************************************************************

15D5 BF 66          SUB     STX     W5        ANSWER POINTER
15D7 BE 6C          COM2    LDX     NUM2      9S COMPLIMENT
15D9 A6 06          COMP    LDA     #$06      SECOND NUMBER
15DB B7 6A                  STA     COUNT
15DD A6 09          LOOP3   LDA     #$09
15DF E0 05                  SUB     5,X       SUBTRACT FROM 9
15E1 E7 05                  STA     5,X       AND PUT IT BACK
15E3 5A                     DECX
15E4 3A 6A                  DEC     COUNT
15E6 26 F5                  BNE     LOOP3
15E8 3F 69                  CLR     CARRY     SET CARRY TO ONE
15EA 3C 69                  INC     CARRY     BEFORE ADDING
15EC 20 04                  BRA     AD        ADD FIRST NUMBER

15EE 3F 69          ADD     CLR     CARRY
15F0 BF 66                  STX     W5        ANSWER POINTER
15F2 A6 06          AD      LDA     #$06
15F4 B7 6A                  STA     COUNT
15F6 BE 6B                  LDX     NUM1      1st No. POINTER
15F8 BF 64                  STX     W3
15FA BE 6C                  LDX     NUM2      2nd No. POINTER
15FC BF 65                  STX     W4
15FE BE 64          LOOP    LDX     W3
1600 E6 05                  LDA     5,X
1602 3A 64                  DEC     W3
1604 BE 65                  LDX     W4
1606 EB 05                  ADD     5,X       ADD
1608 3A 65                  DEC     W4
160A BB 69                  ADD     CARRY     SET ON ADDITION OVERFLOW
160C 3F 69                  CLR     CARRY     OR POS. RESULT SUBTRACTION
160E AD 0F                  BSR     ADJ       DECIMAL ADJUST
1610 BE 66                  LDX     W5
1612 E7 05                  STA     5,X       SAVE ANSWER
1614 3A 66                  DEC     W5
1616 3A 6A                  DEC     COUNT
1618 26 E4                  BNE     LOOP      DONE ?
161A 81                     RTS

161B A0 0A          AJ      SUB     #10       YES, SUBRTACT 10
161D 3C 69                  INC     CARRY     AND REMEMBER CARRY
161F A1 0A          ADJ     CMP     #10
1621 24 F8                  BHS     AJ        10 OR MORE?
1623 81                     RTS               NO
```

```
                          ************************************************
                          *                                              *
                          *    Current  binary divide ratio in  SMEM &   *
                          *    SMEM+1 is converted to decimal in Q.      *
                          *                                              *
                          ************************************************

1624 B6 70                DCON   LDA    SMEM+1    TRANSFER CURRENT
1626 B7 63                       STA    W2        FREQUENCY DEVIDE
1628 B6 6F                       LDA    SMEM      RATIO INTO
162A B7 62                       STA    W1        WORKING AREA
162C AE 5C                       LDX    #R        CLEAR
162E BF 6B                       STX    NUM1
1630 AD 25                       BSR    CLRAS     R
1632 3C 61                       INC    R+5       R < 1
1634 AD 1F                       BSR    CLQ       CLEAR Q
1636 A6 0E                       LDA    #14       14 BITS TO CONVERT
1638 B7 67                       STA    W6
163A 34 63                       LSR    W2        MOVE OUT AND IGNORE
163C 36 62                       ROR    W1        145157 CONTROL BIT
163E 34 63                LOOP2  LSR    W2        MOVE OUT
1640 36 62                       ROR    W1        FIRST (LS) BIT
1642 24 06                       BCC    NXT       ZERO
1644 AE 50                       LDX    #Q        ONE, ADD
1646 BF 6C                       STX    NUM2      CURRENT VALUE
1648 AD A4                       BSR    ADD       OF R
164A AE 5C                NXT    LDX    #R        ADD R
164C BF 6C                       STX    NUM2      TO
164E AD 9E                       BSR    ADD       ITSELF
1650 3A 67                       DEC    W6        ALL
1652 26 EA                       BNE    LOOP2     DONE ?
1654 81                          RTS

                          ************************************************
                          *                                              *
                          *    Miscellaneous.                            *
                          *                                              *
                          ************************************************

1655 AE 50                CLQ    LDX    #Q        CLEAR Q
1657 A6 06                CLRAS  LDA    #06       CLEAR 6 Bytes
1659 B7 6A                       STA    COUNT     STARTING AT X
165B 7F                   CR     CLR    0,X
165C 5C                          INCX
165D 3A 6A                       DEC    COUNT
165F 26 FA                       BNE    CR        DONE ?
1661 81                          RTS

1662 EB                   STABL  FCB    $EB       0   SEGMENT
1663 60                          FCB    $60       1
1664 C7                          FCB    $C7       2   CODES
1665 E5                          FCB    $E5       3
1666 6C                          FCB    $6C       4   FOR THE
1667 AD                          FCB    $AD       5
1668 AF                          FCB    $AF       6   MC145000
1669 E0                          FCB    $E0       7
166A EF                          FCB    $EF       8   LCD DRIVER
166B ED                          FCB    $ED       9

166C A6 50                DR1    LDA    #Q        STORE POINTERS
166E B7 62                       STA    W1        (USED IN DIGIT AND DQ)
1670 AB 05                       ADD    #5
1672 B7 63                       STA    W2
1674 81                          RTS
```

```
*************************************************************
*                                                           *
*     First part of  display  subroutine  adds              *
*     the store and kHz flags and station mode              *
*     indicator,  replaces  BCD  with  segment              *
*     codes and blanks leading zeros.                       *
*                                                           *
*************************************************************

1675 AD F5        DQ     BSR    DR1
1677 AE 5C               LDX    #R        CLEAR R
1679 AD DC               BSR    CLRAS
167B BE 62               LDX    W1        FIND
167D 5A                  DECX             LEADING
167E 5C           RO     INCX             ZEROS
167F B3 63               CPX    W2
1681 27 03               BEQ    OUT       LAST ?
1683 F6                  LDA    0,X       NO
1684 27 F8               BEQ    RO        ZERO ?
1686 5A           OUT    DECX             EXIT LOOP
1687 BF 67               STX    W6        LEAST SIG. LEADING ZERO
1689 A6 05               LDA    #$05
168B B7 65               STA    W4
168D BE 63               LDX    W2        LSB
168F F6           D3     LDA    0,X
1690 BF 66               STX    W5
1692 97                  TAX
1693 D6 16 62            LDA    STABL,X   FIND 7 SEGMENT CODE
1696 BE 65               LDX    W4
1698 E7 5C               STA    R,X       PUT IN DISPLAY TABLE
169A 3A 65               DEC    W4
169C BE 66               LDX    W5
169E 5A                  DECX
169F B3 67               CPX    W6        FINISHED ?
16A1 26 EC               BNE    D3
16A3 0D 01 09            BRCLR  6,PORTB,NODPT SW ?
16A6 0E 01 06            BRSET  7,PORTB,NODPT MW ?
16A9 B6 5F               LDA    R+3
16AB AA 10               ORA    #$10      DECIMAL POINT FOR FM MHZ
16AD B7 5F               STA    R+3
16AF B6 5C        NODPT  LDA    R
16B1 01 6E 02            BRCLR  0,STAT,KS
16B4 B6 6D               LDA    LOGO      STATION MODE LOGO
16B6 07 6E 02     KS     BRCLR  3,STAT,PIKS
16B9 AA 10               ORA    #$10      STORE FLAG INDICATOR
16BB B7 5C        PIKS   STA    R
16BD CD 14 93            JSR    BAND
16C0 A1 03               CMP    #3        BAND 3 ?
16C2 27 09               BEQ    OUTT      YES, NO CHOICE
16C4 03 6E 06            BRCLR  1,STAT,OUTT NO, STEP SIZE ?
16C7 B6 61               LDA    R+5
16C9 AA 10               ORA    #$10      KHZ STEP INDICATOR
16CB B7 61               STA    R+5
```

```
                      ***************************************************
                      *                                                 *
                      *      The second part of the  display routine    *
                      *      sends  the  48  bits  required  by  the    *
                      *      display  driver.   For  comparison  two    *
                      *      routines are included, one using port A    *
                      *      lines and a second using the SCI.          *
                      *                                                 *
                      ***************************************************

16CD AE 05            OUTT   LDX    #5         SEND DISPLAY TABLE TO 145000
16CF E6 5C            DISCHR LDA    R,X
16D1 BF 64            DISPLY STX    W3         SAVE INDEX
16D3 1D 00                   BCLR   6,PORTA    CLEAR DATA
16D5 AE 08                   LDX    #8
16D7 44               DIS1   LSRA              SET UP
16D8 24 02                   BCC    DIS2       BIT OF
16DA 1C 00                   BSET   6,PORTA    ACCUMULATOR
16DC 1E 00            DIS2   BSET   7,PORTA    CLOCK
16DE 1F 00                   BCLR   7,PORTA    IT
16E0 1D 00                   BCLR   6,PORTA    CLEAR DATA
16E2 5A                      DECX              COMPLETE ?
16E3 26 F2                   BNE    DIS1       NO
16E5 BE 64                   LDX    W3         RESTORE INDEX
16E7 5A                      DECX
16E8 2A E5                   BPL    DISCHR

                      ***************************************************
                      *                                                 *
                      *      SCI LCD driver interface.                  *
                      *                                                 *
                      ***************************************************

16EA AE 05                   LDX    #5         INITIALISE X
16EC E6 5C            MORE   LDA    R,X        FETCH DIGIT
16EE 0F 10 FD                BRCLR  7,SCSR,*   WAIT UNTIL TDRE = 1
16F1 B7 11                   STA    SDAT       WRITE IT TO SCI TX REG.
16F3 5A                      DECX              NEXT DIGIT
16F4 2A F6                   BPL    MORE       DONE ?
16F6 0D 10 FD                BRCLR  6,SCSR,*   WAIT UNTIL TC=1
16F9 81                      RTS
                      *
```

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