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Application Note

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Migrating Applications from MC9S12VR64 to MC9S12VR32

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1. Introduction

This application note is intended to highlight the differences between MC9S12VR64 and MC9S12VR32 to facilitate the migration of already developed applications to the new platform MC9S12VR32. MC9S12VR32 is a feature reduced version of MC9S12VR64. It targets LIN applications that do not require as many communication modules, fewer analog inputs and memory as those available in MC9S12VR64. Thus, bringing the possibility to lower the cost of applications without renouncing the high performance offered by MC9S12VR64.

The MC9S12VR32 features the well-known HCS12 core, an integrated 5 V voltage regulator, on chip LIN physical layer, and it is compatible with MC9S12VR64 requiring little to no change at all in the application.

For specific information on the MC9S12VR family, please refer to the reference manual as well as any available errata, both can be found at nxp.com.

The MC9S12VR32 major differences are a reduction of both Flash and EEPROM memory, reduction of SCI and ADC channels, improvements in the CPMU and High-side driver module, and the lack of an SPI module. These differences are being highlighted in Table 1.

Table 1. **Key differences between S12VR64 and S12VR32**

Feature	MC9S12VR64	MC9S12VR32
Flash memory (ECC)	64 KB	32 KB
EEPROM (ECC)	512 Bytes	128 Bytes
SPI	1	-
SCI	2	1
10-bit ADC channels	Up to 6	2
High-side drivers	2	1
CPMU	S12CPMU_UHV	S12CPMU_UHV_V8
Package	32 LQFP 48 LQFP	32 LQFP 32 QFN

This document addresses improvements of certain MC9S12VR32 modules over those of MC9S12VR64 and some major changes that might have an impact in applications.

2. Pinout and pin assignment

The pinout remains almost the same with the exception of the alternative functions related with Serial Communication Interface 1 (SCI1) and Serial Peripheral Interface (SPI). This ensures full compatibility with MC9S12VR64 devices with a 32 Low-profile Quad Flat Package.

Figure 1 highlights the alternative functions unavailable in MC9S12VR32/16.

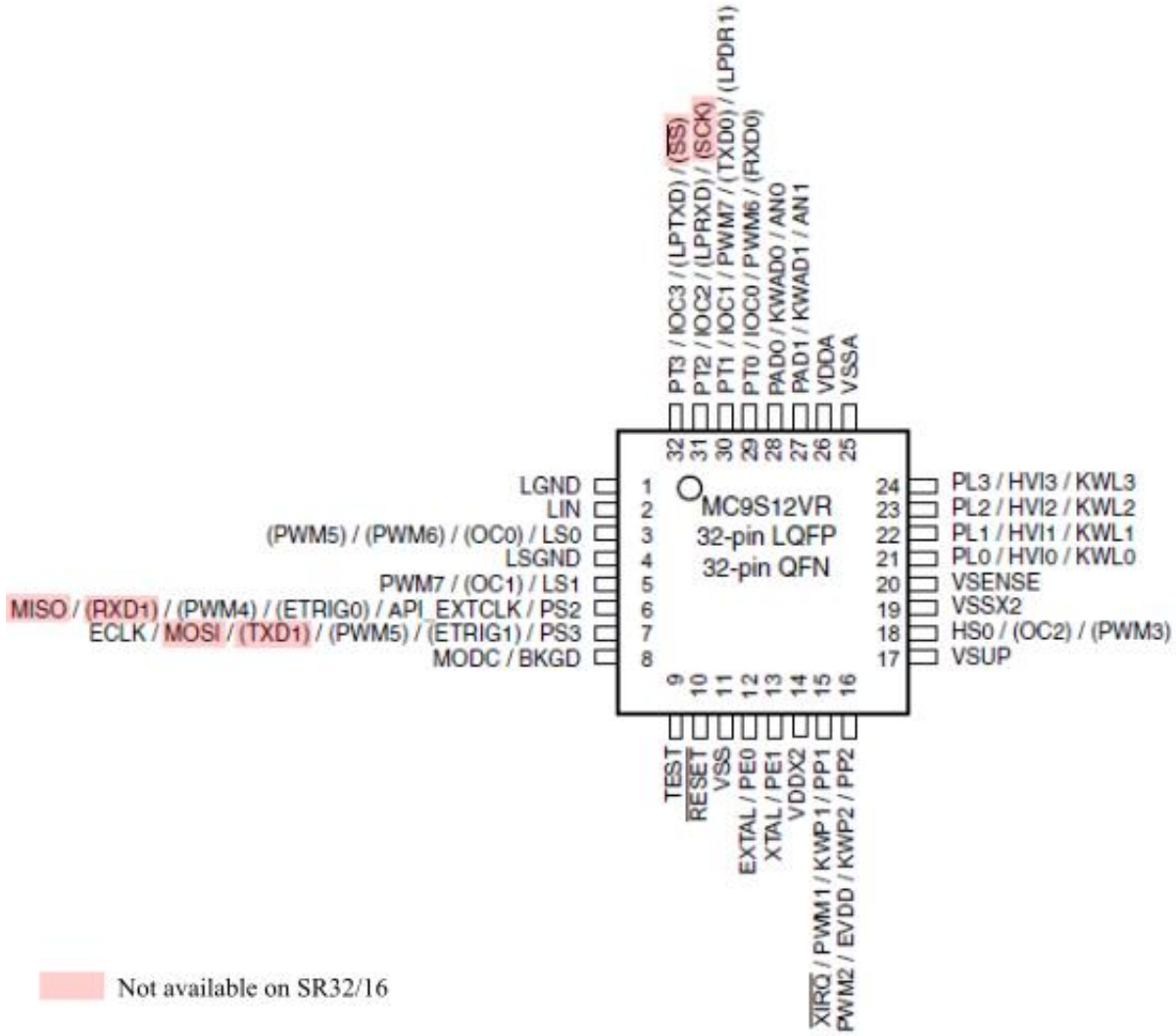

Figure 1. MC9S12VR 32-pin LQFP/QFN pinout

2.1. Port integration module

MC9S12VR32/16 is fully compatible with MC9S12VR64/48 32-pin package versions. The port integration module has been modified to take into account the lack of pins in relation to the 48-pin package.

If the application does not use any of the underlined registers in Figure 2 and Figure 3, then no software modifications are required.

Global Address	Register Name[1]		Bit 7	6	5	4	3	2	1	Bit 0
0x001E	**IRQCR**	R	**IRQE**	**IRQEN**	0	0	0	0	0	0
		W								
0x0246	MODRR0	R	**MODRR07**	**MODRR06**	MODRR05	MODRR04	MODRR03	MODRR02	MODRR01	MODRR00
		W								
0x0247	**MODRR1**	R	0	0	**MODRR15**	**MODRR14**	0	0	0	0
		W								
0x0248	PTS	R	0	0	**PTS5**	**PTS4**	PTS3	PTS2	**PTS1**	**PTS0**
		W								
0x0249	PTIS	R	0	0	**PTIS5**	**PTIS4**	PTIS3	PTIS2	**PTIS1**	**PTIS0**
		W								
0x024A	DDRS	R	0	0	**DDRS5**	**DDRS4**	DDRS3	DDRS2	**DDRS1**	**DDRS0**
		W								
0x024C	PERS	R	0	0	**PERS5**	**PERS4**	PERS3	PERS2	**PERS1**	**PERS0**
		W								
0x024D	PPSS	R	0	0	**PPSS5**	**PPSS4**	PPSS3	PPSS2	**PPSS1**	**PPSS0**
		W								
0x024E	WOMS	R	0	0	**WOMS5**	**WOMS4**	WOMS3	WOMS2	**WOMS1**	**WOMS0**
		W								
0x024F	MODRR2	R	MODRR27	0	**MODRR25**	**MODRR24**	**MODRR23**	MODRR22	MODRR21	**MODRR20**
		W								
0x0258	PTP	R	0	0	**PTP5**	**PTP4**	**PTP3**	PTP2	PTP1	**PTP0**
		W								
0x0259	PTIP	R	0	0	**PTIP5**	**PTIP4**	**PTIP3**	PTIP2	PTIP1	**PTIP0**
		W								

[1] Registers in **bold underlinded** are only available in S12VR64/48. On S12VR32/16 these locations read 0 and write is unimplemented.

Figure 2. Port module integration registers

Global Address	Register Name[1]		Bit 7	6	5	4	3	2	1	Bit 0
0x025A	DDRP	R	0	0	**DDRP5**	**DDRP4**	**DDRP3**	DDRP2	DDRP1	**DDRP0**
		W								
0x025B	RDRP	R	0	0	0	0	0	RDRP2	RDRP1	**RDRP0**
		W								
0x025C	PERP	R	0	0	**PERP5**	**PERP4**	**PERP3**	PERP2	PERP1	**PERP0**
		W								
0x025D	PPSP	R	0	0	**PPSP5**	**PPSP4**	**PPSP3**	PPSP2	PPSP1	**PPSP0**
		W								
0x025E	PIEP	R	OCIE	0	**PIEP5**	**PIEP4**	**PIEP3**	PIEP2	PIEP1	**PIEP0**
		W								
0x025F	PIFP	R	OCIF	0	**PIFP5**	**PIFP4**	**PIFP3**	PIFP2	PIFP1	**PIFP0**
		W								
0x0271	PT1AD	R	0	0	**PT1AD5**	**PT1AD4**	**PT1AD3**	**PT1AD2**	PT1AD1	PT1AD0
		W								
0x0273	PTI1AD	R	0	0	**PTI1AD5**	**PTI1AD4**	**PTI1AD3**	**PTI1AD2**	PTI1AD1	PTI1AD0
		W								
0x0275	DDR1AD	R	0	0	**DDR1AD5**	**DDR1AD4**	**DDR1AD3**	**DDR1AD2**	DDR1AD1	DDR1AD0
		W								
0x0279	PER1AD	R	0	0	**PER1AD5**	**PER1AD4**	**PER1AD3**	**PER1AD2**	PER1AD1	PER1AD0
		W								
0x027B	PPS1AD	R	0	0	**PPS1AD5**	**PPS1AD4**	**PPS1AD3**	**PPS1AD2**	PPS1AD1	PPS1AD0
		W								
0x027D	PIE1AD	R	0	0	**PIE1AD5**	**PIE1AD4**	**PIE1AD3**	**PIE1AD2**	PIE1AD1	PIE1AD0
		W								
0x027F	PIF1AD	R	0	0	**PIF1AD5**	**PIF1AD4**	**PIF1AD3**	**PIF1AD2**	PIF1AD1	PIF1AD0
		W								

[1] Registers in **bold underlinded** are only available in S12VR64/48. On S12VR32/16 these locations read 0 and write is unimplemented.

Figure 3. Port module integration registers

3. Memory map

The memory map remains almost the same with relation to MC9S12VR64/48, the only exception being the space used for the SCI 1 (address 0x00D0-0x00D7) and SPI (address 0x00D8-0x00DF) modules. Writing to the related addresses has no effect and read access to these locations returns zero.

If none of these modules are being used in the application, no software modifications are required.

4. CPMU

The module S12CPMU_UHV_V8 has been enhanced with respect MC9S12VR64's version with the addition of:

- An optional oscillator clock monitor reset
- PLL clock monitor reset and reset flag (PMRF)
- Optional full swing mode for higher noise immunity.

These features are backward compatible with MC9S12VR64/48 derivatives. If these options are not used, no software adjustments are required since the features are disabled after reset. Figure 4 highlights additional fields and registers.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	PMRF
		W								
0x02FE	CPMUOSC2	R	0	0	0	0	0	0	OMRE	OSCMOD
		W								

New additions to VR32/16

Figure 4. Clock, Reset, and Power Management Unit enhancements

4.1. Oscillator clock monitor reset

If the external oscillator is enabled (OSCE = 1 in the CPMUOSC register) and the oscillator clock monitor reset is enabled (OMRE = 1 in the CPMUOSC2 register in Figure 4) then in case of loss of oscillation or if the oscillator frequency drops below the failure assert frequency (200-1200 kHz)[1], the module generates an Oscillator Clock Monitor Reset. It is highly recommended to enable this feature if an external clock is being used as clock source otherwise in case of loss of oscillation the system will stall.

[1] Values obtained from Appendix L XOSCLCP Electrical Specifications of the Reference Manual

NOTE

This feature is also available in the MC9S12VR64/48 derivatives but it is not optional, therefore it must be taken into account if the application uses an external oscillator as clock source.

4.2. PLL clock monitor reset

In case of loss of PLL clock oscillation or if the PLL clock frequency is below the failure assert frequency (0.45–1.6 MHz)[2], the module generates a PLL Clock Monitor Reset and the PLL Clock Monitor Reset Flag is asserted (PMRF field in the CPMUINT in Figure 4).

NOTE

This feature is available only in the MC9S12VR32/16 derivatives.

4.3. Optional full swing mode

Full swing mode for higher immunity against noise injection on the cost of higher power consumption and increased electromagnetic emission. After reset the module is configured for loop controlled mode (reduced amplitude on EXTAL and XTAL).

NOTE

This feature is only available in the MC9S12VR32/16 derivatives.

5. High Side Driver

The High Side Driver module has been enhanced with respect to MC9S12VR64's version with the following features:

- Open load detection
- Slew rate control

As long as the second high side driver is not being used, any MC9S12VR64/48 application is fully compatible with MC9S12VR32/16. No software modifications are required since the additional features are disabled at reset.

Figure 5 highlights new registers (new features) and those that are no longer available since they belonged to the additional high side driver implemented in the MC9S12VR64/48 derivatives.

2 Values obtained from Appendix E PLL Electrical Specifications of the Reference Manual

5.1. Open load detection

An open load detection can be enabled by setting HSOLE0. This feature is only active when the driver is enabled (HSDR0 = 1) and it is not being driven. To detect an open load condition, a small current will flow through the load. If the driving pin HS0 stays at a voltage above an internal threshold, then an open load will be detected and the open load flag will be asserted (HSOL0).

5.2. Slew rate control

This feature enables a major control over EMC behavior in order to achieve a much better EMC performance.

5.2.1. Slew current reduction enable

For EMC test purposes, the maximum output current will be reduced for ~4 µs when switched on to achieve a better EMC behavior if HS-Driver is being used as offboard driver. This bit is only writable when the high-side driver is disabled (HSE0 = 0).

5.2.2. Slew rate control enable

For EMC test purposes, the voltage slew rate will be controlled for ~8 µs when switched on to achieve a better EMC behavior if HS-Driver is being used as offboard driver. This bit is only writable when the high-side driver is disabled (HSE0 = 0).

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 HSDR	R	0	0	0	0	0	0	HSDR1	HSDR0
	W								
0x0001 HSCR	R	0	0	HSOCME1	HSOCME0	0	HSOLE0	HSE1	HSE0
	W								
0x0002 HSSLR	R	0	0	0	0	0	HSSLCU0	0	HSSLEN0
	W								
0x0005 HSSR	R	0	0	0	0	0	0	0	HSOL0
	W								
0x0007 HSIF	R	0	0	0	0	0	0	HSOCIF1	HSOCIF0
	W								

Not available on S12VR 32/16

New additions to S12VR 32/16

Figure 5. High Side Driver changes and enhancements

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