Freescale Semiconductor
Application Note

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Use of PGA on MC56F800x

Interaction of PDB, PGA and ADC

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Contents

1 Introduction

MC56F800x DSCs have two integrated Programmable Gain Amplifiers (PGA) that can amplify the differential signals by up to 32 times and convert it to the single ended signal, which is one of the on-chip ADC inputs.

On old maskset 1M53M devices, with PGA hardware trigger mode enabled in both PGAs, each Programmable Delay Block (PDB) trigger signal will cause a PGA to generate pre-trigger signal to both ADCs. This results in the ADC pre-trigger signal contention and the sample_select signal inside the ADCs may toggle and cause the wrong ADC status and control register to control the conversion.

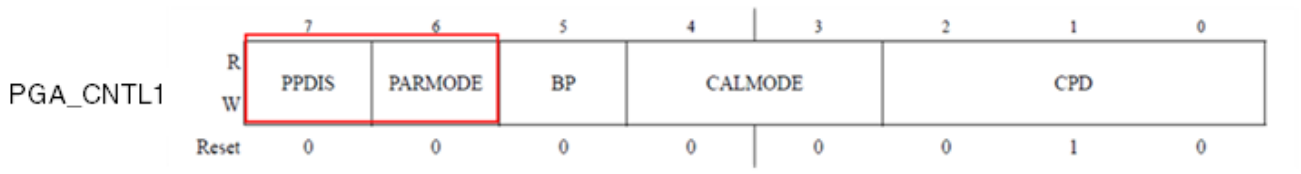
The new maskset devices (2M53M or newer) fixed this issue with new enhanced features and support sampling four analog signals per single hardware trigger. The applications designed for old maskset devices, can run smoothly on the new maskset devices.

This application note describes the new enhanced features of PGA and the possible valid PGA configurations for different signal sampling schemes.

2 PGA new features

Two new control bits are added: PARMODE bit (bit6) and PPDIS bit (bit7) in PGA_CNTL1.

Figure 1. PGA_CNTL1 register definition



- PPDIS bit - Ping-Pong disable bit:
  - 1 Allow only the Pretrigger to the associated ADC to be sent.
  - 0 Allow both Pretriggers to be sent to both ADCs.
- PARMODE bit -- PGA Parallel Mode bit:
  - 1 PGA Parallel Mode is enabled. PGA passes PDB Pretriggers to ADC Pretrigger inputs.
  - 0 PGA Parallel Mode is not enabled. PGA passes PGA generated Pretriggers to ADC Pretrigger inputs.

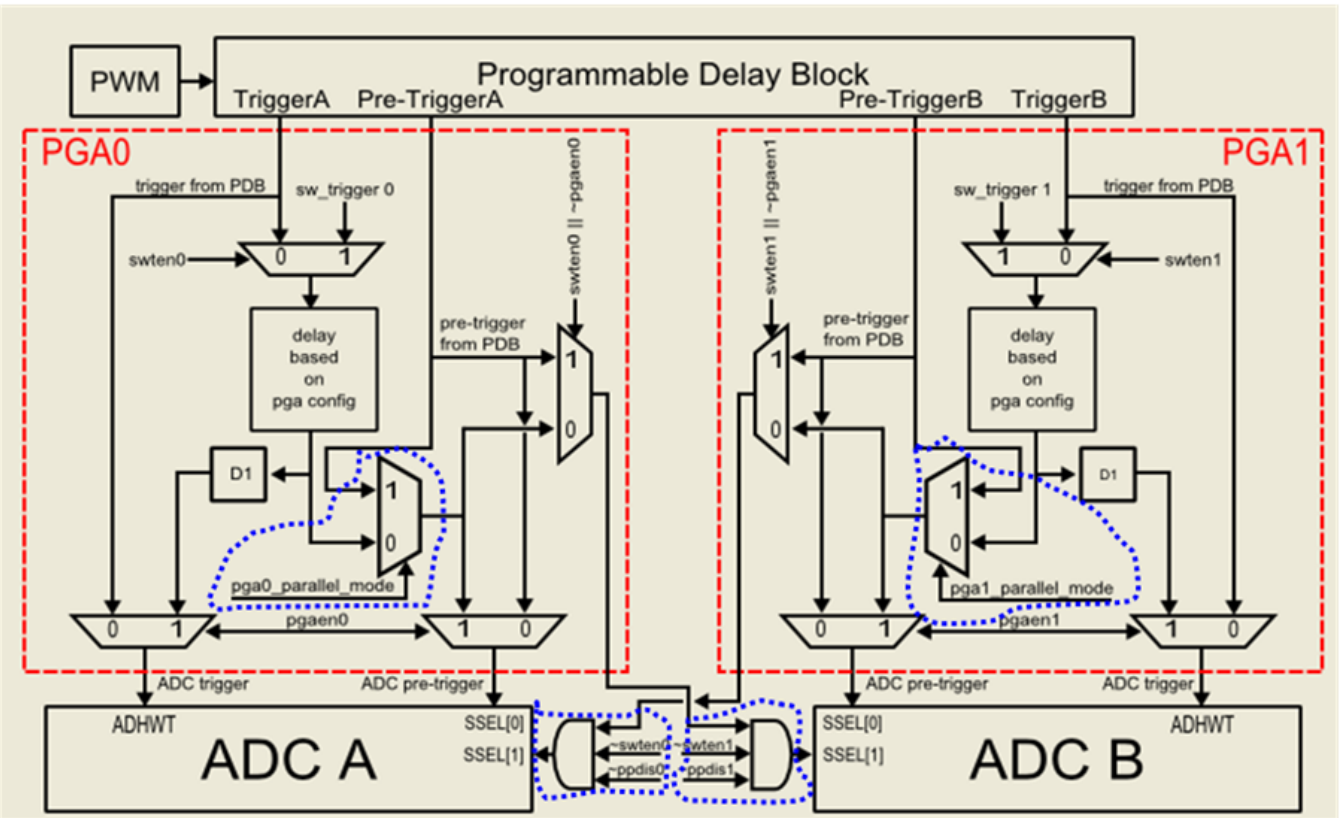
The PGA is designed to operate in conjunction with the ADC. The ADC has been enhanced to allow two different conversions to be pre-programmed into the ADC, using duplicate copies of the ADC status and control register 1. Conversions specified by ADCn_ADCSC1A and ADCn_ADCSC1B can be executed one after the other as a result of two sequential trigger events and the result will be stored in ADCn_ADCRA and ADCn_ADCRB respectively.

Prior to each conversion, a Pretrigger input into the ADC specifies whether ADCn_ADCSC1A or ADCn_ADCSC1B should control the next conversion. These Pretriggers occur one peripheral clock prior to the actual hardware trigger into the ADC. Because the PGA adds latency to each analog-to-digital conversion, ADC trigger and Pretrigger timing must be adjusted accordingly.

The Figure below shows the PGA diagram and the interaction between PDB, PGA and ADC. ADC A is acronym of ADC0, and ADC B is acronym of ADC1. The logics with blue circle in dotted lines are newly added. Each PGA is associated with a separate ADC module. Note that both ADCs get both Pretrigger. This allows simultaneous conversions on ADC 0 and ADC 1. If a PGA is not enabled for use, the associated PDB generated Pretriggers and trigger are passed unchanged. Likewise, use of a PGA software trigger causes the associated PDB pre-trigger to be available for use by the other ADC.

When the PGA is enabled for use with hardware trigger, it consumes the PDB generated trigger and Pretrigger, and generates new ones for use by the ADCs. One of the ADC Pretriggers generated by a PGA can be disabled to avoid contention with the other pre-trigger. Disabling both Pretriggers generated by both PGAs allow parallel independent ADC conversions.

Figure 2. Interaction between PDB, PGA and ADC



The valid PGA configurations for different ADC conversion mode are listed in Table below.

There are following restrictions:

- pga_parallel_mode bits need to be set to the same value in both PGAs and set to 1 during ping-pong mode
- ppdis bits are used to enable parallel independent conversions on ADC_A and ADC_B
- swten bits cannot be set on disabled PGA
- when swten is set, the corresponding parmode bit must be set to 0

NOTE

- pga0en is PGA0 enable signal (PGA0_CNTL0[EN])
- pga1en is PGA1 enable signal (PGA1_CNTL0[EN])
- swten0 is PGA0 software trigger mode enable signal (PGA0_CNTL0[TM])
- swten1 is PGA1 software trigger mode enable signal (PGA1_CNTL0[TM])
- pga0_parallel_mode is PGA0 parallel mode disable signal PGA0_CNTL1[PARMODE])
- pga1_parallel_mode is PGA1 parallel mode disable signal (PGA1_CNTL1[PARMODE])
- ppdis0 is PGA0 ping-pong disable signal (PGA0_CNTL1[PPDIS])
- ppdis1 is PGA1 ping-pong disable signal (PGA1_CNTL1[PPDIS])

Table 1. Valid PGA configurations for different ADC conversion modes

Mode	Trigger Setup	pga0en	pga1en	swten0	swten1	ppdis0	ppdis1	parmode0	parmode1
One-shot PGA disabled	PDB one-shot	0	0	0	0	X	X	X	X
Ping-Pong PGA disabled	PDB two-shot	0	0	0	0	0	0	X	X
One-shot PGA enabled	PDB one-shot	1	1	0	0	1	1	X	X
Ping-Pong PGA enabled	PDB two-shot	1	1	0	0	0	0	1	1
SW/HW trigger parallel independent	PGA0 SW trigger PDB trigger B one-shot	1	1	1	0	X	1	0	0
SW/HW trigger parallel independent	PGA1 SW trigger PDB trigger A one-shot	1	1	0	1	1	X	0	0
PGA SW trigger parallel independent	PGA SW trigger	1	1	1	1	X	X	0	0
PGA0 HW trigger single	PDB trigger A one-shot	1	0	0	0	1	X	0	0
PGA0 HW PGA1 bypass	PDB one-shot	1	0	0	0	1	X	0	0
PGA0 SW trigger single	PGA0 SW trigger	1	0	1	0	X	1	0	0
PGA1 HW trigger single	PDB trigger B one-shot	0	1	0	0	X	1	0	0
PGA1 HW trigger, PGA0 bypass	PDB one-shot	0	1	0	0	1	1	0	0
PGA1 SW trigger single	PGA1 SW trigger	0	1	0	1	1	X	0	0

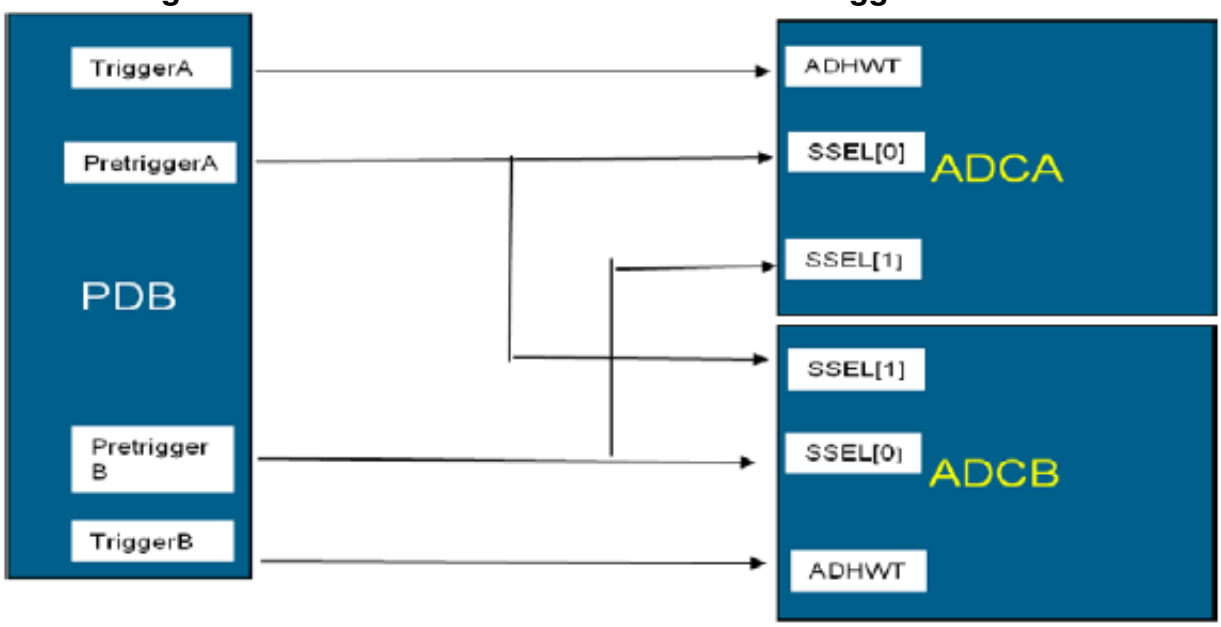
3 Valid PGA configurations

This section describes valid PGA configurations with reference to PDB triggers and ADC results for different sampling schemes. The PGA block may not be shown in the following figures in case the PGA is bypassed. PDB pre-trigger and trigger signals in PDB one-shot or two-shot mode are drawn in the following figures for the simplicity too. “X” for a register bit means don’t care.

3.1 One-shot PGAs Disabled, PDB Trigger A disabled

In this configuration, both PGAs are disabled and bypassed. Figure below depicts the interaction of the PDB, ADC in this configuration.

Figure 3. One-shot PGAs disabled with PDB Trigger A disabled



PGA setup is as below:

- PGA0_CNTL0[EN] = PGA1_CNTL0[EN] = 0;
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 0;
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = X;
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0;

PDB trigger setup is as below:

- PDB one-shot mode
- TriggerA is disabled
- TriggerB is enabled and function of Delay B only

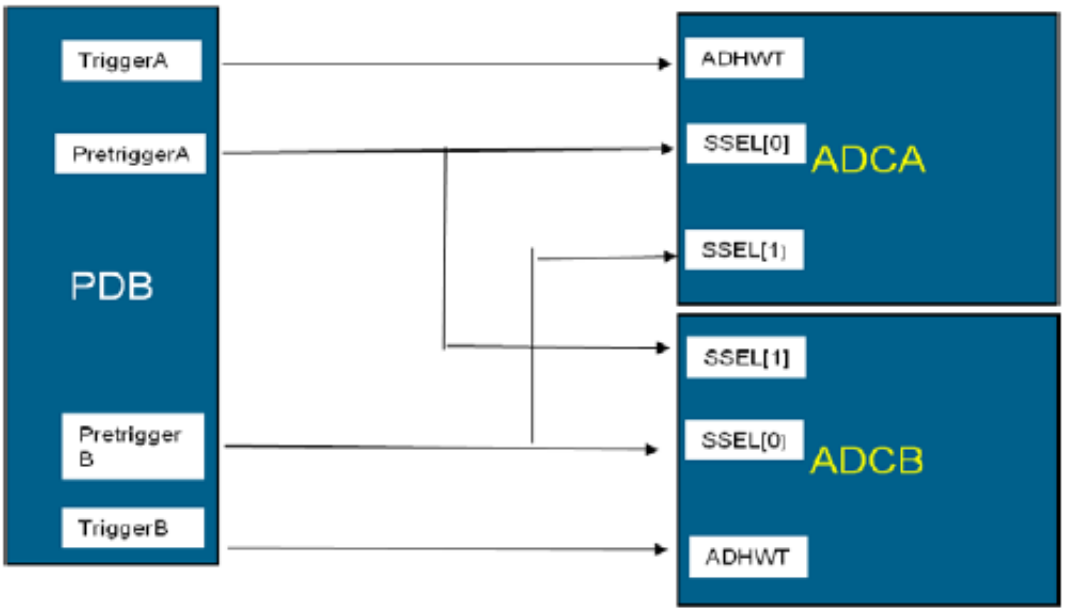
PDB PretriggerB selects ADC0_SC1B/ADCRB, ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 1 sample in ADCRA for ADCB.

3.2 One-shot PGA Disabled, PDB TriggerB disabled

In this configuration, both PGAs are disabled, and, bypassed. Figure below depicts the interaction of the PDB, ADC in this configuration.

Figure 4. One-shot PGAs disabled with PDB Trigger B disabled



PGA setup is as below:

- PGA0_CNTL0[EN] = PGA1_CNTL0[EN] = 0;
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 0;
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = X;
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0;

PDB trigger setup is as below:

- PDB one-shot mode
- TriggerA is enabled and function of Delay A only
- TriggerB is disabled

PDB PretriggerA selects ADC0_SC1A/ADCRA, ADC1_SC1B/ADCRB.

In this configuration, ADC samples per trigger is 1 sample in ADCRA for ADCA.

3.3 One-shot PGAs disabled, ping-pong disabled

In this configuration, both PGAs are disabled, bypassed, and both PGA's ping-pong are disabled. Figure below depicts the interaction of the PDB, ADC in this configuration.

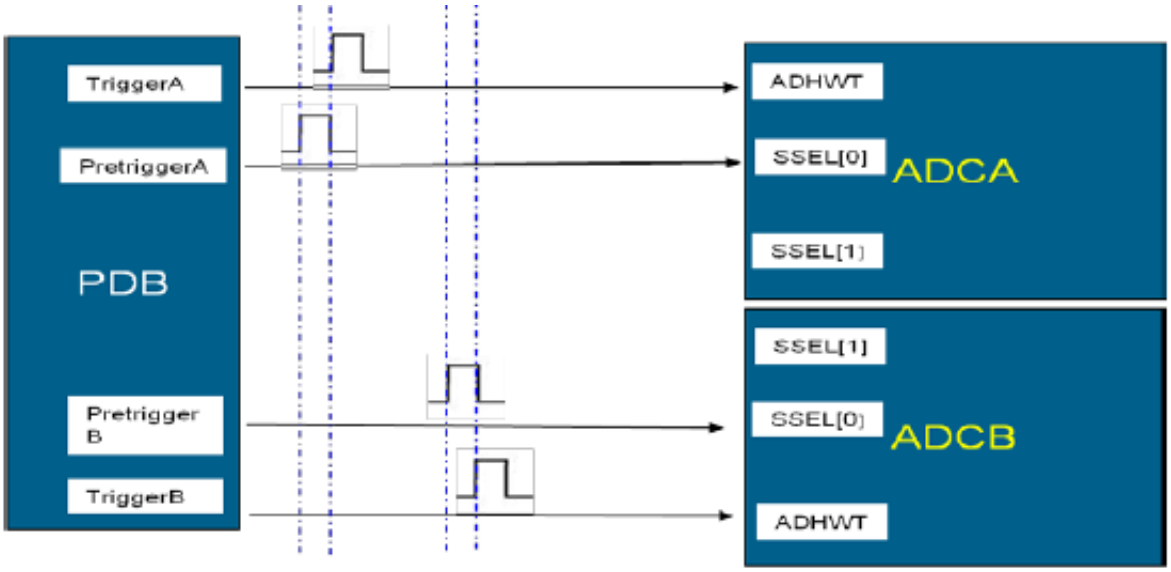


Figure 5. One-shot PGAs disabled, ping-pong disabled

PGA setup is as below:

- PGA0_CNTL0[EN] = PGA1_CNTL0[EN] = 0
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = X
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot
- Both TriggerA and TriggerB are enabled

PDB PretriggerA selects ADC0_SC1A/ADCRA .

PDB PretriggerB selects ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 1 sample in ADC0_ADCRA for ADCA and 1 sample in ADC1_ADCRA for ADCB.

3.4 Ping-Pong PGA Disabled

In this configuration, both PGAs are disabled, bypassed. Figure below depicts the interaction of the PDB, ADC in this configuration.

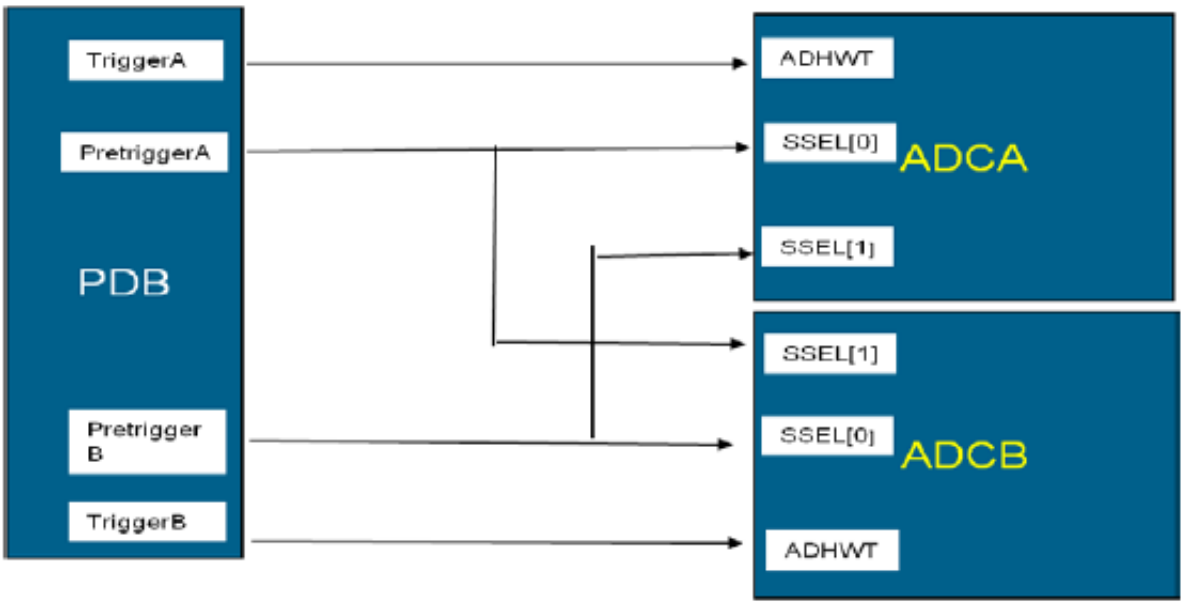


Figure 6. Ping-Pong PGA's disabled

PGA setup is as below:

- PGA0_CNTL0[EN] = PGA1_CNTL0[EN] = 0
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = X
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger setup is as below:

- PDB two-shot mode
- DelayB is greater than or equal to the DelayA plus the ADC conversion time or vice versa
- Both TriggerA and TriggerB are enabled and function of both Delay A and Delay B

PDB PretriggerA selects ADC0_SC1A/ADCRA, ADC1_SC1B/ADCRB.

PDB PretriggerB selects ADC0_SC1B/ADCRB, ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 4:

For ADCA, the first sample is in ADC0_ADCRA, the second sample in ADC0_ADCRB.

For ADCB, the first sample is in ADC1_ADCRB, the second sample in ADC1_ADCRA.

3.5 Ping-Pong PGA's enabled

In this configuration, both PGAs are enabled, and both PGA's parallel mode are enabled. Figure below depicts the interaction of the PDB, PGA and ADC in this configuration.

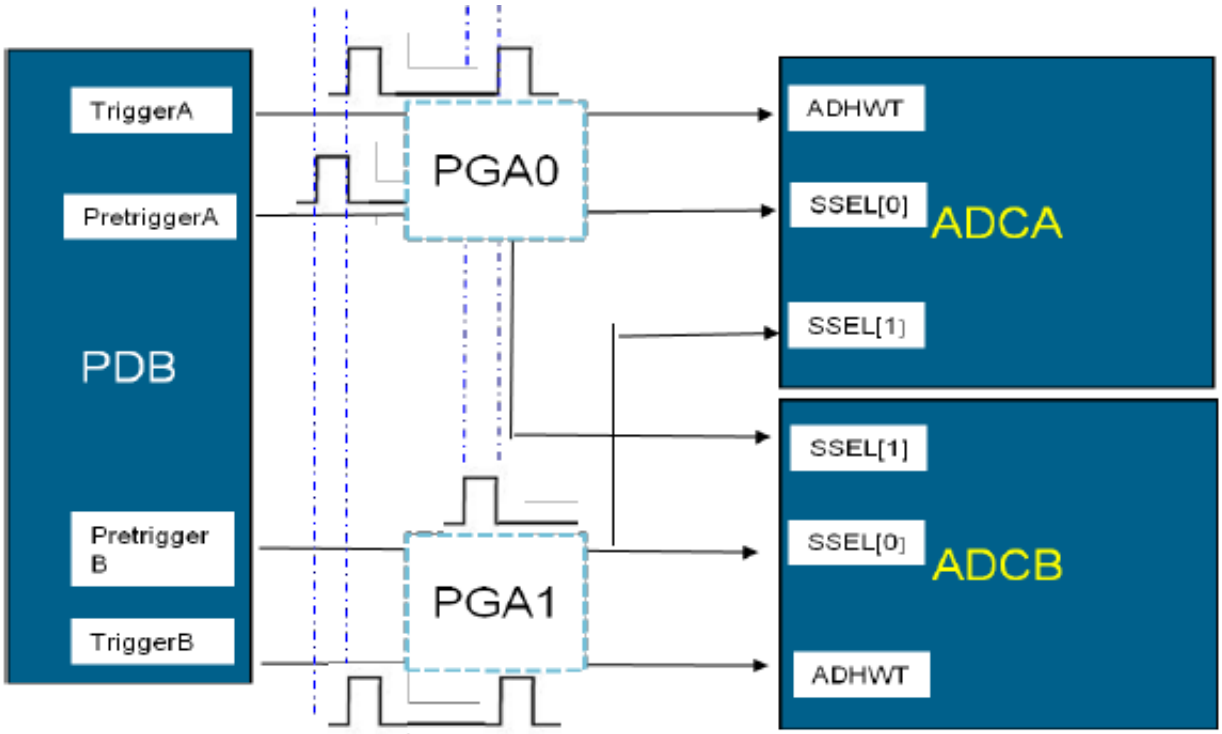


Figure 7. Ping-Pong PGAs Enabled

PGA setup is as below:

- PGA0_CNTL0[EN] = PGA1_CNTL0[EN] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 1
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 0
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot mode
- DelayB is greater than or equal to the DelayA plus the ADC conversion time or vice versa
- Both TriggerA and TriggerB are enabled and function of both Delay A and Delay B

PDB PretriggerA selects ADC0_SC1A/ADCRA, ADC1_SC1B/ADCRB.

PDB PretriggerB selects ADC0_SC1B/ADCRB, ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 4:

For ADCA, the first sample is in ADC0_ADCRA, the second sample is in ADC0_ADCRB. For ADCB, the first sample is in ADC1_ADCRB, the second sample is in ADC1_ADCRA.

3.6 One-shot PGA's enabled

In this configuration, both PGAs are enabled, but PGA's ping-pong are disabled, PGA's parallel mode are disabled too. Figure below depicts the interaction of the PDB, PGA,ADC in this configuration.

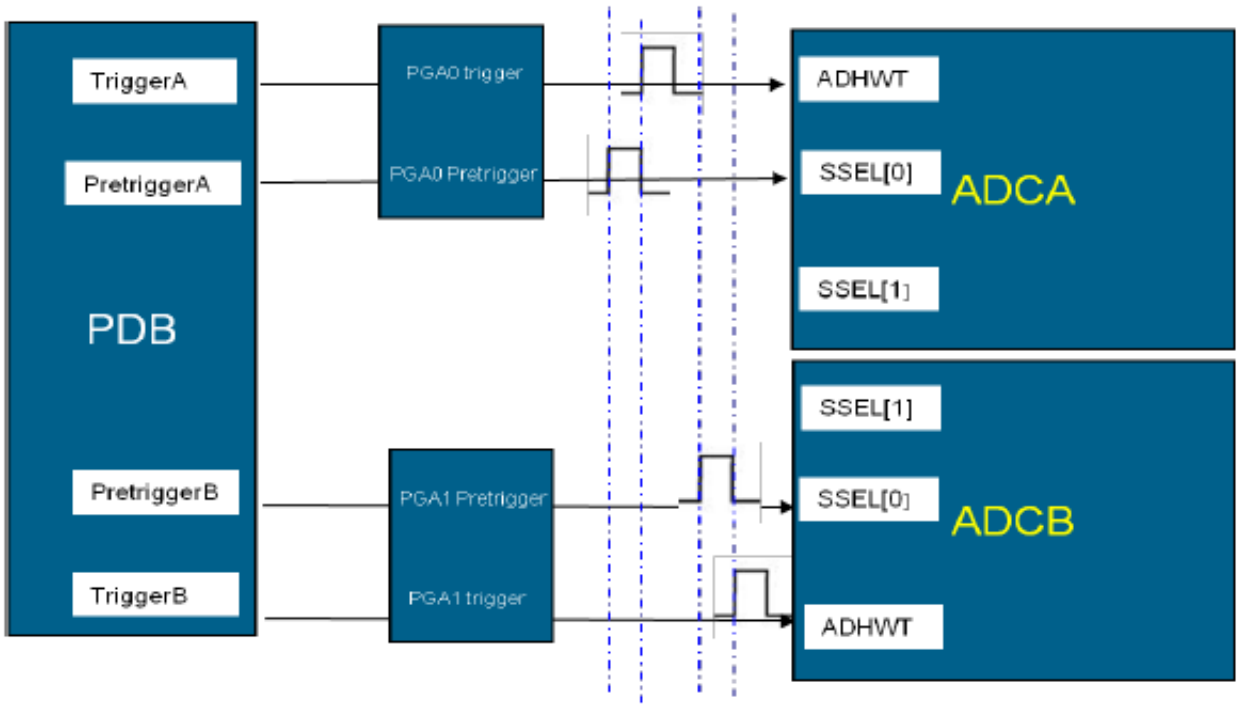


Figure 8. One-shot PGAs enabled

PGA setup is as below:

- PGA0_CNTL0[EN] = PGA1_CNTL0[EN] = 1
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot mode
- TriggerA is enabled and function of Delay A only
- TriggerB is enabled and function of Delay B only

PGA0 generated Pre-triggerA selects ADC0_SC1A/ADCRA.

PGA1 generated PretriggerB selects ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 2 samples:

- For ADCA, 1 sample is in ADC0_ADCRA
- For ADCB, 1 sample is in ADC1_ADCRA

3.7 One-shot PGA's enabled, parallel mode enabled

In this configuration, both PGAs are enabled, parallel mode is enabled, but PGA's ping-pong are disabled. Figure below depicts the interaction of the PDB, PGA,ADC in this configuration.

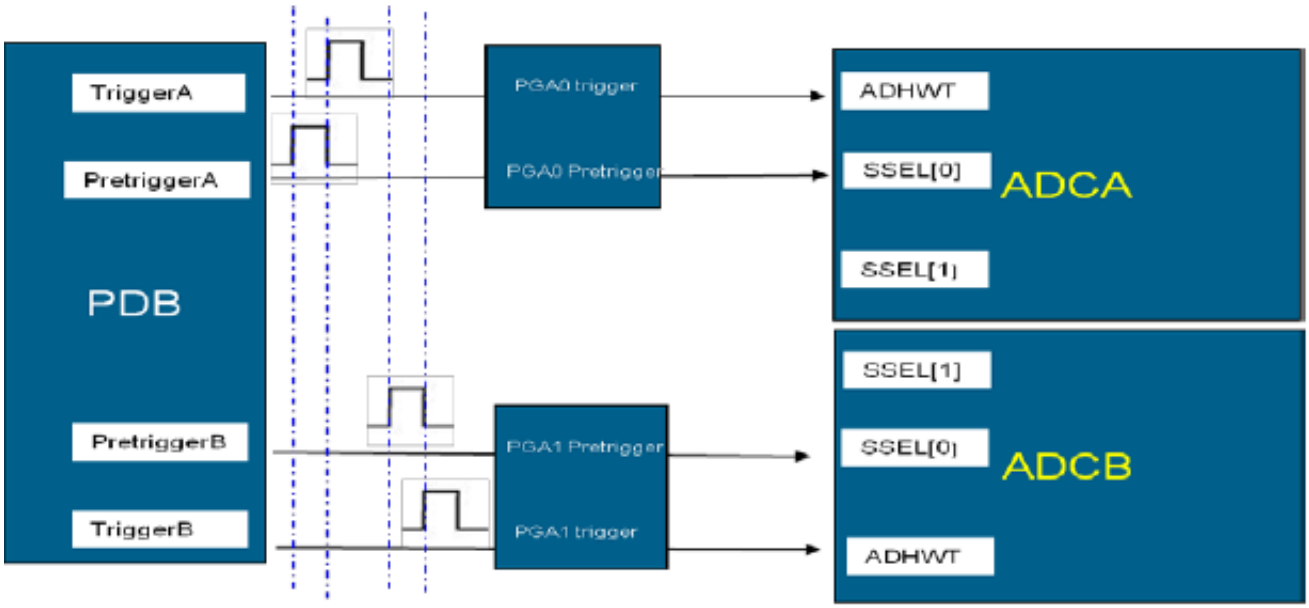


Figure 9. One-shot PGAs enabled, parallel mode enabled

PGA setup is as below:

- PGA0_CNTL0[EN] = PGA1_CNTL0[EN] = 1
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 1
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot mode
- TriggerA is enabled and function of Delay A only
- TriggerB is enabled and function of Delay B only

PDB PretriggerA selects ADC0_SC1A/ADCRA.

PDB PretriggerB selects ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 2 samples:

- For ADCA, 1 sample is in ADC0_ADCRA
- For ADCB, 1 sample is in ADC1_ADCRA

3.8 PGA0 HW PGA1 bypass

In this configuration, PGA0 is enabled, PGA1 is bypassed, both PGA's ping-pong are disabled. Figure below depicts the interaction of the PDB, ADC in this configuration.

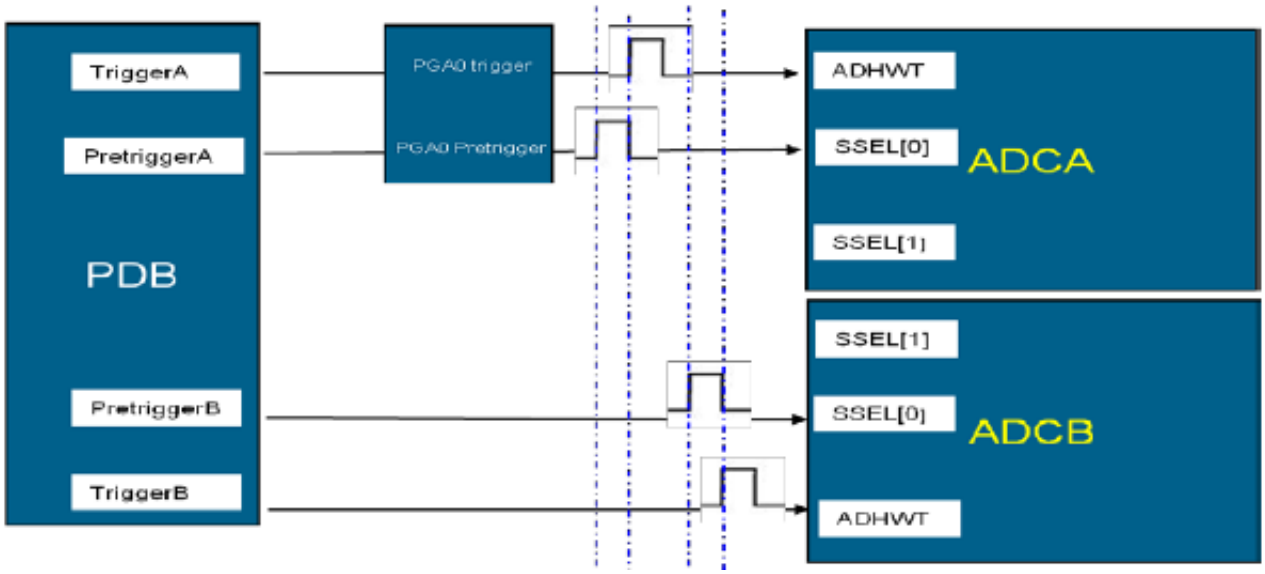


Figure 10. PGA0 HW PGA1 bypass

PGA setup is as below:

- PGA0_CNTL0[EN] =1, PGA1_CNTL0[EN] = 0
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot mode
- TriggerA is enabled and function of Delay A only
- TriggerB is enabled and function of Delay B only

PGA0 generated pretrigger selects ADC0_SC1A/ADCRA.

PDB Pretrigger B selects ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 2 samples:

- For ADCA, 1 sample is in ADC0_ADCRA
- For ADCB, 1 sample is in ADC1_ADCRA.

3.9 PGA0 HW trigger single

In this configuration, PGA0 is enabled, PGA1 is bypassed, both PGA's ping-pong are disabled. Figure below depicts the interaction of the PDB, PGA and ADC in this configuration.

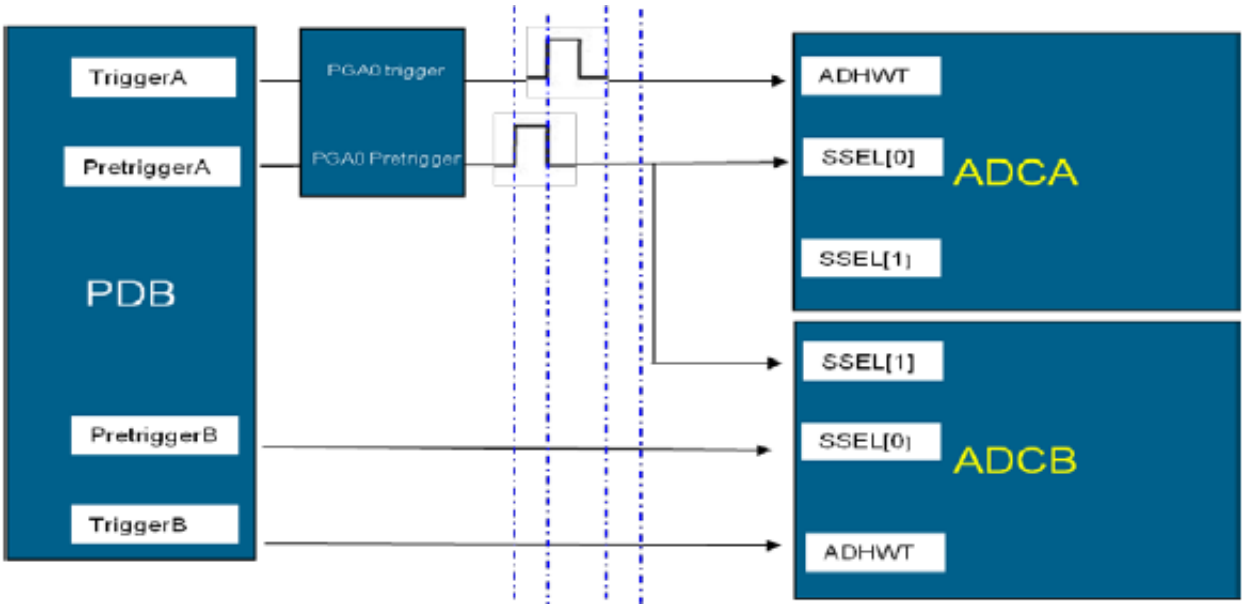


Figure 11. PGA0 HW trigger single

PGA setup is as below:

- PGA0_CNTL0[EN] =1, PGA1_CNTL0[EN] = 0
- PGA0_CNTL1[PPDIS] = 1,PGA1_CNTL1[PPDIS]= X
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot mode
- TriggerA is enabled and function of Delay A only
- TriggerB is disabled

PGA0 generated Pretrigger selects ADC0_SC1A/ADCRA, ADC1_SC1B/ADCRB.

In this configuration, ADC samples per trigger is 1 sample:

1 sample is in ADC0_ADCRA

3.10 PGA1 HW trigger PGA0 bypass

In this configuration, PGA1 is enabled, PGA0 is bypassed, both PGA's ping-pong are disabled. Figure below depicts the interaction of the PDB, PGA0, ADC in this configuration.

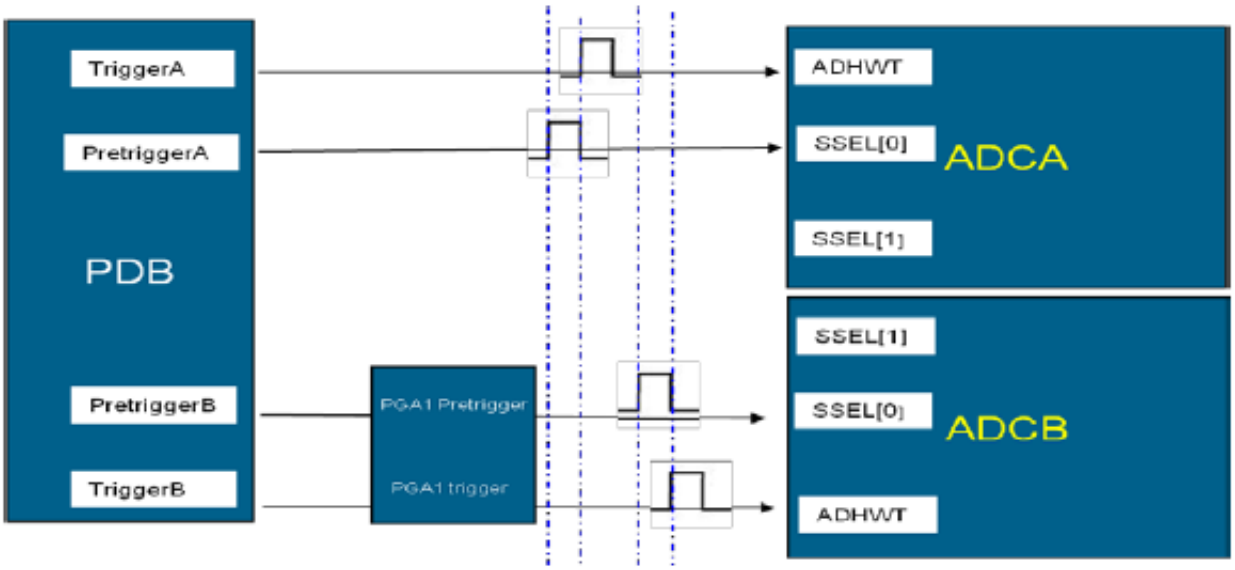


Figure 12. PGA1 HW trigger PGA0 bypass

PGA setup is as below:

- PGA0_CNTL0[EN] =0, PGA1_CNTL0[EN] = 1
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot mode
- TriggerA is enabled and function of Delay A only
- TriggerB is enabled and function of Delay B only

PGA1 generated Pretrigger selects ADC1_SC1A/ADCRA.

PDB PretriggerA selects ADC0_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 2 samples:

- For ADCA, 1 sample is in ADC0_ADCRA.
- For ADCB, 1 sample is in ADC1_ADCRA.

3.11 PGA1 HW trigger single

In this configuration, PGA1 is enabled, PGA0 is bypassed, PGA1's ping-pong is disabled. Figure below depicts the interaction of the PDB, PGA,ADC in this configuration.

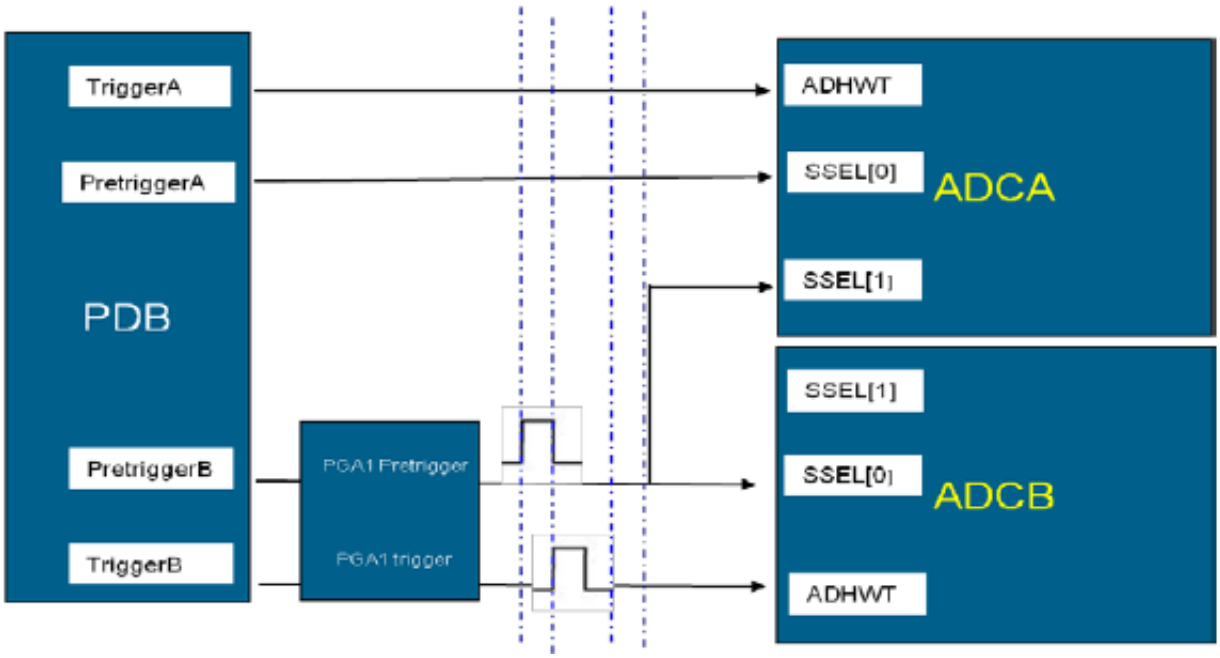


Figure 13. PGA1 HW trigger single

PGA setup is as below:

- PGA0_CNTL0[EN] =0, PGA1_CNTL0[EN] = 1
- PGA0_CNTL1[PPDIS] = X,PGA1_CNTL1[PPDIS]=1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0
- PGA0_CNTL0[TM] = PGA1_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot mode
- Trigger B is enabled and function of Delay B only
- Trigger A is disabled

PGA1 generated pretrigger selects ADC1_SC1A/ADCRA, and ADC0_SC1B/ADCRB.

In this configuration, ADC samples per trigger is 1 sample:

For ADCB, 1 sample is in ADC1_ADCRA.

3.12 SW/HW trigger parallel independent, PGA1 SW trigger PDB trigger A one-shot

In this configuration, both PGA are enabled, PGA0's ping-pong is disabled, PGA1 uses software trigger. Figure below depicts the interaction of the PDB, PGA, ADC in this configuration.

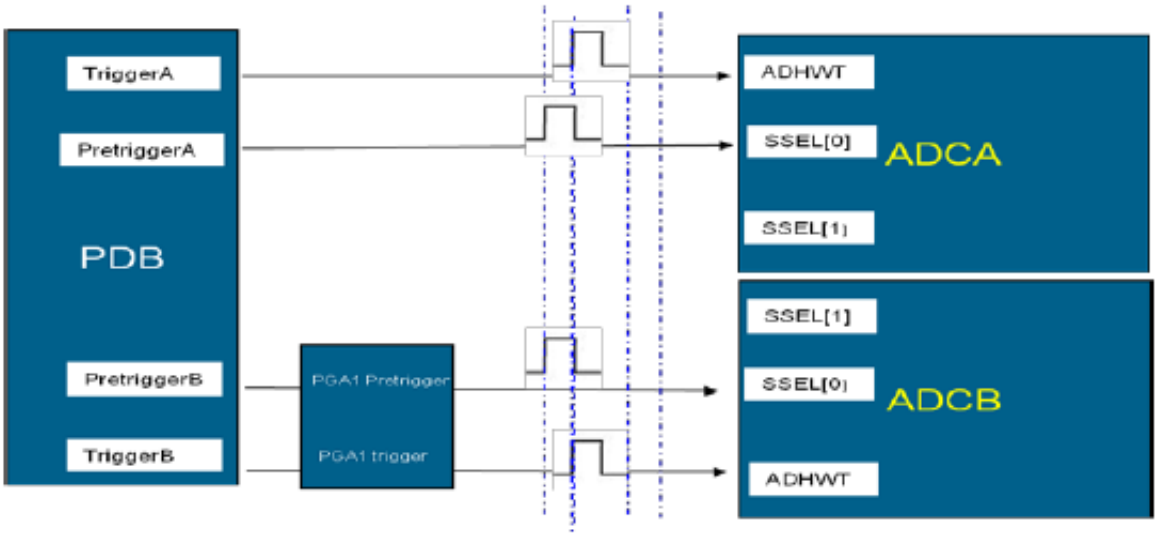


Figure 14. PGA1 SW trigger PDB trigger A one-shot

PGA setup is as below:

- PGA0_CNTL0[EN] =1, PGA1_CNTL0[EN] = 1
- PGA0_CNTL1[PPDIS] = 1, PGA1_CNTL0[TM] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0
- PGA1_CNTL1[PPDIS] = X, PGA0_CNTL0[TM] = 0

PDB trigger Setup is as below:

- PDB one-shot mode
- TriggerA is enabled and function of Delay A only
- Trigger B is enabled, but will be masked by PGA1

PGA1 generated pretrigger selects ADC1_SC1A/ADCRA.

PDB PretriggerA selects ADC0_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 2 samples:

- For ADCA, 1 sample is in ADC0_ADCRA
- For ADCB, 1 sample is in ADC1_ADCRA

3.13 SW/HW trigger parallel independent, PGA0 SW trigger PDB trigger B one-shot

In this configuration, both PGAs are enabled, PGA1's ping-pong is disabled, PGA0 uses software trigger. Figure below depicts the interaction of the PDB,PGA,ADC in this configuration.

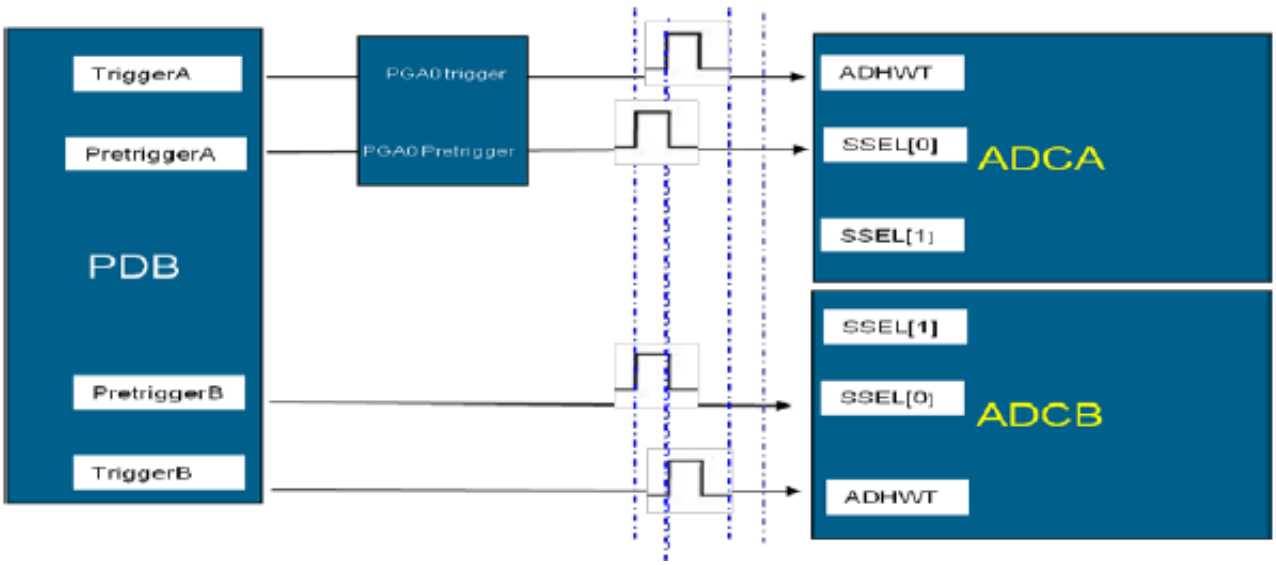


Figure 15. PGA0 SW trigger PDB trigger B one-shot

PGA setup is as below:

- PGA0_CNTL0[EN] =1, PGA1_CNTL0[EN] = 1
- PGA1_CNTL1[PPDIS] = 1, PGA0_CNTL0[TM] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0
- PGA0_CNTL1[PPDIS] =X, PGA1_CNTL0[TM] = 0

PDB trigger setup is as below:

- PDB one-shot mode
- Trigger B is enabled and function of Delay B only
- Trigger A is enabled, but will be masked by PGA0

PGA0 generated Pretrigger selects ADC0_SC1A/ADCRA.

PDB PretriggerB selects ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 2 samples:

- For ADCA, 1 sample is in ADC0_ADCRA
- For ADCB, 1 sample is in ADC1_ADCRA

3.14 PGA SW trigger parallel independent

In this configuration, both PGAs are enabled, both PGA use software trigger. Figure below depicts the interaction of the PDB, PGA and ADC in this configuration.

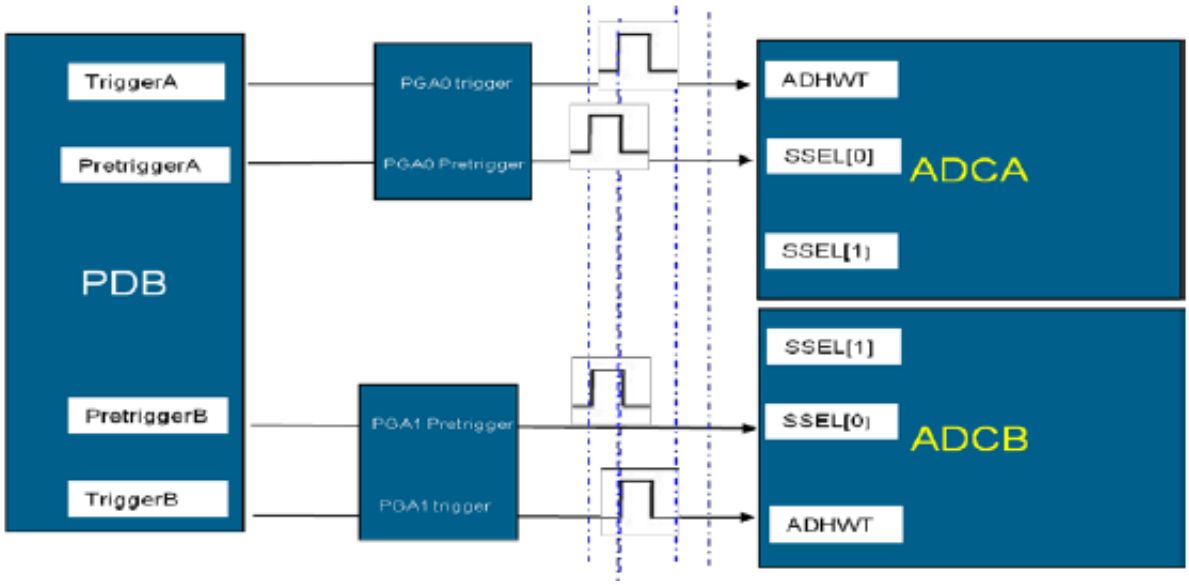


Figure 16. PGA SW trigger parallel independent

PGA setup is as below:

- PGA0_CNTL0[EN] =1, PGA1_CNTL0[EN] = 1
- PGA0_CNTL0[TM] = 1, PGA1_CNTL0[TM] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0
- PGA0_CNTL1[PPDIS] = PGA1_CNTL1[PPDIS] = X

PDB trigger setup is as below:

- PDB one-shot mode
- Trigger B and Trigger A are enabled, but will be masked by both PGAs

PGA0 generated Pretrigger selects ADC0_SC1A/ADCRA.

PGA1 generated Pretrigger selects ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 2 samples:

- For ADCA, 1 sample is in ADC0_ADCRA
- For ADCB, 1 sample is in ADC1_ADCRA

3.15 PGA0 SW trigger single

In this configuration, PGA0 is enabled, PGA1 is bypassed, PGA0 uses software trigger, PGA1's ping-pong is disabled. Figure below depicts the interaction of the PDB, PGA, ADC in this configuration.

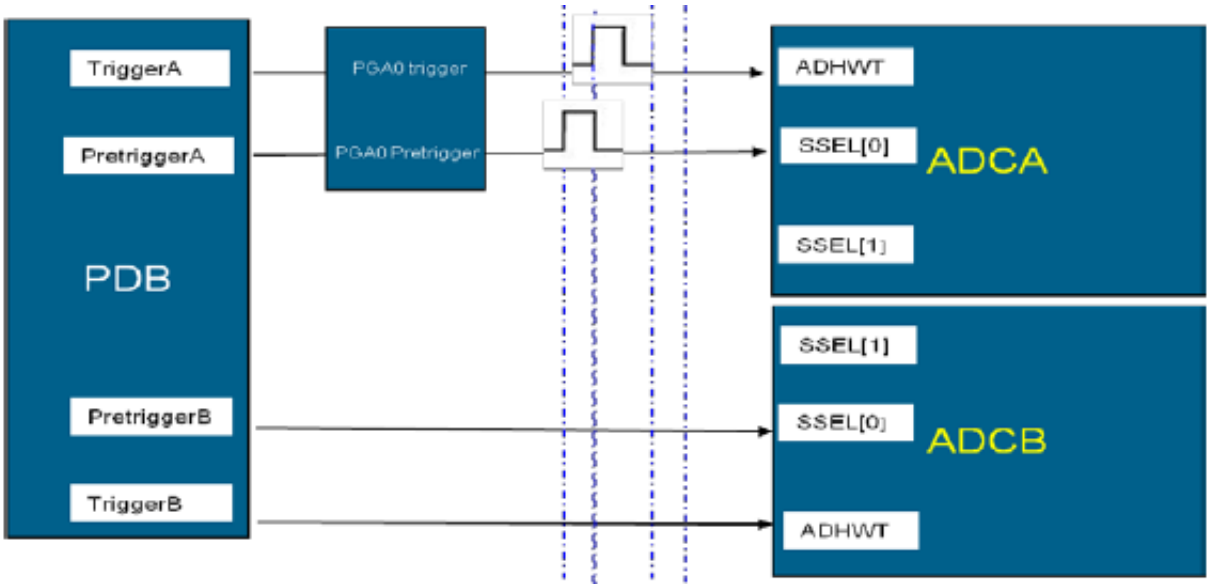


Figure 17. PGA0 SW trigger single

PGA setup is as below:

- PGA0_CNTL0[EN] =1, PGA1_CNTL0[EN] = 0
- PGA0_CNTL0[TM] = 1, PGA1_CNTL0[TM] = 0
- PGA0_CNTL1[PPDIS] = X,PGA1_CNTL1[PPDIS] = 1
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0

PDB trigger setup is as below:

- PDB one-shot mode
- Trigger A is enabled, but will be masked by PGA0
- Trigger B is disabled

PGA0 generated Pretrigger selects ADC0_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 1 sample:

- For ADCA, 1 sample is in ADC0_ADCRA.

3.16 PGA1 SW trigger single

In this configuration, PGA1 is enabled, PGA0 is bypassed, PGA1 uses software trigger, PGA0's ping-pong is disabled. Figure below depicts the interaction of the PDB, PGA, ADC in this configuration.

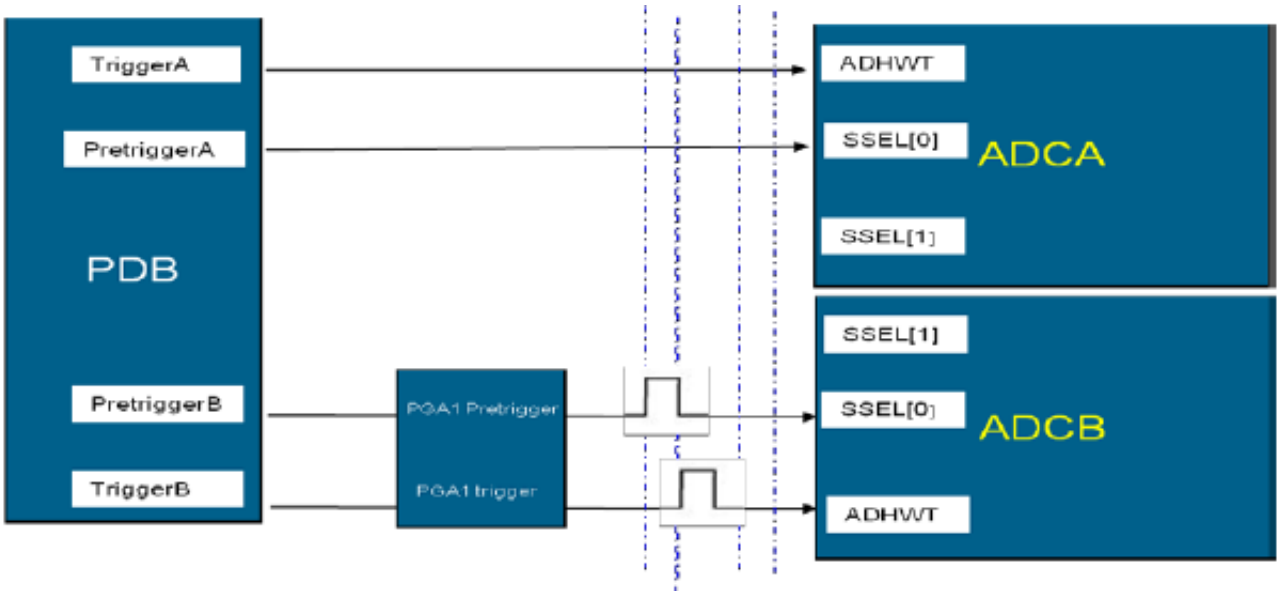


Figure 18. PGA1 SW trigger single

PGA setup is as below:

- PGA1_CNTL0[EN] =1, PGA0_CNTL0[EN] = 0
- PGA1_CNTL0[TM] = 1, PGA0_CNTL0[TM] = 0
- PGA0_CNTL1[PPDIS] = 1,PGA1_CNTL1[PPDIS] = X
- PGA0_CNTL1[PARMODE] = PGA1_CNTL1[PARMODE] = 0

PDB trigger setup is as below:

- PDB one-shot mode
- Trigger B is enabled, but will be masked by PGA1
- Trigger A is disabled

PGA1 generated Pretrigger selects ADC1_SC1A/ADCRA.

In this configuration, ADC samples per trigger is 1 sample:

- For ADCB, 1 sample is in ADC1_ADCRA.

4 Conclusion

There are l6 PGA configurations introduced in this application note. A PGA configuration can be selected based on the specific application requirements. To get four samples per hardware trigger, the recommended PGA configuration is Ping-Pong PGA's enabled in case both PGAs are used, or Ping-Pong PGA's disabled. To get two samples per hardware trigger, the recommended PGA configurations are One-shot PGA's enabled with parallel mode enabled, One-shot PGA's disabled with ping-pong disabled, One-shot PGA's disabled with PDB Trigger A disabled, One-shot PGA's disabled with PDB Trigger B disabled. These configurations eliminate the possible contentions between the PGA generated Pretrigger signals and are safe to get exact number of samples per hardware trigger.

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