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Architectural Differences between the i.MX23, i.MX25, and i.MX28

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Contents

1 Introduction

This application note describes the key architectural differences between the i.MX23, i.MX25, and i.MX28 ARM® based 32-bit applications processors. This application note provides an overview on several aspects of these processors which includes core, security, peripherals, and connectivity. It compares the different features of the processors.

2 Overview

The i.MX23 is a System on Chip (SoC) designed for applications such as portable media players, portable navigation devices and other handheld multimedia devices that require low-power, high performance and integration, and quality audio and video playback. The 90 nm SoC is based on the ARM926EJ-S™ core, coupled with the on-chip audio and power management functions. This highly integrated SoC eliminates the use of discrete ICs (more than 10 in number) found in the portable navigation devices. Unlike the other ICs based on the ARM9™ core, the i.MX23 integrates the analog functions on the same silicon die as that of the processor. For more information, refer to the

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i.MX23 Applications Processor Reference Manual (IMX23RM) and *i.MX23 Applications Processor Data Sheet* (IMX23EC).

The i.MX25 multimedia applications processor includes several key features that allow the user to reduce the overall system bill of materials cost such as Double Data Rate 2 (DDR2) support, two embedded USB PHYs, 3.3 V I/O support, general purpose 12-bit Analog to Digital Converters (ADCs), and Touch Screen Controller (TSC). In addition, the i.MX25 makes the industrial and general embedded market a key focus, with the integration of 10/100 Ethernet Media Access Control (MAC), Secure Digital Input/Output (SDIO) connectivity, resolution up to Super Video Graphics Array (SVGA) (800 × 600) Thin Film Transistor (TFT) Liquid Crystal Display (LCD) support, camera sensor interface, and 400 MHz CPU speed grade. The i.MX25 processor provides an additional tamper detection security that monitors and helps to prevent against system integrity attacks from hackers. Therefore, the i.MX25 processor is recommended for any type of secure device (wired or wireless payment terminal, Point-of-Scale (POS)), or any other type of product that requires secure system boot and tamper detection. The i.MX25 also complements the i.MX ARM11™ portfolio by maintaining a large share of peripheral commonality with the i.MX35 multimedia applications processor family. For more information, refer to the *i.MX25 Multimedia Applications Processor Reference Manual* (IMX25RM), *i.MX25 Applications Processor for Consumer and Industrial Products* (IMX25CEC), and *i.MX25 Applications Processor for Automotive Products* (IMX25AEC).

The i.MX28 is a low-power, high performance applications processor optimized for the general embedded industrial and consumer markets. The i.MX28 is based on the ARM926EJ-S core with speed up to 454 MHz coupled with the Power Management Unit (PMU). The i.MX28 can be connected to the devices such as high speed USB, Controller Area Network (CAN), Secured Digital (SD)/SDIO/Multi Media Card (MMC) and 10M/100M Ethernet. The i.MX28 is suitable for a wide range of applications including Human Machine Interface (HMI) panels, industrial drive, Programmable Logic Controller (PLC), I/O control display, factory robotics display, handle scanners and printers, POS terminals, patient monitoring devices, and smart energy meters. For more information, refer to the *i.MX28 Applications Processor Reference Manual* (IMX28RM), *i.MX28 Applications Processor Data Sheet for Consumer and Industrial Products* (IMX28CEC), and *i.MX28 Applications Processor Data Sheet for Automotive Products* (IMX28AEC).

Table 1 provides the features of the i.MX23, i.MX25, and i.MX28 processors.

Table 1. Features of the i.MX23, i.MX25, and i.MX28 Processors

Feature	i.MX23	i.MX25	i.MX28
System Core			
Micro Controller Unit (MCU) core	ARM926EJ-S, 454 MHz	ARM926EJ-S, 400 MHz	ARM926EJ-S, 454 MHz
Caches	16-Kbyte data and 16-Kbyte instruction	16-Kbyte data and 16-Kbyte instruction	32-Kbyte data and 16-Kbyte instruction
On-chip RAM	32 Kbyte	128 Kbyte	128 Kbyte
On-chip ROM	64 Kbyte	32 Kbyte	128 Kbyte
On-chip Secure RAM	N/A	2 Kbyte	N/A
On-Chip One-Time-Progammable (OCOTP)	1 Kbit	IC Identification Module (IIM)	1280 bit

Table 1. Features of the i.MX23, i.MX25, and i.MX28 Processors (continued)

Feature	i.MX23	i.MX25	i.MX28
Embedded Trace Macrocell (ETM)	Yes	Yes	Yes
Joint Test Action Group (JTAG) Interface	1-wire serial/6-wire parallel	Secure JTAG (parallel only)	6-wire parallel
Security Features			
Security hardware	Data Co-Processor (DCP): • Advanced Encryption Standard (AES) • Hashing	Runtime Integrity Checker v3 (RTICv3) Secure RAM Module and Security Monitor (SCCv3) DryIce Random Number Generator (RNGB)	DCP: • AES • Hashing
One-Time programmable storage	1-Kbit OCOTP ROM	IIM	1280-bit OCOTP ROM
Secure RAM	N/A	2 Kbyte	N/A
Secure JTAG	N/A	Yes	N/A
Secure Boot	128-bit AES hardware decryption	High Assurance Boot (HAB) with SHA-256	128-bit AES hardware decryption HAB with SHA-256
External Memory and Storage			
Memory and storage hardware interface	External Memory Interface (EMI) General Purpose Media Interface (GPMI) • NAND Flash Synchronous Serial Port (SSP)	EMI • Multi-Master Memory Interface (M3IF) • Enhanced SDRAM Controller (ESDRAMC) • NAND Flash Controller (NFC) • Wireless Extension Interface Module (WEIM) Advanced Technology Attachment (ATA) Enhanced SD Host Interface (eSDHC)	EMI GPMI • NAND Flash SSP
SDRAM	2.5 V DDR1 1.8 V Mobile DDR (mDDR)	3.3 V SDRAM 1.8 V DDR2 1.8 V mDDR	1.8 V DDR2 1.8 V mDDR 1.5 V Low Power DDR2 (LP-DDR2)
NAND Flash	Four 8-bit/16-bit NAND Single Level Cell (SLC)/Multiple Level Cell (MLC) NAND 8-bit Reed-Solomon Error Correction Code (ECC) 20-bit BCH ECC	Four 8-bit/16-bit NAND SLC/MLC NAND 8-bit Reed Solomon ECC Internal RAM Buffer	Eight 8-bit/16-bit NAND SLC/MLC NAND 20-bit BCH ECC
NOR Flash	N/A	Yes	N/A

Table 1. Features of the i.MX23, i.MX25, and i.MX28 Processors (continued)

Feature	i.MX23	i.MX25	i.MX28
ATA	N/A	UDMA-5	N/A
SD/MMC	eMMC 4.2, eMMC 4.3 (limited)	eMMC 4.3	eMMC 4.3, eMMC 4.4
Audio Features			
Serial audio interface	Dual Serial Audio Interface (SAIF) half-duplex	Enhanced Serial Audio Interface (ESAI) full-duplex	Dual SAIF half-duplex
Sony-Philips Digital Interface Format (SPDIF) digital audio out	Yes	N/A	Yes
Digital audio multiplexer	N/A	Yes	N/A
Analog audio outputs	Stereo headphone amplifier Mono speaker amplifier	N/A	N/A
Analog audio inputs	Mono microphone input Two stereo line inputs	N/A	N/A
Display and Video			
LCD Interface (LCDIF)	Yes	Yes	Yes
Resolution	Up to 640 × 480	Up to 800 × 600	Up to 800 × 480
Bit/Pixel	8, 16, 18, 24 (color)	1, 2, 4 (mono) 4, 8, 12, 16, 18, 24 (color)	8, 16, 18, 24 (color)
TV-Out	Yes	N/A	N/A
Display processing	Pixel Processing Pipeline (PXP) 8 Overlays Color key/Alpha blend Color space conversion and scaling Rotation	1 Overlay (Graphic window) Color key/Alpha blend Panning	PXP 8 Overlays Color key/Alpha blend Color space conversion and scaling Rotation
CMOS Sensor Interface (CSI)	N/A	Yes	N/A
Linear image scanner interface	N/A	N/A	High Speed Analog to Digital Conversion (HSADC)
Power Management			
Internal power supply	DC-DC switched converter Four linear regulators • 3.3 V • 1.2 V • 1.8 V • 2.5 V	N/A	DC-DC switched converter Four linear regulators • 3.3 V • 1.2 V • 1.8 V • 1.5 V

Table 1. Features of the i.MX23, i.MX25, and i.MX28 Processors (continued)

Feature	i.MX23	i.MX25	i.MX28
Power management	Adaptive Voltage Control (AVC) CLK_H auto-slow Clock gating Silicon speed sensor Multiple peripheral clock (domains)	Dynamic Voltage and Frequency Scaling (DVFS) Clock gating Active Well Bias (AWB)	AVC CLK_H auto-slow Clock gating Silicon speed sensor Multiple peripheral clock (domains)
Low-power mode	Standby Deep-sleep	Wait Doze Stop Sleep	Standby Deep-sleep
Network			
Ethernet	N/A	One Fast Ethernet Controller (FEC) 10/100	Two Ethernet Controller (ENET) 10/100
IEEE1588 Hardware Timestamp	N/A	N/A	Yes
3-port L2 switch	N/A	N/A	Yes
CAN	N/A	Dual CAN (FlexCAN)	Dual CAN (FlexCAN)
Communications			
Universal Asynchronous Receiver/Transmitter (UART)	Three	Five	Six
UART speed	Up to 3.25 mega bits per second (Mbps)	Up to 4 Mbps	Up to 3.25 Mbps
Infrared Data Association (IrDA)	N/A	UART IrDA compatible	N/A
I^2C interface	One	Three	Two
Serial Peripheral Interface (SPI)	SSP	Configurable Serial Peripheral Interface (CSPI) Synchronous Serial Interface (SSI)	SSP
Subscriber Identification Module (SIM)	N/A	Yes	N/A
1-wire module	N/A	Yes	N/A
SDIO Rev. 2.0	Yes	Yes	Yes
I/O Modules			
USB 2.0 High Speed	1 HS port (Host) with HS PHY (does not support LS)	1 HS port (On-The-Go (OTG)) with HS PHY and 1 HS port (Host) with FS PHY	1 HS port (OTG) with HS PHY and 1 HS port (Host) with HS PHY
Pulse Width Modulator (PWM)	Five channels	Four channels	Eight channels
General Purpose I/O (GPIO)	Yes	Yes	Yes
Input/Output Multiplexer (IOMUX)	Pin multiplexing scheme	Yes	Pin multiplexing scheme

Table 1. Features of the i.MX23, i.MX25, and i.MX28 Processors (continued)

Feature	i.MX23	i.MX25	i.MX28
Low Resolution ADC (LRADC)	Yes (12-bit resolution)	Yes (12-bit resolution)	Yes (12-bit resolution)
TSC	Yes (4-wire resistive)	Yes (4-wire or 5-wire resistive)	Yes (4-wire or 5-wire resistive)
Keypad Port (KPP)	N/A	Yes	N/A
Boot Modes			
I^2C	Yes	Yes	Yes
SPI	Yes	Yes	Yes
SD/MMC	Yes	Yes	Yes
NAND	Yes	Yes	Yes
JTAG	Yes	Yes	Yes
NOR Flash	N/A	Yes	N/A
USB	Yes	N/A	Yes
UART	N/A	Yes	N/A
WEIM	N/A	Yes	N/A

3 System Core

The core of the i.MX23, i.MX25, and i.MX28 is fast, proven, power efficient implementation of the ARM926EJ-S core. These processors include a stand-alone ARM CoreSight Embedded Trace Marcocell, ETM9CSSingle that provides instruction trace and data trace for the ARM9 microprocessor.

Figure 1 shows the ARM926 RISC processor core.

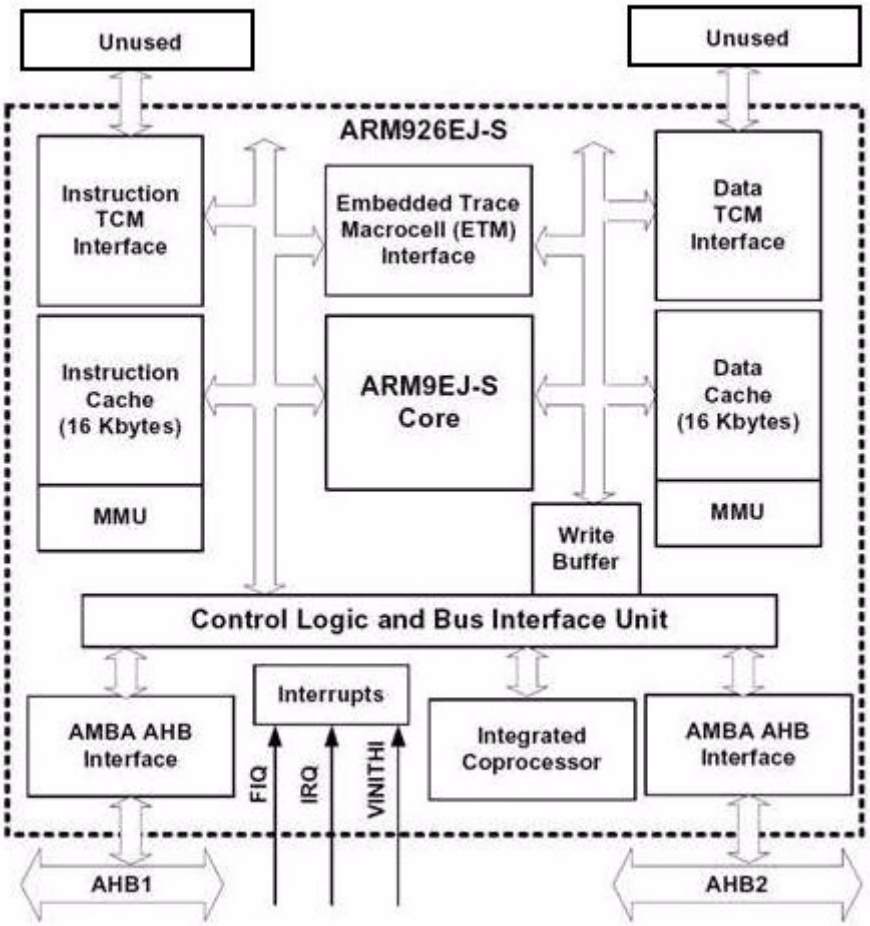


Figure 1. ARM926 RISC Processor Core

Table 2 shows the comparison of the system core features of the i.MX23, i.MX25, and i.MX28.

Table 2. Comparison of System Core Features

Feature	i.MX23	i.MX25	i.MX28
MCU core	ARM926EJ-S, 454 MHz	ARM926EJ-S, 400 MHz	ARM926EJ-S, 454 MHz
Cache	16-Kbyte data and 16-Kbyte instruction	16-Kbyte data and 16-Kbyte instruction	32-Kbyte data and 16-Kbyte instruction
On-chip RAM	32 Kbyte	128 Kbyte	128 Kbyte
On-chip ROM	64 Kbyte	32 Kbyte	128 Kbyte
On-chip Secure RAM	N/A	2 Kbyte	N/A
OCOTP	1 Kbit	IIM	1280 bit
ETM	Yes	Yes	Yes
JTAG Interface	1-wire serial/6-wire parallel	Secure JTAG (parallel only)	6-wire parallel

3.1 i.MX23 System Core

The i.MX23 can run up to 454 MHz. The i.MX23 includes a 16-Kbyte data cache, 16-Kbyte instruction cache, 32-Kbyte on-chip RAM, and 64-Kbyte on-chip ROM. The i.MX23 includes a serial JTAG module that maps 1-wire protocol to 6-wire JTAG interface. The HW_DIGCTL_USE_SERIAL_JTAG bit in the digital control block selects the serial or parallel JTAG to be used. The default configuration is set by the USE_PARALLEL_JTAG bit in HW_OCOTP_ROM0 in the OCOTP ROM. It is loaded by the ROM code during the boot up. If the bit is not blown, the serial JTAG is used by default.

The i.MX23 includes a 1-Kbit OCOTP ROM to store the hardware and software capability bits, ROM configuration bits, processor operations, and unique-ID fields. The OCOTP ROM can also be used to store customer programmable cryptography key. Four words storage is also available for general use. In addition, a 32-bit word is dedicated to control the read and write locking of several One-Time-Programmable (OTP) regions that are copied into the shadow register.

3.2 i.MX25 System Core

The i.MX25 can run up to 400 MHz. The i.MX25 includes a 16-Kbyte data cache, 16-Kbyte instruction cache, 128-Kbyte on-chip RAM, 32-Kbyte on-chip ROM, and 2-Kbyte on-chip secure RAM to store sensitive information. The i.MX25 includes a secure JTAG port which protects the debug port from system integrity attack by regulating or blocking the access to the system debug features.

The i.MX25 has an IIM which provides the primary user visible mechanism for interfacing with the on-chip fuse elements. The fuses are used for unique chip identifiers, mask version numbers, cryptographic keys, and several control signals that require permanent non-volatility. The IIM can also provide up to 28 volatile control signals and can generate a second 168-bit SCC key.

3.3 i.MX28 System Core

The i.MX28 can run up to 454 MHz. The i.MX28 includes 32-Kbyte data cache, 16-Kbyte instruction cache, 128-Kbyte on-chip RAM, and 128-Kbyte on-chip ROM. The i.MX28 includes a 6-wire parallel JTAG interface for debugging.

The i.MX28 includes 1280 bits of OCOTP ROM to store hardware and software capability bits, ROM configuration bits, processor operations, and unique-ID fields. The OCOTP ROM can also be used to store customer programmable cryptography key. Four words storage is also available for general purpose. In addition, a 32-bit word is dedicated to control the read and write locking of several OTP regions, which are copied into the shadow register.

4 Security Features

Table 3 shows a comparison of the security features of the i.MX23, i.MX25, and i.MX28.

Table 3. Comparison of Security Features

Feature	i.MX23	i.MX25	i.MX28
Security hardware	DCP: • AES • Hashing	RTICv3 SCCv3 DRYICE RNGB	DCP: • AES • Hashing
One-time programmable storage	1-Kbit OCOTP ROM	IIM	1280-bit OCOTP ROM
Secure RAM	N/A	2 Kbyte	N/A
Secure JTAG	N/A	Yes	N/A
Secure Boot	128-bit AES hardware decryption	HAB with SHA-256	128-bit AES hardware decryption HAB with SHA-256

4.1 Security Hardware

The security hardware features of the i.MX23, i.MX25, and i.MX28 processors are described in the following sections.

4.1.1 DCP

The i.MX23 and i.MX28 have a DCP module that includes an AES block for general encryption and a hashing block for security functions. The AES block implements a 128-bit key/data encryption/decryption block as defined by the National Institute of Standards and Technology (NIST) as US FIPS PUB 197. For more information, see http://csrc.nist.gov/publications/PubsFIPS.html.

The DCP implements four SRAM based keys that can be used by the software to securely store the keys on a temporary basis. Keys are written using the programmed I/O (PIO) interface by specifying a key index. This key index specifies the key that should be loaded, and a subword pointer which indicates the word that should be written within the key. After a subword is written, the subword pointer is automatically incremented so that the higher order words of the key can be programmed without rewriting the key index. The keys written to the storage are not readable.

After a system reset, the OTP controller reads the e-fuse devices, provides the OTP key information over a parallel 128-bit interface and captures the key into the key RAM.

The DCP supports two forms of encryption:

- Electronic Code Book (ECB) mode—this is the basic mode where the output is a function of the key and plain text.
- Cipher Block Chaining (CBC) mode—this mode can be implemented around ECB to provide additional security. CBC takes the previously encrypted data and logically XORs it with the next incoming plain text before performing the encryption. During decryption, the process is reversed

and previously encrypted data is XORed with the decrypted ECB data and the plain text is retrieved.

The hashing module on the i.MX23 and i.MX28 DCP implements the SHA-1 hashing algorithm and the modified CRC-32 checksum algorithm. In addition to the SHA-1 hashing algorithm, the i.MX28 also implements the SHA-256 hashing algorithm. These algorithms produce a signature for a block of data that can be used to determine if the data is intact.

The CRC-32 algorithm implements a 32-bit CRC algorithm similar to the one used by the Ethernet and other protocols. The SHA-1 block implements a 160-bit hashing algorithm that operates on 512-bit (64-byte) blocks, defined by US FIPS PUB 180-1. The SHA-256 block implements a 256-bit hashing that operates on 512-bit (64-byte) blocks, defined by US FIPS PUB 180-2 (For more information, see http://csrc.nist.gov/publications/PubsFIPS.html). The module can be used to generate a unique signature for a block of data to validate the integrity of the data by comparing the resulting digest with the original digest.

4.1.2 RNGB

The i.MX25 contains a true hardware based RNGB. RNGB can be used for generating true random numbers for security keys and random challenges for software applications. Unlike the software driven pseudo random number generators, the hardware RNGB is not predictable and therefore, less vulnerable to prediction attacks.

4.1.3 SCCv3

The i.MX25 contains SSCv3 that provides 2 Kbyte of secure storage for sensitive information on both on-chip RAM and off-chip non-volatile memory. When used with the on-chip memory, the data is stored in RAM, which can be cleared (if required) to prevent unauthorized access. When used with the off-chip memory, the data is stored in encrypted form using an encryption key that is unique to each device and is accessible only to the Secure RAM module.

4.1.4 DryIce

The i.MX25 has a DryIce module that provides volatile storage of encryptions keys with robust tamper detection and secure key erase for POS terminals. The DryIce module also provides a trusted time source for the Digital Rights Management (DRM) schemes. The trusted time source consists of a 47-bit secure time counter that uses a 32.768 kHz clock source and a 32-bit monotonic counter. The DryIce is powered by the SoC power supply and the backup power source to maintain the secure counter and key storage in the event of power loss.

4.1.5 RTICv3

The i.MX25 contains RTICv3 and HASH accelerator that includes SHA-1 and SHA-256 message authentication to ensure the integrity of the peripheral memory contents. The RTICv3 is used to assist the boot authentication process by verifying the memory contents during the system boot. The RTICv3 can also verify the memory contents during the run-time execution.

4.2 Secure Boot

The encrypted boot and HAB features are described in the following sections.

4.2.1 Encrypted Boot

The i.MX23 and i.MX28 support encrypted boot with the secure bootloader in the ROM and DCP. At the reset, the ARM core starts the operation on the on-chip ROM instead of directly performing the operation on the user code. The boot mode is sampled from the boot pins on the ROM startup, and then the ROM loader takes the control. The ROM loader first calls the initialization function for the selected boot driver, which initializes the corresponding hardware port and external device. The loader then requests the boot image data from the driver.

The encrypted boot images are encrypted using a randomly selected session key by elftosb application. The key is symmetric and based on the AES-128 algorithm. The session key is encrypted by the OTP key and determined by the ROM during the authentication process. The bootloader authenticates and decrypts the boot image on reset. Based on the Cipher Block Chaining Message Authentication Code (CBC-MAC) signature calculated using the DCP and OTP key, a proprietary authentication scheme (not HAB) is used by the bootloader to authenticate the boot images. Only authenticated images are booted by the bootloader and loaded into the SDRAM.

4.2.2 HAB

HAB ensures trusted execution of the firmware by validating the code image stored in the external memory originated from a trusted authority. It also verifies if the code is in the original form. The HAB uses digital signatures to validate the external code images, and therefore establishes the security level of the system.

The digital signatures are created by encrypting the hash values of the code blocks with a RSA private key crypto system. The signature is then added to the code and stored in the Flash. Verification by the HAB uses a public key stored in the on-chip non-volatile memory. The private key is not stored in the end device. The signature extracted from the code block and public key is used to decrypt it into the original hash value. A new hash value of the code block is recalculated and compared with the decrypted hash value for verification.

The secure boot of the i.MX25 shown in Figure 2 is supported by HAB3 with SHA-256. The HAB component of ROM protects against potential threat from attackers by modifying the areas of code or data in programmable memory. The HAB also prevents attempts to gain access to unavailable features.

Figure 2 shows the secure boot of the i.MX25 processor supported by HAB3 with SHA-256.

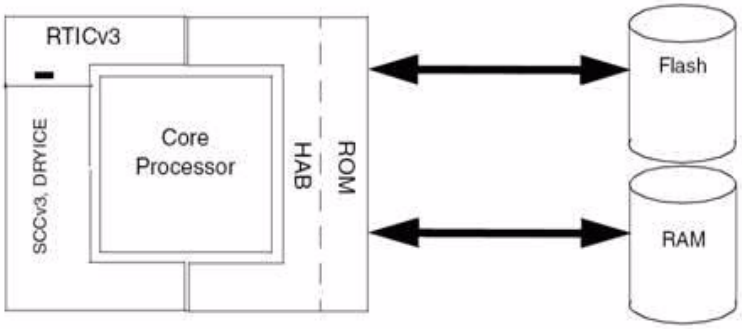


Figure 2. i.MX25 Secure Boot Components

The i.MX28 supports HAB4. On the i.MX28, the ROM loader loads the boot image into memory and calls the HAB authenticate image function to verify the image. The boot image is not executed unless the image authentication is successful. The public key is stored in the CRYPTO_KEY_OTP fuse bits on OCOTP. Encryption is turned ON/OFF by the ENABLE_UNENCRYPTED_BOOT fuse (unencrypted image is booted if the fuse is blown). Similarly, the HAB can be turned ON/OFF by the HAB_DISABLE fuse (HAB is disabled if the fuse is blown). The HAB_CONFIG fuse controls the HAB security type. Users have control over the HAB super root key hash through the HW_OTP_SRK fuses, which are used to compare the DCP SHA-256 generated super root key (public key) hash from the boot image. The Boot images are created by elftosb application, which handles both encryption and HAB signature binding. In addition, the HAB boot can be combined with the encrypted boot on the i.MX28.

5 External Memory and Storage

The i.MX23, i.MX25, and i.MX28 can interface efficiently with several external memories and storage devices such as Flash memory and Secure Digital (SD). Table 4 shows a comparison of the external memory and storage features of the i.MX23, i.MX25, and i.MX28.

Table 4. Comparison of External Memory and Storage

Feature	i.MX23	i.MX25	i.MX28
Memory and storage hardware interface	EMI GPMI • NAND Flash SSP	EMI • M3IF • ESDRAMC • NFC • WEIM ATA eSDHC	EMI GPMI • NAND Flash SSP
SDRAM	2.5 V DDR1 1.8 V mDDR	3.3 V SDRAM 1.8 V DDR2 1.8 V mDDR	1.8 V DDR2 1.8 V mDDR 1.5 V LP-DDR2
NAND Flash	Four 8-bit/16-bit NAND SLC/MLC NAND 8-bit Reed-Solomon ECC 20-bit BCH ECC	Four 8-bit/16-bit NAND SLC/MLC NAND 8-bit Reed Solomon ECC Internal RAM Buffer	Eight 8-bit/16-bit NAND SLC/MLC NAND 20-bit BCH ECC

Table 4. Comparison of External Memory and Storage (continued)

Feature	i.MX23	i.MX25	i.MX28
NOR Flash	N/A	Yes	N/A
ATA	N/A	UDMA-5	N/A
SD/MMC	eMMC 4.2, eMMC 4.3 (limited)	eMMC 4.3	eMMC 4.3, eMMC 4.4

5.1 i.MX23 Memory Interfaces

The i.MX23 supports off-chip DRAM storage through the EMI controller. The EMI supports 2.5 V DDR1 and 1.8 V mDDR.

The EMI consists of two major components:

- DRAM controller
- Delay Compensation Circuitry (DCC)

The DRAM controller supports up to two external chip-selects and a maximum of 128 Mbytes of DRAM storage. The 128-pin LQFP has one chip select pin and supports a maximum of 64 Mbytes of DRAM. The 169-pin BGA has two chip select pins and supports a maximum of 128 Mbytes of DRAM. The programmable registers within the DRAM controller allow flexibility for device timings, low-power operation, and performance tuning.

The i.MX23 GPMI is a flexible interface that supports up to four NAND Flash devices. The GPMI has configurable address and command behavior, and it provides support for future devices.

The GPMI has the following features, which efficiently supports NAND Flash:

- Individual chip select and ready/busy pins for four NAND Flashes
- Individual state machine and Direct Memory Access (DMA) channel for each chip select
- Special command modes work with the DMA controller to perform all normal NAND Flash functions without the intervention of the CPU
- Configurable timing based on a dedicated clock that allows optimal balance of high NAND Flash performance and low system power

The i.MX23 has hardware ECC accelerators to provide forward error correction to interface with the MLC NAND Flashes. The ECC engine on the i.MX23 implements Bose Ray-Choudhury Hocquenghem (BCH-ECC) engine and provides up to 20 bits of correction. For backward compatibility, Reed-Solomon (RS-ECC8) engine is used, which provides 4 or 8 bits of correction. Both engines are tightly coupled to the GPMI and are for mutually exclusive use, with separate programming modules and DMA structures.

External media like SD or MMC can be supported by the i.MX23 SSP. eMMC version 4.2 and 4.3 is supported. However, the ROM cannot boot an eMMC 4.3 device with the CSD_STRUCTURE version in the EXT_CSD register. To support SD, SDIO, MMC, and high speed (4-bit and 8-bit) MMC cards, SSP is configured in the SD/SDIO/MMC mode. In this mode, the SSP supports simultaneous command and data transfers. Commands are sent to the card and responses are returned to the host on the CMD line. Register data is sent as a command response. Block data read from or written to the card Flash is transferred on the DAT line(s). The SSP also supports the SDIO Interrupt Request (IRQ).

5.2 i.MX25 Memory Interfaces

The i.MX25 EMI handles the external memory access. The EMI manages the following external memory controllers to support different memory devices:

- M3IF
- ESDRAM/LP-DDR memory controller (ESDRAMC/mDDR controller)
- NFC
- SRAM/Pseudo SRAM (PSRAM)/FLASH memory controller (WEIM)

The M3IF supports multiple requests up to eight masters through the input port interfaces. The M3IF supports memory snooping that monitors a region (from 2 Kbytes to 16 Mbytes) in the external memory for the write access. Some versions of M3IF also support memory watermark protection up to eight chip selects for hardware preselected masters.

The ESDRAMC/mDDR controller provides interface and control for synchronous Single Data Rate (SDR), LP-DDR, and DDR1 devices. It also provides support for 4-bank DDR2 devices and can be connected to 8-bank DDR2 devices (though it can access only 4 banks without the On Device Termination (ODT) control signal). The controller supports 64-Mbit, 128-Mbit, 256-Mbit, 512-Mbit, and 1-Gbit (4 banks) synchronous DRAM with two independent chip selects and up to 128-Mbyte addressable memory per chip select. Only 16-bit SDRAM is supported by the controller. The controller has a PC133 compliant interface that supports SDR at 133 MHz and DDR at 266 MHz, with JEDEC standard pin-out and operations (For more information, see http://www.jedec.org/). Consecutive memory accesses are optimized through memory command anticipation or latency hiding. The controller also has a built-in auto-refresh timer and state machine with self-refresh entry and exit support to keep the data in SDRAM valid during the system reset and low-power modes.

The NFC provides a glueless interface to both 8-bit and 16-bit NAND Flash with page sizes of 512 bytes, 2 Kbytes, or 4 Kbytes. The NFC has an internal RAM buffer (4 Kbytes + 512 bytes), which can be configured as a boot RAM, or operated as a buffer during normal operation. The NFC supports both SLC and MLC NAND Flashes. MLC NAND Flash uses two Reed Solomon RS (511,503) ECCs, which corrects 4/8 error bits in 528/538 bytes (512 bytes main + 16/26 bytes spare). The i.MX25 includes an internal bootcode loader to provide advanced data protection during power-up when booted from the external NAND Flash.

The WEIM interfaces with the external devices and includes generation of chip selects, clocks, and control for the external peripherals and memory. The WEIM provides asynchronous and synchronous access to 16-bit or 32-bit devices with SRAM-like interface. The WEIM has six chip selects for the external devices with selectable protection for each chip select. The WEIM includes a programmable data port size wait-state generator for each chip select. The WEIM supports asynchronous accesses with programmable setup and hold time for control signals. For synchronous accesses, the WEIM supports burst read mode for AMD, Intel, and Micron burst Flash memory, and burst write mode for PSRAM (CellularRAM™ from Micron, Infineon, Cypress). The WEIM also supports multiplexed address/data bus operation, external cycle termination/postpone with DTACK signal, and big/little-endian modes operation per access.

5.3 i.MX28 Memory Interfaces

The i.MX28 supports off-chip DRAM storage through the EMI controller. The i.MX28 EMI supports 1.8 V mobile DDR (LP-DDR), standard 1.8 V DDR2, and 1.5 V Low Voltage DDR2 (LV-DDR2) up to 200 MHz clock rate.

The i.MX28 EMI consists of the following three major components:

- AXI/AHB bus interface and multi-port arbiter
- DRAM control logic
- DRAM PHY

The i.MX28 EMI has integrated ODT for DDR2 applications. The DRAM controller supports up to two chip selects and a maximum of 1024 Mbytes DRAM storage.

The i.MX28 GPMI is a flexible interface that supports up to eight NAND Flash devices with configurable address and command behavior, providing support for future devices.

The GPMI has the following features to efficiently support the NAND Flash:

- Individual chip select and ready/busy pins for eight NAND Flashes
- Individual state machine and DMA channel for each chip select
- Special command modes work with the DMA controller to perform all normal NAND Flash functions without CPU intervention
- Configurable timing based on a dedicated clock that allows optimal balance of high NAND Flash performance and low system power

The GPMI provides an interface to the Bose Ray-Choudhury Hocquenghem (BCH-ECC) module to reduce the SOC bus traffic and software involvement. The BCH encoder and decoder module corrects 2 to 20 single bit errors within a block of data not larger than 900 bytes (typically 512 bytes) in applications such as protecting data and resources store on the MLC NAND Flash.

External media such as SD or MMC can be supported by the i.MX28 SSP. There are four SSPs on the i.MX28. To support SD, SDIO, MMC, and high speed (4-bit and 8-bit) MMC cards, SSP is configured in the SD/SDIO/MMC mode. SSP is fully compliant with the SDIO Rev. 2.0 and eMMC 4.4 standard. It has the capability of SDR and DDR operations, power-on and alternate boot operations. In the SSP mode, SSP supports simultaneous command and data transfers. Commands are sent to the card and responses are returned to the host on the CMD line. Register data is sent as a command response. Block data read from or written to the card Flash is transferred on the DAT line(s). SSP also supports SDIO.

6 Audio Features

The i.MX23 includes the following digital and analog audio interfaces:

- Two SAIFs
- Integrated high quality audio ADC and Digital to Analog Converter (DAC)
- SPDIF transmitter
- Several analog audio input/output options

The i.MX25 includes the following digital audio interfaces:

- ESAI
- Synchronous Serial Audio Interface (SSI/Integrated Interchip Sound (I^2S))
- Digital Audio Multiplexer (AUDMUX) for selecting input sources

The i.MX28 includes the following digital audio interfaces:

- Two SAIFs
- SPDIF transmitter

Table 5 shows a comparison of the audio features of the i.MX23, i.MX25, and i.MX28.

Table 5. Comparison of Audio Features

Feature	i.MX23	i.MX25	i.MX28
Serial audio interface	Dual SAIF half-duplex	ESAI full-duplex	Dual SAIF half-duplex
SPDIF digital audio out	Yes	N/A	Yes
Digital audio multiplexer	N/A	Yes	N/A
Analog audio outputs	Stereo headphone amplifier Mono speaker amplifier	N/A	N/A
Analog audio inputs	Mono microphone input Two stereo line inputs	N/A	N/A

6.1 i.MX23 and i.MX28 SAIF

The i.MX23 and i.MX28 includes two SAIF modules. But for the i.MX23, the SAIF module is only available on the 169-pin Ball Grid Array (BGA) package.

Figure 3 shows the block diagram of SAIF.

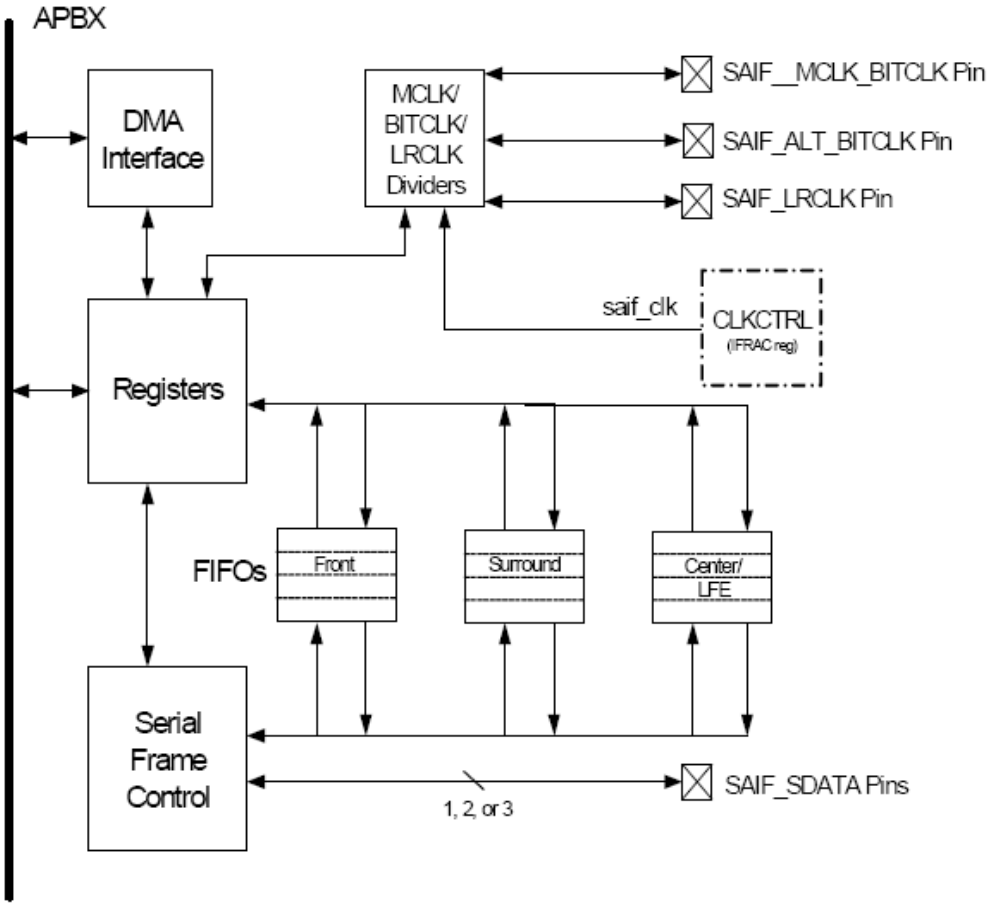


Figure 3. SAIF Block Diagram

The SAIF provides the following functions:

- 3-wire, 4-wire, or 5-wire serial interface to the common analog codes
- Half-duplex operations
- 16-bit to 24-bit serial stereo digital audio Pulse Code Modulation (PCM) play/record
- Two, four, or six channels supported—three stereo pairs (mono supported in two-channel mode)
- Generic frame control supports I^2S, left-justified and right-justified frame formats, and other nonstandard variants of these formats
- Master and slave BITCLK and LRCLK modes (clocks driven to codec or received from codec) and an optional master MCLK mode
- Sample rates from 8 kHz to 192 kHz using a high resolution fractional divider driven by Phase Locked Loop (PLL)
- Programmable over-sample rate for MCLK output (32x, 48x, 64x, 96x, 128x, 192x, 256x, 384x, and 512x) supports codecs is observed in systems with both audio and video
- Four-entry FIFOs (per sample pair) buffer, either two-channel sample pairs (17–24 bit PCM) or four-packed-channel sample pairs (16-bit PCM)

- Samples transferred to/from the FIFO through the APBX DMA interface, FIFO service interrupt, or software polling

The SAIF port is a half-duplex port. It can either transmit or receive PCM audio, but not simultaneously. One sample data is communicated at a time serially, alternating between the left and right samples. One to three serial data lines (SDATA0-SDATA2) can be used to transmit either two (stereo/mono), four (stereo/surround), or six (stereo/surround/center/LFE) channels of digital PCM audio data. Sample boundaries are delineated by a left/right clock (LRCLK) pin. The individual bits within each sample are delineated by a bit clock (BITCLK) pin.

The LRCLK can be programmed to toggle every 16, 24, or 32 BITCLK transition. As the data ranges from 16 to 24 bits, serial data within each LRCLK period can either fully occupy the LRCLK cycle or cause the LRCLK period to contain BITCLK cycles in which data is not communicated. Therefore, the following three types of sample frame formats can be programmed:

- I^2S
- Left-justified
- Right-justified

Several programming options exist to alter these basic frame types, such as the LRCLK signal polarity, BITCLK edge selection to drive/sample serial data, and sample justification/delay within an LRCLK period.

For codecs that do not contain their own PLL or for applications which do not include a crystal oscillator to drive the codec, SAIF can provide a master clock (MCLK) reference that can be configured from 512x to 32x of the audio data sample rate. This master clock is used by the internal logic of the off-chip codec to synchronize the BITCLK/LRCLK/SDATA inputs for DAC operation.

The digital PCM audio sample rate is determined by programming a fractional divider within the clock controller module.

The i.MX23 has two SAIF modules instantiated on chip. However, due to the pin multiplexing constraints, only one set of clock pins is provided for both ports. Therefore, only one of the two SAIFs can act as a master or drive the clock pins at a time. The other SAIF acts as a slave to the master. This implies that both SAIFs must operate at the same sample rate.

The following are the valid configurations for SAIF1 and SAIF2 on the i.MX23:

- One SAIF is in the TX mode (is default clock master) while the other SAIF is in the RX slave mode and is internally controlled by the TX SAIF's BITCLK and LRCLK
- One SAIF is in the RX master mode while the other SAIF is in the RX slave mode and is internally controlled by the RX master SAIF's BITCLK and LRCLK
- Both the SAIFs are in the RX slave mode with BITCLK and LRCLK controlled by the off-chip codec
- Only one SAIF can be used (any configuration)

The i.MX28 also has two SAIF modules instantiated on-chip. Each SAIF has a set of clock pins and can operate in master mode simultaneously if they are connected to different off-chip codecs. The SAIFs can operate at different sample rate. Also, one of the two SAIFs can act as a master or drive the clock pins. The

other SAIF in slave mode receives clocking from the master SAIF. Both SAIFs must operate at the same sample rate.

The following are the valid configurations for SAIF1 and SAIF2 on the i.MX28:

- One SAIF is in the TX mode (is default clock master) while the other SAIF is in the RX slave mode and is internally controlled by the TX SAIF's BITCLK and LRCLK
- One SAIF is in the RX master mode while the other SAIF is in the RX slave mode and is internally controlled by the RX master SAIF's BITCLK and LRCLK
- Both the SAIFs are in the RX slave mode with BITCLK and LRCLK controlled by the off-chip codec
- Both the SAIFs are in the master mode driving their BITCLK and LRCLK
- Only one SAIF can be used (any configuration)

6.2 i.MX23 and i.MX28 SPDIF Transmitter

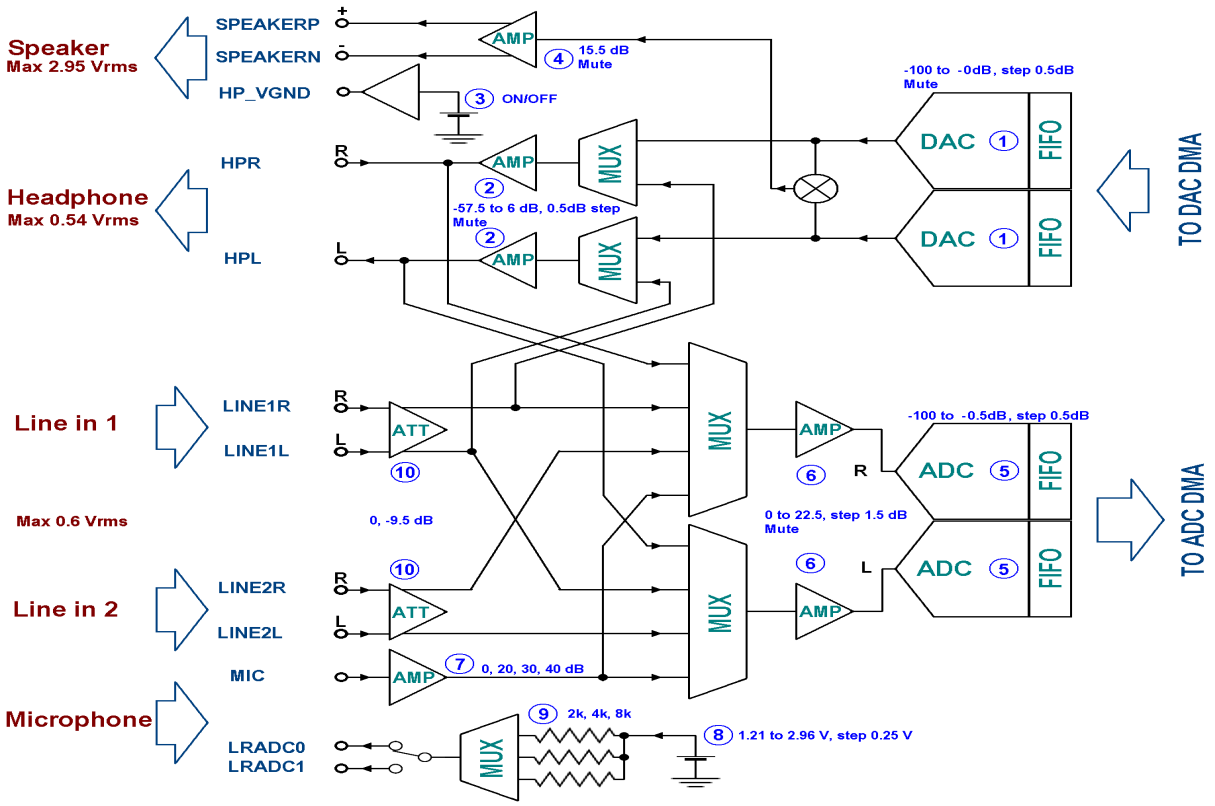
Both the i.MX23 and i.MX28 includes a SPDIF transmitter module that transmits data according to the SPDIF digital audio interface standard (IEC-60958). For more information, see http://www.aes.org/. Data samples are transmitted as blocks of 192 frames, each frame consisting of two 32-bit subframes. A 32-bit subframe is composed of a 4-bit preamble, 24-bit data payload (such as a left or right channel PCM sample), and 4-bit status field. The status fields are encoded according to the IEC-60958 consumer specification, reflecting the contents of the HW_SPDIF_FRAMECTRL and HW_SPDIF_CTRL registers. For information on programming these fields, refer to the IEC-60958 specification.

The subframe is transmitted serially (LSB first) using a biphase-mark channel coding scheme. This encoding allows a SPDIF receiver to recover the embedded clock signal. The subframe information can be changed on-the-fly, but it is not reflected in the serial stream until the current frame is transmitted. This ensures consistency of the frame and the generated parity appended to that frame.

6.3 i.MX23 Analog Audio

The i.MX23 contains an integrated, high quality mixed signal audio subsystem, including high quality sigma-delta DAC with 97 dB Signal-to-Noise Ratio (SNR) and ADC with 87 dB SNR. The DAC is used for audio decoder/player product application. The ADC is used for voice recording and MP3 encoding applications.

Figure 4 shows the i.MX23 mixed signal audio subsystem.



Output

1 DAC digital domain volume control—HW_AUDIOOUT_DACVOLUME (-100 to 0 dB, 0.5 dB step with mute function)

2 Headphone AMP volume control—HW_AUDIOOUT_HPVOL (-57.5 to 6 dB, 0.5 dB step with mute function)

3 Direct drive headphone ground —HW_AUDIOOUT_PWDN (ON/OFF)

4 Speaker AMP—HW_AUDIOOUT_SPEAKERCTRL (15.5 dB or Mute)

Input

5 ADC digital domain volume control—HW_AUDIOIN_ADCVOLUME (0 to -100 dB, 0.5 dB step)

6 ADC input gain control—HW_AUDIOIN_ADCVOL (0 to 22.5 dB, 1.5 dB step)

7 Microphone AMP gain control—HW_AUDIOIN_MICGAIN (0 dB, 20dB, 30dB, and 40 dB)

8 Microphone bias voltage—HW_AUDIOOUT_MICLINE_MIC_BIAS (1.21 to 2.96 V, 0.25 V step)

9 Mic bias resistor—HW_AUDIOOUT_MICLINE_MIC_RESISTOR (2 kΩ, 4 kΩ, 8 kΩ)

10 Line-in attenuator—HW_AUDION_MICLINE_DIVIDE_LINE1, HW_AUDION_MICLINE_DIVIDE_LINE2 (works with external resistor) (0 dB, -9.5 dB)

Figure 4. i.MX23 Mixed Signal Audio Subsystem

The i.MX23 includes a low noise headphone driver that allows the i.MX23 to directly drive the low impedance (16 Ω) headphones. The direct drive mode or capless mode eliminates the requirement for expensive DC blocking capacitors in the headphone circuit. The headphone power amplifier detects the headphone shorts and report them through the interrupt collector. A digitally programmable master volume control allows the user to control the headphone volume. Use of the headphone amplifier volume control is recommended as the digital control can reduce SNR performance. Unwanted clicks and pops are eliminated by zero-crossing updates in the volume/mute circuits and headphone driver startup and shutdown circuits.

The microphone circuit has a mono-to-stereo programmable gain pre-amp and an optional microphone bias generator. In addition, there is a stereo line input for external audio sources. A class A-B mono speaker amplifier is also integrated. This speaker must be powered from a 4.2 V source (such as battery) that provides high current. The speaker amplifier with a 4.2 V supply and a 4 Ω speaker load supports only bridge-tied configuration and provides an output up to 1.75 W_{rms}.

6.4 i.MX25 ESAI

The i.MX25 includes an ESAI which provides a full-duplex serial port for communication with several devices, including industry standard codecs, SPDIF transceivers, and other DSPs. ESAI consists of independent transmitter and receiver sections, each with its own clock generators.

ESAI is synchronous as all serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. It supports the following modes of operation:

- Normal mode—used to transfer data at a periodic rate (one word per period).
- Network mode—intended for periodic data transfer (similar to the normal mode of operation). However, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks.
- On-demand mode—intended for nonperiodic data transfer. When the data is available, it is transferred serially at high speed.

Figure 5 shows the i.MX25 ESAI block diagram.

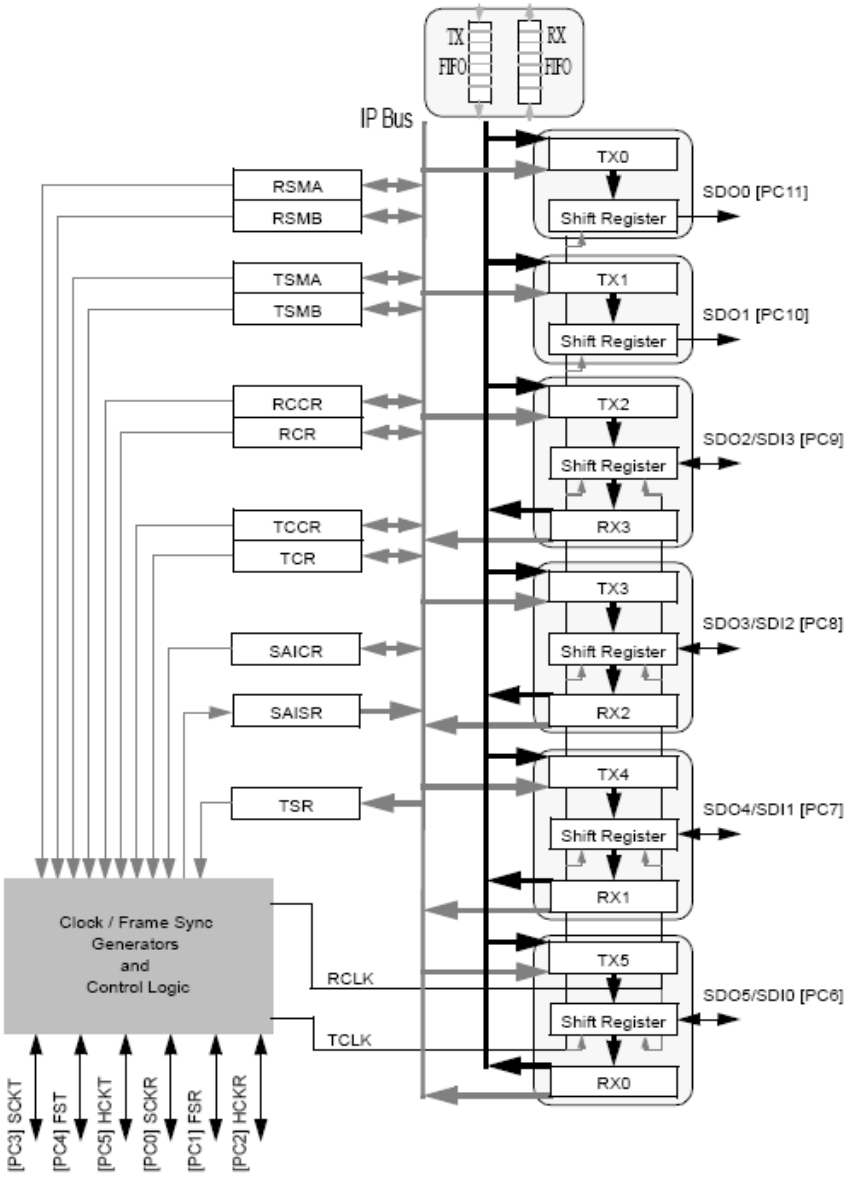


Figure 5. i.MX25 ESAI Block Diagram

ESAI has the following features:

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in master or slave mode
- Maximum of six transmitters and four receivers with SDO2/SDI3, SDO3/SDI2, SDO4/SDI1, and SDO5/SDI0 pins are shared by transmitters 2 to 5 and receivers 0 to 3. SDO0 and SDO1 pins are used by transmitters 0 and 1 respectively
- Programmable data interface modes supported are I^2S, LSB-aligned, and MSB-aligned
- Programmable word length (8, 12, 16, 20, or 24 bits)

- Flexible selection between the system clock or the external oscillator as input clock source, programmable internal clock divider, and frame sync generation
- AC97 support
- Time Slot Mask registers for reduced CPU overhead (for the Transmit and Receive operations)
- 128-word Transmit and Receive FIFO

6.5 i.MX25 Digital AUDMUX

The i.MX25 includes a digital AUDMUX which is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs).

The AUDMUX has two sets of interfaces:

- Internal ports to the on-chip peripherals
- External ports to the off-chip audio devices

Data is routed by configuring the appropriate internal and external ports.

7 Display and Video

The i.MX23, i.MX25, and i.MX28 provide an integrated LCD controller to easily interface with an external LCD module. They also provide advanced display processing features. The i.MX23 also includes TV-Out functionality.

Table 6 shows a comparison of the display and video features of the i.MX23, i.MX25, and i.MX28.

Table 6. Comparison of Display and Video Features

Feature	i.MX23	i.MX25	i.MX28
LCDIF	Yes	Yes	Yes
Resolution	Up to 640 × 480	Up to 800 × 600	Up to 800 × 480
Bit/Pixel	8, 16, 18, 24 (color)	1, 2, 4 (mono) 4, 8, 12, 16, 18, 24 (color)	8, 16, 18, 24 (color)
TV-Out	Yes	N/A	N/A
Display processing	PXP 8 Overlays Color key/Alpha blend Color space conversion and Scaling Rotation	1 Overlay (Graphic window) Color Key/Alpha blend Panning	PXP 8 Overlays Color Key/Alpha blend Color Space Conversion and Scaling Rotation
CSI	N/A	Yes	N/A
Linear image scanner interface	N/A	N/A	HSADC

7.1 i.MX23 Display Processing

The i.MX23 has significantly advanced display processing and output capabilities. The display processing and output have the following four distinct modules:

- Display Controller (LCDIF)
- PXP
- PAL/NTSC TV encoder
- 10-bit Video DAC for analog composite output

These features allow post video decode pixel processing to be handled in the hardware with minimal CPU intervention. The i.MX23 also supports multiple pixel formats and display configurations.

Figure 6 shows the i.MX23 display processing subsystem.

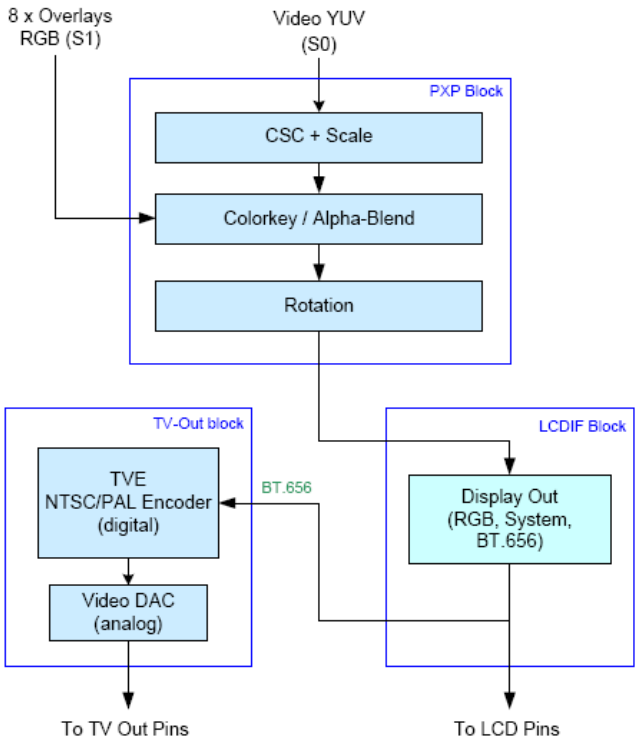


Figure 6. i.MX23 Display Processing Subsystem

The i.MX23 Display Controller (LCDIF) supports the following features:

- 24-bit full color parallel RGB (DOTCLK) mode to drive up to VGA (640 × 480) full color display at refresh rates up to 60 Hz
- Full 24-bit system mode (8080/6080/VSYNC/WSYNC). The read mode is not supported
- 8-bpp, 16-bpp, 18-bpp, or 24-bpp color display panels
- ITU-R BT.656 compliant D1 digital video output mode with on-the-fly RGB to YCbCr color space conversion. This output also feeds the integrated TV encoder

- Wide variety of input and output formats allowing conversion between input and output (such as RGB565 input to RGB888 output). Also provides the packed pixel format support

The i.MX23 PXP performs the necessary post display frame pre-processing in hardware with minimal CPU and memory overhead. This allows the CPU to have maximum processing bandwidth for video-decode operation. For example, PXP can be is used to perform alpha blending of graphic or video buffers with graphics data before sending to an LCD display or TV encoder. PXP also supports image rotation for handheld devices that require portrait and landscape image support.

Figure 7 shows the i.MX23 pixel pipeline block diagram.

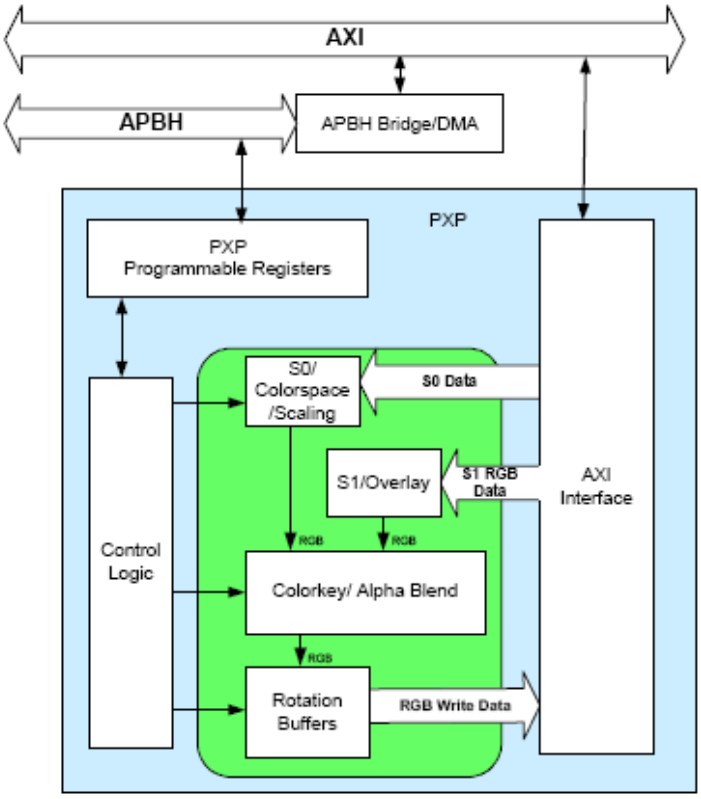


Figure 7. i.MX23 Pixel Pipeline Block Diagram

PXP is organized to have a background image (S0) and one or more overlay images that can be blended with the background. Each overlay image must be a multiple of eight pixels in both height and width. The offset of the overlay in the background image must be a multiple of eight pixels. As PXP processes the data, it reads each 8×8 block from the background image and finds the highest priority (lowest numbered) overlay located at that block coordinates. PXP then fetches the overlay and performs the alpha blending and color key operations on the two blocks. The resulting 8×8 pixel block is then written to the corresponding block in the output buffer.

For the S0 plane, PXP supports RGB images (unscaled) or color space conversion (YUV-RGB) and scaling of YUV images. The S1 plane consists of up to eight overlay regions consisting of 16-bit or 32-bit RGB data. Then the S0 and S1 planes are combined by alpha blending, color key substitution, or raster operations (ROPs) to form the output image. Finally, the resulting image is rotated clockwise in 90º

increments or flipped horizontally or vertically. PXP supports letter boxing and interlacing of progressive content.

The PAL/NTSC TV encoder is a part of the i.MX23 integrated TV-Out functionality. The encoder takes the input directly from the LCDIF without intermediate memory access. To utilize the TV-Out path, the LCDIF must be configured to output the ITU-R BT.656/BT.601 D1 digital video stream mode. This stream is synchronized to the internal 108 MHz clock of the TV encoder. Now, the TV encoder encodes the stream into a format suitable for the Video Digital-to-Analog Converter (VDAC). Before being sent to the VDAC, the output of the TV encoder is passed through a pixel interpolating filter, which decreases the requirements of the off-chip video filtering.

The i.MX23 includes a fully integrated, low-power, 10-bit VDAC, which directly takes the TV encoder output and generates an analog compliant, Composite Video Baseband Signal (CVBS). The i.MX23 also supports an optional source termination and automatic jack detection (through an interrupt) and allows the VDAC to automatically enable/disable.

7.1.1 i.MX25 LCD Controller (LCDC)

The i.MX25 includes a LCDC which provides the display data for external gray-scale or color LCD panel. The LCDC supports black and white, gray-scale, passive matrix color (passive color or Color Super Twist Nematic (CSTN)), and active matrix color (active color or TFT) LCD panels.

The LCDC provides the following features:

- Standard panel interface for common LCD drivers
- 1-bit, 2-bit, or 4-bit panel interface for monochrome panels and 4-bit, 8-bit, 12-bit, 16-bit, 18-bit, or 24-bit panel interface for color panels
- Hardware generated cursor with blink, color, and size programmability
- Logical operation between color hardware cursor and background
- Hardware panning (soft horizontal scrolling)
- Graphic window support for the viewfinder function in color display
- Graphic window color keying for the graphical hardware cursor
- 256 transparency levels for the alpha blending between the graphic window and background plane

Figure 8 shows the i.MX25 LCD controller block diagram.

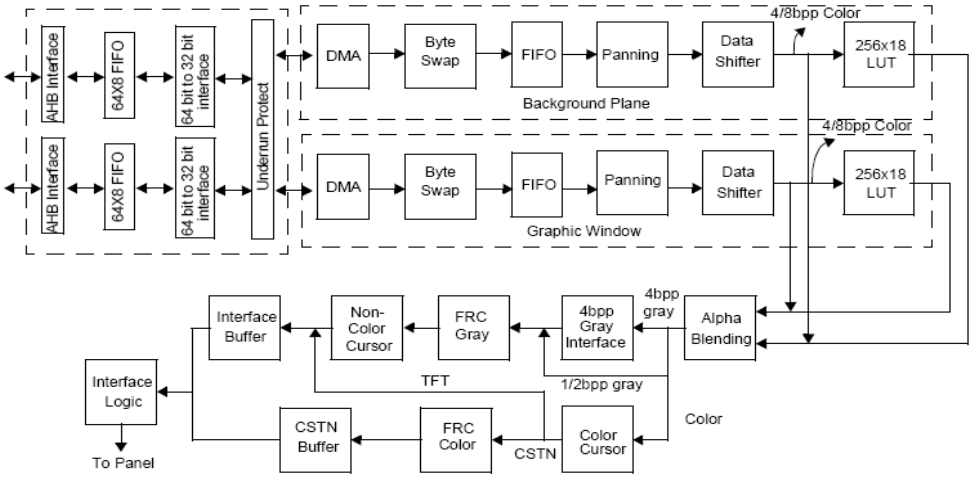


Figure 8. i.MX25 LCD Controller Block Diagram

A graphic window is supported in the LCD color panel screen for the viewfinder and graphic hardware cursor functions. The start address, width, and height of the graphic window are software programmable. The position of the graphic window is specified by the graphic window position register. The graphic window and background can be alpha blended with a constant alpha for the entire window, so that all pixels in the graphic window have the same transparency level (256 possible levels). In addition, one of the pixel colors can be chosen for color keying. The pixel color selected in the graphic window is made completely transparent.

7.2 i.MX25 Smart LCD Controller (SLCDC)

The i.MX25 contains a SLCDC module to transfer data from the display memory buffer to the external display device. The DMA transfers data transparently with minimal software intervention. In addition, the DMA Bus utilization is controllable and deterministic.

Figure 9 shows the i.MX25 SLCDC system diagram.

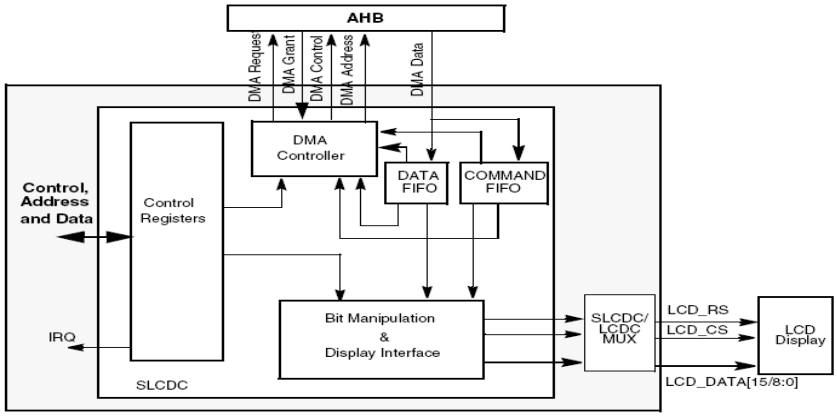


Figure 9. i.MX25 SLCDC System Diagram

As the displays become larger and colorful, the demand for the processor increases and more CPU power is required to render and manage the image. The role of the SLCDC is to reduce the CPU involvement in the data transfer from memory to the display device, so that the CPU can concentrate on image rendering. The DMA is used to optimize the data transfer. The embedded control information required by the display device is automatically read from a second buffer in the system memory and inserted into the data stream at the right time. Therefore, the role of CPU in the transfer is completely eliminated.

Several display sizes and types are used in different products that use SLCDC. The SLCDC module has the capability of directly interfacing with the selected display devices. Both serial and parallel interfaces are supported. The SLCDC module supports only the write operation to the display controller and does not support the read operation from the display controller.

7.3 i.MX25 CSI

The i.MX25 includes a CSI which allows the device to connect directly to the external CMOS image sensors. The interface is configurable to support common CMOS sensors. The CSI supports the following sensors:

- Dumb sensors that support only traditional sensor timing (Vertical SYNC and Horizontal SYNC) and output only Bayer and statistics data
- Smart sensors that support CCIR656 video decoder formats and perform additional image processing

The CSI also provides a configurable master clock frequency output to the sensor and supports statistic data generation for Auto Exposure (AE) and AWB control of the camera (only for Bayer data and 8-bit/pixel format).

7.4 i.MX28 Display Processing

The i.MX28 contains a powerful, flexible display, and capture subsystem that consists of the following modules:

- Display Controller (LCDIF)
- PXP

The i.MX28 Display Controller (LCDIF) supports the following features:

- 24-bit full color parallel RGB (DOTCLK) mode to drive up to WVGA (800 × 480) full color display at refresh rates up to 60 Hz. High robustness is guaranteed by the 512-pixel FIFO
- Full 24-bit system mode (8080/6080/VSYNC/WSYNC)
- 8-bpp, 16-bpp, 18-bpp, or 24-bpp color display panels
- ITU-R BT.656 compliant D1 digital video output mode with on-the-fly RGB to YCbCr color space conversion. This output is suitable for driving the external TV encoder
- Wide variety of input and output formats that allow the conversion between input and output (such as RGB565 input to RGB888 output). It supports packed pixel formats

The i.MX28 PXP performs the required post display frame pre-processing in hardware with minimal CPU overhead. PXP can operate either in the 8 × 8 or 16 × 16 block mode. When using 32-bit memories with EMI, 16 × 16 is recommended for efficient memory access.

The background image is read from an external memory (single-plane YUV, dual-plane Y/UV, and three-plane Y/U/V inter-leaved source buffer formats are supported) into the internal buffers. These buffers are fed into a color space converter (for example, YUV to RGB) followed by the scaling engine, which utilizes an advanced bilinear weighted scaling algorithm. The scaling operation is defined in terms of the output image. The output of the scaler is fed into another internal buffer, S0. If the background image is already available in the RGB color space, it is assumed to be scaled appropriately for the required output format and can be read directly into the internal S0 buffer. To maintain the efficient use of the external memory, only the relevant (visible) portion of the background image is fetched.

The scaled RGB image (in the internal S0 buffer) can be blended with up to eight programmable overlays. The coordinates of the overlays can be described again in terms of the resultant output image. Each overlay can either have a global programmable opacity or per-pixel resolution if constructed with the RGB color space. In addition, each overlay can have a relative priority level such that, when the output image is constructed, PXP only fetches the visible overlay in the block. The overlays are fetched into the internal S1 buffer. Alpha blending is performed on the S0 and S1 buffers to generate the blended output into the internal S3 buffer. Other operations such as BITBLT and color keying can also be performed at this stage.

The final stage of the PXP operation is rotator, which can perform flips and 90º, 180º, and 270º rotations. The rotator operates on the pixel blocks in the S3 buffer to maximize the external memory fetch efficiency. It writes the pixel blocks to the external memory in this final stage.

PXP supports scaling down up to 4:1 in the single pass mode. This is useful for scaling 720p decoded content to a QVGA display. PXP can also be used to further scale down images using a multi pass approach.

7.5 i.MX28 HSADC Controller

The i.MX28 contains a HSADC module designed to drive the linear image scanner sensor (for example, TOSHIBA TCD1304DG linear image scanner sensor). It also supports other general user cases which require to sample the analog source with a speed up to 2 mega samples per second (Msps). The HSADC module integrates a 12-bit ADC module. To improve the flexibility, the HSADC module can work with the PWM module to generate the driving signals for the external devices such as the linear image scanner sensor. The PWM can also generate the trigger signal, which is synchronous with the HSADC module to start the ADC conversion. An APBH-DMA channel is connected to the HSADC module to move the sample data from the asynchronous FIFO inside the HSADC module to the external memory.

8 Power Management

The i.MX23 and i.MX28 have an integrated DC-DC switched controller that allows the device to operate directly from Li-Ion batteries. The i.MX23, i.MX25, and i.MX28 provide advanced power management features, which make them suitable for low-power applications.

Table 7 shows a comparison of the power management features of the i.MX23, i.MX25, and i.MX28.

Table 7. Comparison of Power Management Features

Feature	i.MX23	i.MX25	i.MX28
Internal power supply	DC-DC switched converter Four linear regulators • 3.3 V • 1.2 V • 1.8 V • 2.5 V	N/A	DC-DC switched converter Four Linear regulators • 3.3 V • 1.2 V • 1.8 V • 1.5 V
Power management	AVC CLK_H auto-slow Clock gating Silicon speed sensors Multiple peripheral clock (domains)	DVFS Clock gating AWB	AVC CLK_H auto-slow Clock gating Silicon speed sensors Multiple peripheral clock (domains)
Low-power mode	Standby Deep-sleep	Wait Doze Stop Sleep	Standby Deep-sleep

8.1 i.MX23 Power Management

The i.MX23 contains a sophisticated PMU that includes the following:

- Integrated DC-DC converter
- Four linear regulators
- Regulated 4.2 V output

PMU can operate from a Li-Ion battery using the DC-DC converter or a 5 V supply using the linear regulators and can automatically switch between them without interrupting the operation. PMU includes circuits for battery and system voltage brownout detection, on-chip temperature, digital speed, and process monitoring.

The integrated PMU converter can be used to provide programmable power for the device and the entire application (up to five rails):

- VDDIO (nominal 3.3 V)—DC-DC or linear regulator from 5 V
- VDDD (nominal 1.2 V)—DC-DC or linear regulator from VDDA
- VDDA (nominal 1.8 V)—DC-DC or linear regulator from VDDIO
- VDDM (nominal 2.5 V)—linear regulator from VDDIO
- VDD4P2 (nominal 4.2 V)—when connected to a 5 V source, it can source DC-DC

The 4.2 V regulated output also allows for programmable current limits:

- Total load plus the battery charge current (5 V limit)
- Battery charge current
- Load current—for both on-chip and off-chip circuits

The 4.2 V circuit adjusts the distribution of current supply between the load and the battery charger depending on programmed current limits and load conditions. For example, when the battery is charged, and the 5 V current limit is exceeded, the 4.2 V regulator derives current from the battery charger circuit and diverts it to the load circuit.

The DC-DC converter can operate from the standard Li-ion battery up to 4.2 V. The converter uses the off-chip reactive components (L and C) and operates in the pulse-width or frequency-modulated mode depending on the load condition. The real-time clock includes an alarm function that can be used to trigger the DC-DC converter. The DC-DC converter then triggers the rest of the system.

PMU is designed to support AVC which can reduce system power consumption by half. AVC also allows the chip to operate at a higher peak CPU operating frequency than that of the typical voltage control systems. The DC-DC converters and the clock generator can be re-programmed on-the-fly to dynamically trade-off power and performance. All the major functional clock domains/branches have trunk level clock gating for the power management, to gate the clock domains OFF when the modules are not required for certain applications. This clock gating is instantiated using an ICG element from the standard cell library. Software must enable the clock domain that drives on-chip devices when trunk level clock gating is implemented. The i.MX23 also has multiple peripheral clock domains to control the clocks of individual peripherals to save power while optimizing the performance. The i.MX23 can be toggled into a deep-sleep mode, which reduces the CPU speed to minimum and shuts down all the peripherals.

The CLK_H domain on the i.MX23 can be programmed to any divided ratio with respect to the CLK_P domain, depending on the performance and power requirements. A dynamic clock frequency management controller monitors the system performance and scales the CLK_H frequency to meet performance needs. When the system is quiesced, the CLK_H frequency is automatically reduced to save power.

The i.MX23 integrates a silicon speed sensor to measure the performance characteristics of an individual die at its ambient temperature and process. The information given by the speed senor can be monitored by the system software to keep the operating voltage to minimum.

The i.MX23 supports the following low-power modes:

- Standby mode—the power consumption is minimized in this mode. The CPU is switched to the bypass mode (direct clocking from the crystal), interrupts are disabled (except for the wake up sources), DMA is disabled, RAM is switched to the bypass mode and self-refreshed, and the PLL is switched ON.
- Deep-sleep mode—the CPU and all the peripherals (including DC-DC) except the RTC are shut down. The i.MX23 consumes least power in this mode.

8.2 i.MX25 Power Management

The i.MX25 has the following voltage segments:

- Digital Logic—nominal voltage is 1.2 V
- DryIce—sourced from the internal power switch, powered from the core power supply or coin battery
- Analog—supplies the OSC24M, PLLs, USB PHY, Fuse box, and TSC

The two main active power savings technique applied to the i.MX25 are as follows:

- Clock gating—it includes two levels of clock gating—clock tree roots (in CRM) and clock tree leaf nodes (in the modules). This technique reduces the active power consumption by gating the clock across each module when the module is in the idle state.
- DVFS—it allows a simple software dynamic voltage frequency scaling. The frequency of the MCU clock domain and voltage of the chip is changed on-the-fly while all the modules (including the MCU) continue their normal operation.

Another technique to reduce power is AWB. AWB reduces static power consumption by applying back-bias on the transistors. AWB can be applied on the ARM core and EMI while they are not functioning.

The i.MX25 low-power modes can reduce the system power to various levels. The ARM core can be put into the standby mode, clocks can be gated, PLLs can be stopped (in some cases), and oscillator can be powered-off. The core logic voltage can be reduced to state-retention level when the device is idle.

Table 8 shows the i.MX25 low-power modes.

Table 8. i.MX25 Low-Power Modes

Power Mode	Conditions			
	Core	Well Bias	Clocks	Modules
Run	ARM is active	Well bias is OFF	Clocks are ON	Modules are active
Wait	ARM is in wait for interrupt mode	Well bias is OFF	MCU PLL is ON USB PLL is OFF OSC24M is ON OSC32K is ON	All other modules are OFF
Doze	ARM platform clock is OFF	Well bias is ON	MCUPLL is ON USBPLL is OFF OSC24M is ON OSC32K is ON	All other modules are OFF
Stop	All PLLs are OFF	Well bias is ON	OSC24M is OFF OSC32K is ON	All other modules are OFF
Sleep	All PLLs are OFF Core voltage is dropped to 1 V	Well bias is ON	OSC24M is OFF OSC32K is ON	All other modules are OFF

8.3 i.MX28 Power Management

The i.MX28 contains a sophisticated PMU that includes the following:

- Integrated DC-DC converter
- Four linear regulators
- Regulated 4.2 V output

PMU can operate from a Li-Ion battery using the DC-DC converter, or a 5 V supply using the linear regulators and can automatically switch between them without interrupting the operation. PMU includes circuits for battery and system voltage brownout detection, on-chip temperature, digital speed, and process

monitoring. In addition, there exist safety features such as thermal shutdown and battery charge current cut-off based on the external thermistor.

The integrated PMU converter can be used to provide programmable power for the device and the entire application (up to five rails):

- VDDIO (nominal 3.3 V)—DC-DC or linear regulator from 5 V
- VDDD (nominal 1.2 V)—DC-DC or linear regulator from VDDA
- VDDA (nominal 1.8 V)—DC-DC or linear regulator from VDDIO
- VDD1P5 (nominal 1.5 V)—linear regulator from VDDA for LVDDR2
- VDD4P2 (nominal 4.2 V)—when connected to a 5 V source, it can source DC-DC

The 4.2 V regulated output also allows for programmable current limits:

- Total load plus the battery charge current (5 V limit)
- Battery charge current
- Load current—for both on-chip and off-chip circuits

The 4.2 V circuit adjusts the distribution of current supply between the load and the battery charger depending on programmed current limits and load conditions. For example, when the battery is charged, and the 5 V current limit is exceeded, the 4.2 V regulator derives current from the battery charger circuit and diverts it to the load circuit.

The DC-DC converter can operate from the standard Li-ion battery up to 4.2 V. The converter uses the off-chip reactive components (L and C) and operates in the pulse-width or frequency-modulated mode depending on the load condition. The real-time clock includes an alarm function that can be used to trigger the DC-DC converter. The DC-DC converter then triggers the rest of the system.

PMU is designed to support AVC which can reduce system power consumption by half. AVC also allows the chip to operate at a higher peak CPU operating frequency than that of the typical voltage control systems. The DC-DC converters and the clock generator can be re-programmed on-the-fly to dynamically trade-off power and performance. All the major functional clock domains/branches have trunk level clock gating for the power management, to gate the clock domains OFF when the modules are not required for certain applications. This clock gating is instantiated using an ICG element from the standard cell library. Software must enable the clock domain that drives on-chip devices when trunk level clock gating is implemented. The i.MX28 also has multiple peripheral clock domains to control the clocks of individual peripherals to save power while optimizing the performance. The i.MX28 can be toggled into a deep-sleep mode, which reduces the CPU speed to minimum and shuts down all the peripherals.

The CLK_H domain on the i.MX28 can be programmed to any divided ratio with respect to the CLK_P domain, depending on the performance and power requirements. A dynamic clock frequency management controller monitors the system performance and scales the CLK_H frequency to meet performance needs. When the system is quiesced, the CLK_H frequency is automatically reduced to save power.

The i.MX28 integrates three silicon speed sensor to measure the performance characteristics of an individual die at its ambient temperature and process. One is inside ARM9 to measure the CPU core performance, the other is in core logic which includes system bus and peripherals to measure core logic performance and the last one is inside the DC-DC block. The information given by the speed senor can be monitored by the system software to keep the operating voltage to minimum.

The i.MX28 supports the following low-power modes:

- Standby mode—the power consumption is minimized in this mode. The CPU is switched to the bypass mode (direct clocking from the crystal), interrupts are disabled (except for the wake up sources), DMA is disabled, RAM is switched to the bypass mode and self-refreshed, and the PLL is switched ON.
- Deep-sleep mode—the CPU and all the peripherals (including DC-DC) except the RTC are shut down. The i.MX28 consumes least power in this mode.

Table 9 shows the i.MX28 power mode settings.

Table 9. i.MX28 Power Mode Settings

Core/Clock/Module	Deep-Sleep	Standby	Run (300 MHz)	Run (454 MHz)
ARM core	OFF	OFF	Active at 300 MHz	Active at 454 MHz
USB0 PLL (System PLL)	OFF	OFF	ON	ON
OSC24M	OFF	ON	ON	ON
OSC32K	ON	ON	ON	ON
DCDC	OFF	ON	ON	ON
RTC	ON	ON	ON	ON
Other modules	OFF	OFF	ON	ON

9 Network

The i.MX23 does not provide network features. The i.MX25 includes a FEC and CAN module. The i.MX28 includes two ENET and CAN modules.

Table 10 shows a comparison of the networking features of the i.MX23, i.MX25, and i.MX28.

Table 10. Comparison of Networking Features

Feature	i.MX23	i.MX25	i.MX28
Ethernet	N/A	One FEC 10/100	Two ENET10/100
IEEE 1588 Hardware Timestamp	N/A	N/A	Yes
3-port L2 switch	N/A	N/A	Yes
CAN	N/A	Dual CAN (FlexCAN)	Dual CAN (FlexCAN)

9.1 i.MX25 FEC

FEC on the i.MX25 is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media.

FEC supports the following three different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver:

- 10/100 Mbps MII

- 10/100 Mbps RMII
- 10 Mbps-only 7-wire interface (which uses a subset of MII pins)

Figure 10 shows the i.MX25 FEC block diagram.

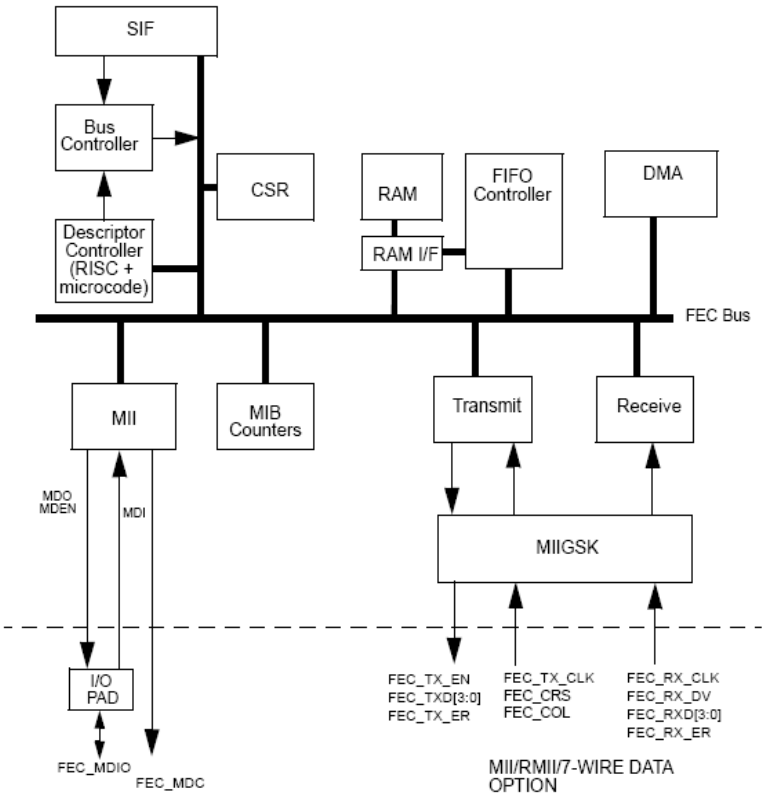


Figure 10. i.MX25 FEC Block Diagram

9.2 i.MX28 Ethernet Interfaces

The i.MX28 includes extensive Ethernet connectivity support. ENET includes two programmable 10/100 IEEE802.3 Ethernet MACs. Similar to the i.MX25, an external PHY or SerDes device is required to complete the interface to the media. Each MAC supports multiple standard media independent interfaces. There is one time stamping module for each MAC to support Ethernet applications that require precise timing references for incoming and outgoing frames to implement a distributed time synchronization protocol such as the IEEE 1588.

In addition, a hardware 3-port switch is supported for redundancy (dual cables) or daisy-chaining (packet forwarding) to support automatic extension of control networks. Two unified DMA (uDMA) blocks allow backward compatibility to FEC interface on the i.MX25.

Figure 11 shows the ENET overview block diagram.

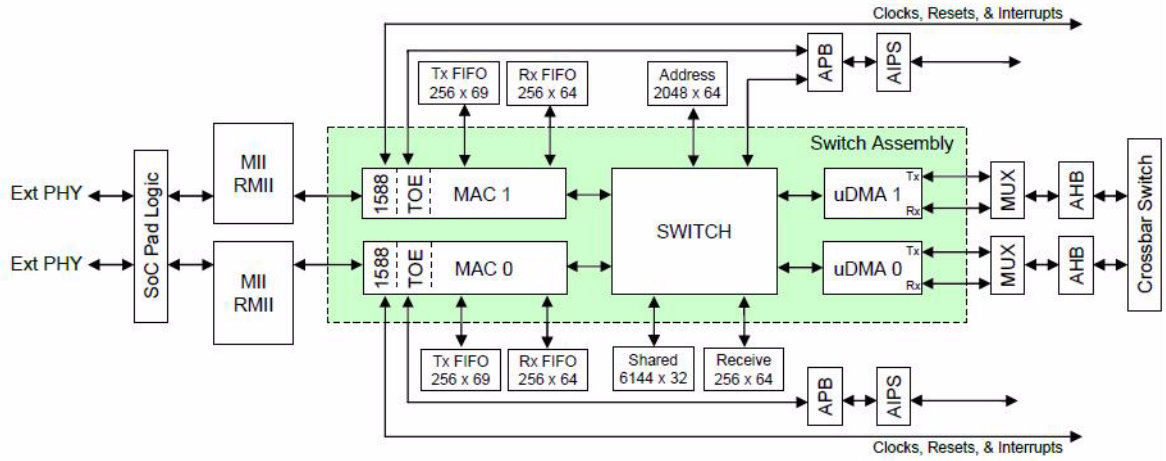


Figure 11. ENET Block Diagram

9.3 i.MX25 FlexCAN

The FlexCAN module on the i.MX25 is a communication controller implementing the CAN protocol according to the CAN2.0B protocol specification. Figure 12 describes the sub modules implemented in the FlexCAN module that includes two embedded memories, one for storing message buffers and other for storing individual RX mask registers. FlexCAN Supports 64 message buffers.

Figure 12 shows the i.MX25 FlexCAN block diagram.

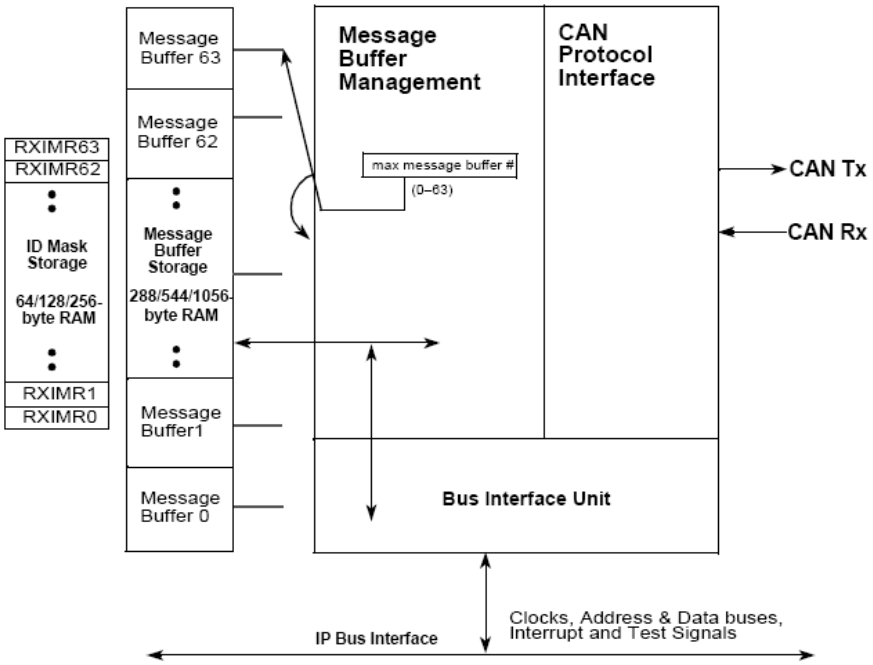


Figure 12. i.MX25 FlexCAN Block Diagram

9.4 i.MX28 CAN Interfaces

The i.MX28 includes two FlexCAN controllers which are compatible with the CAN 2.0B protocol specification.

The CAN Protocol Interface (CPI) performs the following functions:

- Manages the serial communication on the CAN bus
- Requests the RAM access to receive and transmit message frames
- Validates the received messages
- Performs error handling

The Message Buffer Management (MBM) handles selection, reception, and transmission of the message buffer, considering the arbitration and ID matching algorithms.

10 Communications

The i.MX23, i.MX25, and i.MX28 provide several peripherals for external communications such as UART and I^2C. Table 11 shows a comparison of the communication features of the i.MX23, i.MX25, and i.MX28.

Table 11. Comparison of Communication Features

Feature	i.MX23	i.MX25	i.MX28
UART	Three	Five	Six
UART speed	Up to 3.25 Mbps	Up to 4 Mbps	Up to 3.25 Mbps
IrDA	N/A	UART IrDA compatible	N/A
I^2C interface	One	Three	Two
SPI	SSP	CSPI SSI	SSP
SIM	N/A	Yes	N/A
1-wire module	N/A	Yes	N/A
SDIO Rev. 2.0	Yes	Yes	Yes

10.1 i.MX23 Communication Interfaces

The i.MX23 includes three EIA/TIA compatible UARTs—two for application use and one for debug. The application UARTs are high speed devices that can operate up to 3.25 Mbps with 16-byte receive and transmit FIFOs. The application UARTs support DMA and flow control (CTS/RTS). The debug UART can run up to 115.2 kilo bits per second (Kbps) with flow control (CTS/RTS), but it does not support DMA.

The i.MX23 contains a two-wire System Management Bus (SMB)/I^2C bus interfaces. It can act as a slave or master on the SMB interface. The on-chip ROM supports boot operations from I^2C mastered EEPROMs, as well as slave I^2C boot mode. The interface supports standard speed (up to 100 Kbps) and fast speed (up to 400 Kbps) I^2C connections. Typical applications for I^2C bus include EEPROM, LED/LCD, FM tuner, and cellphone baseband device connection.

The i.MX23 also contains two integrated SSP, each with a dedicated DMA channel and a dedicate clock divider from PLL. Each SSP supports a wide range of synchronous serial interfaces that includes the following:

- 1-bit, 4-bit, or 8-bit high speed MMC/SD/SDIO
- Motorola (1-bit) and Winbond (1-bit, 2-bit, and 4-bit) SPI with a maximum of three slave selects
- Texas Instruments SSI

10.2 i.MX25 Communication Interfaces

The i.MX25 includes five high speed TIA/EIA compatible UARTs that can operate up to 4 Mbps. Each UART has two independent, 32-entry FIFOs for transmit and receive. The UARTs also support DMA, flow control (CTS/RTS), DCE/DTE capability, and auto baud rate detection up to 115.2 Kbps. The IrDA functionality can be provided by the UART with the use of external circuitry. But the speed is limited to 115.2 Kbps.

The i.MX25 I^2C provides three standard two-wire serial interfaces for connecting the chip with peripherals or host controllers. The I^2C module provides functionality of a standard I^2C master and slave. This interface operates at standard speed (up to 100 Kbps) and fast speed (up to 400 Kbps) depending on the pin loading and timing characteristics.

The i.MX25 CSPI module is a full-duplex, synchronous, four-wire serial communication module. The CSPI module contains an 8×32 receive buffer (RXFIFO) and 8×32 transmit buffer (TXFIFO). Using data FIFOs, the CSPI allows rapid data communication with fewer software interrupts. The CSPI is master/slave configurable with four chip select signals to support multiple peripherals. The CSPI can operates at a frequency up to one-quarter of the reference clock frequency.

The i.MX25 also provides SSI which is a full-duplex, serial port that allows the device to communicate with a variety of serial devices. These serial devices can be standard codecs, DSPs, microprocessors, peripherals, or popular industry audio codecs that implement the inter-IC sound bus standard, I^2S, and Intel AC97 standard.

The i.MX25 SIM is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards. The SIM block diagram is shown in Figure 13. The SIM module has two ports that can be used to interface with various cards. The interface with the MCU is a 32-bit connection to the IP bus.

Figure 13 shows the i.MX25 SIM block diagram.

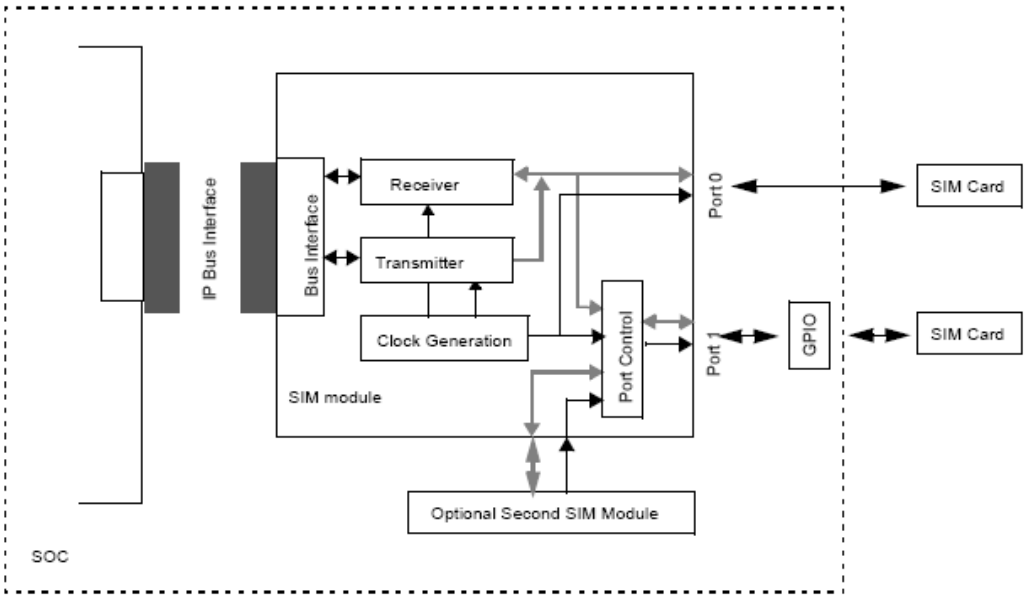


Figure 13. i.MX25 SIM Block Diagram

The i.MX25 includes a 1-wire module which provides the communication link to a generic 1-Kbit add-only memory. The module sends or receives one bit at a time, with an option for the software to manage the data using bytes. The required protocol to access the generic 1-wire device is defined by Maxim-Dallas. The generic 1-wire device contains information about the battery characteristics.

Figure 14 shows the i.MX25 1-wire module block diagram.

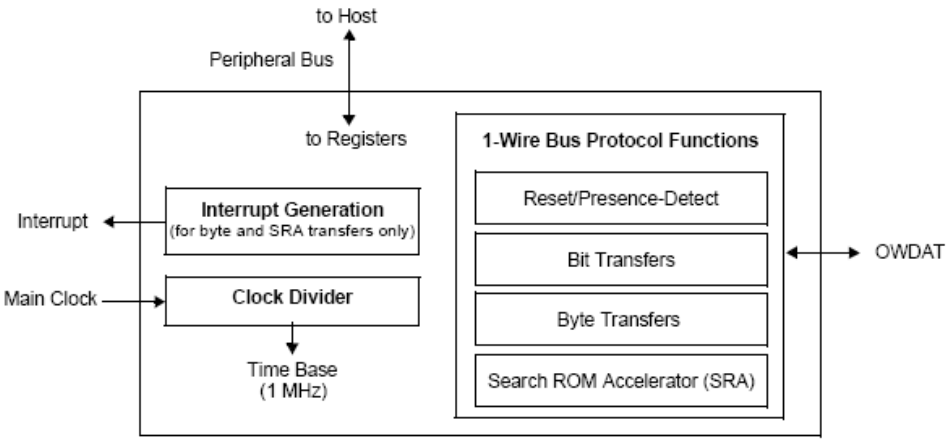


Figure 14. i.MX25 1-Wire Module Block Diagram

10.3 i.MX28 Communication Interfaces

The i.MX28 includes six high speed TIA/EIA compatible UART—five for application use and one for debug. The application UARTs can operate up to 3.25 Mbps with 16-byte receive and transmit FIFOs. The

application UARTs supports DMA and flow control (CTS/RTS). The debug UART can operate only up to 115.2 Kbps with flow control support. However, it does not support DMA.

The i.MX28 contains two SMB/I^2C bus interfaces. Each interface can act as a slave or master on the SMB interface. The on-chip ROM supports boot operations from I^2C mastered EEPROMs and slave I^2C boot mode. The interface supports standard speed (up to 100 Kbps) and fast speed (up to 400 Kbps) I^2C connections. Typical applications for I^2C bus include EEPROM, LED/LCD, FM tuner, and cellphone baseband device connection.

The i.MX28 contains four integrated SSP to provide flexible interfaces for inter-IC and removable media control and communication. The SSP supports the following modes:

- MMC/SD/SDIO 1-bit, 4-bit, and 8-bit modes
- SPI master and slave modes
- Texas Instruments SSI mode

SSP is fully compliant with the eMMC 4.4 standard. Specifically, it supports power-on and alternate boot mode and is designed to perform SDR and DDR operations at a maximum speed of 52 MHz. In SPI mode, SSP has the enhancements to support 1-bit legacy MMC cards and SPI master dual (2-bit) and quad (4-bit) read modes. SSP has a dedicated DMA channel in the bridge and can also be controlled directly by the CPU through PIO registers. Each SSP is independent of the other and can have different SSPCLK frequencies.

11 I/O Modules

Table 12 shows a comparison of the I/O modules of the i.MX23, i.MX25, and i.MX28.

Table 12. Comparison of I/O Modules

Feature	i.MX23	i.MX25	i.MX28
USB 2.0 High Speed	1 HS port (Host) with HS PHY (does not support LS)	1 HS port (OTG) with HS PHY and 1 HS port (Host) with FS PHY	1 HS port (OTG) with HS PHY and 1 HS port (Host) with HS PHY
PWM	Five channels	Four channels	Eight channels
GPIO	Yes	Yes	Yes
IOMUX	Pin multiplexing scheme	Yes	Pin multiplexing scheme
LRADC	Yes (12-bit resolution)	Yes (12-bit resolution)	Yes (12-bit resolution)
TSC	Yes (4-wire resistive)	Yes (4-wire or 5-wire resistive)	Yes (4-wire or 5-wire resistive)
KPP	N/A	Yes	N/A

11.1 USB Interface

The i.MX23, i.MX25, and i.MX28 include high speed USB version 2.0 controller and integrated USB Transceiver Macrocell Interface (UTMI) PHY. The USB interface can operate as a USB device or USB host.

The i.MX23 device interface can be connected to USB 2.0 hosts and hubs operating in the USB 2.0 high speed mode at 480 Mbps. The i.MX23 can also be connected to USB 2.0 full speed interfaces at 12 Mbps, low speed interfaces are not supported. The USB port is a dynamically configured port which can support up to five endpoints, each of which can be configured for bulk interrupt or isochronous transfers. The USB configuration information is read from the on-chip memory through the USB controller DMA.

The i.MX25 contains a USB 2.0 OTG and USB 2.0 host. Both the OTG and host ports can operate in the high speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps) modes. The OTG has an integrated HS PHY. The HS host has an integrated FS PHY, but supports HS external PHY through ULPI (UTMI + Low Pin Interface). The module has DMA capability to handle data transfer between internal buffers and system memory.

The i.MX28 contains a USB 2.0 OTG as well as a USB 2.0 host. Both the OTG and the host ports can operate in the high speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps) modes. They have an integrated HS PHY. The module has DMA capability to handle data transfer between internal buffers and system memory.

11.2 PWM Controller

The i.MX23, i.MX25, and i.MX28 contain PWM output controllers. It can be used as high voltage generators for electroluminescent lamp display backlight with external components. The applications also include LED and backlight brightness control. The i.MX25 PWM controller is optimized to generate tones and sound from the stored audio images.

11.3 GPIO and Pin Multiplexing

The i.MX23 has four banks of pins, three of which can be used as GPIO pins. The GPIO pins are fixed at 3.3 V. All digital pins have selectable output drive strength and weak internal keepers to minimize power loss due to the undriven pins. The i.MX23 contains several specialized hardware interfaces, but does not have sufficient pins to allow the use of all interface signals simultaneously. A pin multiplexing scheme is used to choose the interfaces that should be enabled. In addition, the GPIO pins can be used as interrupt inputs, and the interrupt trigger type is configurable.

The GPIO module on the i.MX25 provides 32 dedicated, general purpose, one-bit contacts that can be individually configured as inputs or outputs. The voltage level of the pins depend on the associated supply rail (physical NVCC connection). Each GPIO input has a dedicated edge-detect circuit that can be configured through the software to detect rising edge, falling edge, logic levels on the input signals. The output from the edge detection circuit can be used for generating interrupts. The i.MX25 allows pin sharing by multiple hardware interfaces with an IOMUX. The IOMUX module deals with signal multiplexing and consists of only combinational logic built with a basic IOMUX cell. Each pin is shared by multiple signals and has a related IOMUX cell to handle signal multiplexing. Each IOMUX cell can support up to eight mux mode (ATL0–ATL7), so that each pin can be ultimately shared by eight signals.

The i.MX28 has seven banks of pins, five of which can be used as GPIO pins. Each GPIO pin has separate voltage control (1.8 V/3.3 V). All digital pins have selectable output drive strength and weak internal keepers to minimize power loss due to the undriven pins. The GPIO pins can be used as interrupt inputs and the interrupt trigger type and polarity are configurable. Similar to the i.MX23, a pin multiplexing scheme is used to choose the interface that should be enabled.

11.4 TSC and ADC

The i.MX23 and i.MX28 contain LRADC that provides 16 physical channels of 12-bit resolution analog-to-digital conversion. Only eight virtual channels can be used at a time, but these eight channels can be mapped to any of the 16 physical channels. Some physical channels have dedicated inputs. The remaining six channels are available for other uses such as resistive button sense, touch screens, and other analog input. Channels 0 and 1 have integrated current sources to drive the external temperature monitor thermistors. The LRADC provides typical performance of 12-bit no-missing-codes, 9-bit/~56dB SNR, and 1% absolute accuracy (limited by the bandgap reference). In case of the i.MX23, channels 2-5 have integrated drivers for 4-wire resistive touch screens with drive voltage generation and touch detection interrupt circuit. In case of the i.MX28, for 5-wire TSC, channel 6 can be used for wiper.

The i.MX25 TSC and the associated ADC provide a resistive touch screen solution for low cost Personal Digital Assistants (PDA), cell phones, ePOS devices, and multimedia players. The ADC has a 12-bit resolution and supports a sample rate up to 125 kHz. The module implements simultaneous touch screen control and auxiliary ADC operation for temperature, voltage, and other measurement functions. The module includes the driver switches to control the screen and an input multiplexer to allow one of four additional inputs to be supported. The ADC reference voltage can be configured in differential and single ended modes. The controller supports pen touch screen detection to automatically interrupt the processor.

Figure 15 shows the i.MX25 TSC in the system.

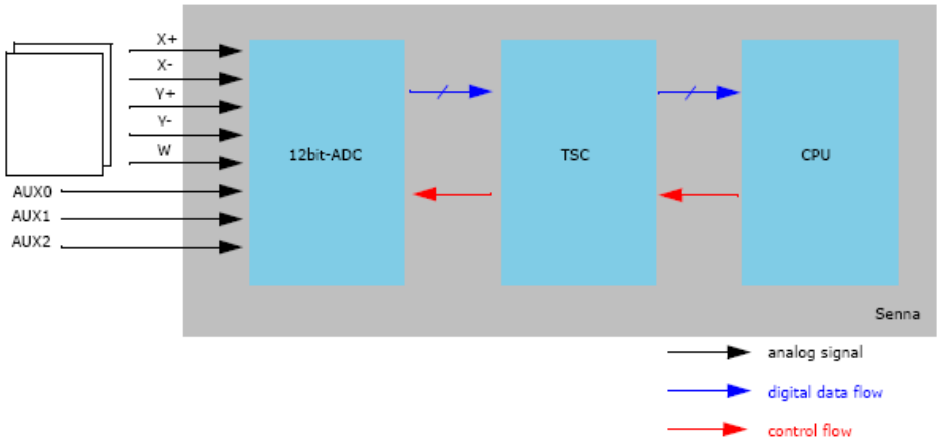


Figure 15. i.MX25 TSC in System

11.5 i.MX25 KPP

The i.MX25 KPP is a 16-bit peripheral that can be used as a keypad matrix interface or as a GPIO. The KPP is designed to interface the keyboard matrix with 2-point contact or 3-point contact keys. It simplifies the software task of scanning a keypad matrix. With appropriate software support, the KPP can detect, debounce, and decode one or multiple keys pressed simultaneously on the keypad.

Figure 16 shows the i.MX25 KPP peripheral block diagram.

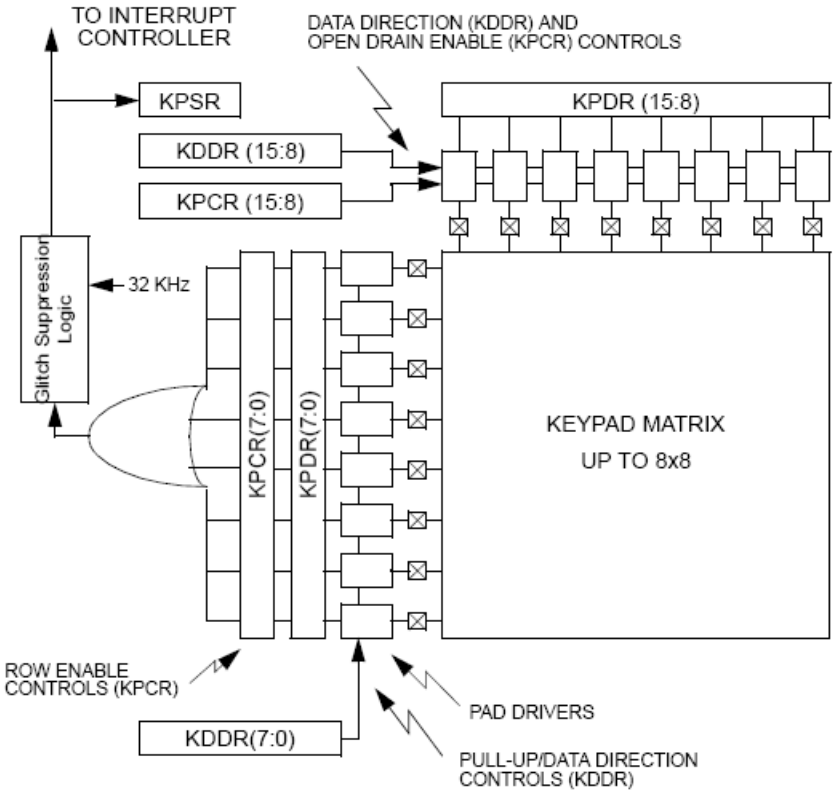


Figure 16. i.MX25 KPP Peripheral Block Diagram

12 Boot Modes

The i.MX23, i.MX25, and i.MX28 can be booted from a number of interfaces. Table 13 shows a comparison of the boot modes of the i.MX23, i.MX25, and i.MX28.

Table 13. Comparison of Boot Modes

Feature	i.MX23	i.MX25	i.MX28
I^2C	Yes	Yes	Yes
SPI	Yes	Yes	Yes
SD/MMC	Yes	Yes	Yes
NAND	Yes	Yes	Yes
JTAG	Yes	Yes	Yes
NOR Flash	N/A	Yes	N/A
USB	Yes	N/A	Yes
UART	N/A	Yes	N/A
WEIM	N/A	Yes	N/A

12.1 i.MX23 Boot Modes

Table 14 lists the boot modes supported by the i.MX23 ROM.

Table 14. Boot Modes Supported by the i.MX23 ROM

PORT	BOOT MODE
USB	Encrypted/unencrypted USB slave boot mode
I^2C	Encrypted/unencrypted I^2C master—boots from 3.3 V EEPROM
SPI1	Encrypted/unencrypted SPI master from SSP1—boots from 3.3 V Flash memory
SPI2	Encrypted/unencrypted SPI master from SSP2—boots from 3.3 V Flash and EEPROM
SSP1	Encrypted/unencrypted SD/MMC master from SSP1—boots from 3.3 V 1-bit, 4-bit, and 8-bit SD/MMC cards
SSP2	Encrypted/unencrypted SD/MMC master from SSP2—boots from 3.3 V 1-bit, 4-bit, and 8-bit SD/MMC cards
GPMI	Encrypted/unencrypted NAND, 3.3 V, 8-bit wide, and ECC4 and ECC8
JTAG_WAIT	Unencrypted startup—waits for JTAG debugger connection

The boot mode can be selected by using the external resistors or through OTP eFuse bit programming. The boot pins on the i.MX23 are located on LCD_RS, LCD_DATA[5], and LCD_DATA[3:0]. LCD_RS is pulled-up to enable the boot mode selection from the LCD data pins. The ROM probles the LCD_RS pin and it is pulled-up. The boot ROM decodes the boot mode vector from the data pins. If LCD_RS is pulled-down, the boot mode is determined by the OTP eFuse bits. In either case, the ROM code selects the boot mode according to the selection map illustrated in Table 15.

Table 15 shows the i.MX23 boot mode selection map.

Table 15. i.MX23 Boot Mode Selection Map

ETM Enable/LCD _DATA [5]	BM3/LCD _DATA [3]	BM2/LCD _DATA [2]	BM1/LCD _DATA [1]	BM0/LCD _DATA [0]	PORT	BOOT MODE
0/1	0	0	0	0	USB	USB (unencrypted versus encrypted is under OTP control)
0/1	0	0	0	1	I^2C	I^2C master
0/1	0	0	1	0	SPI	SPI master SSP1 boot from Flash
0/1	0	0	1	1	SPI	SPI master SSP2 boot from Flash
0/1	0	1	0	0	GPMI	NAND
0/1	0	1	0	1	—	Reserved
0/1	0	1	1	0	JTAG_WAIT	Startup waits for JTAG debugger connection
x	0	1	1	1	—	Reserved
0/1	1	0	0	0	SPI	SPI master SSP2 boot from EEPROM
0/1	1	0	0	1	SSP1	SD/MMC master on SSP1
0/1	1	0	1	0	SSP2	SD/MMC master on SSP2
x	1	0	1	1	—	Reserved

Table 15. i.MX23 Boot Mode Selection Map (continued)

ETM Enable/LCD _DATA [5]	BM3/LCD _DATA [3]	BM2/LCD _DATA [2]	BM1/LCD _DATA [1]	BM0/LCD _DATA [0]	PORT	BOOT MODE
0/1	1	1	0	0	—	Reserved
0/1	1	1	0	1	—	Reserved
x	1	1	1	0	—	Reserved
x	1	1	1	1	—	Reserved

12.2 i.MX25 Boot Modes

The i.MX25 processor boots using HAB which is in the internal ROM. The ROM configures the hardware and validates the image that resides inside the memory, using the HAB library. The boot image is loaded from different memory/device sources and controlled by the boot mode pins, BMOD[1:0]. The loaded boot image is sampled when reset is disabled.

Table 16 lists the i.MX25 boot mode summary.

Table 16. i.MX25 Boot Mode Summary

BMOD [1:0]	Boot Type	Boot Details
00	Internal Boot	Executing ROM code which handles booting from the following sources: • NOR Flash (through WEIM, 16 bit, slow asynchronous mode for debugging • OneNAND • SPI (serial Flash, Chip Select #1)/I^2C • NAND Flash, MLC NAND 0.5-Kbyte/512-byte, 2-Kbyte/4-Kbyte page/(e-fuse selectable) • SD/MMC (support high capacity)/MoviNAND boot (through MMC interface)
01	Reserved	Reserved
10	External (direct) boot	Hardware boot (Direct boot through interface, independent of boot ROM code) from WEIM interface
11	USB/UART bootloader	Load and execute code through serial devices: • USB (Full speed through integrated PHY or external) • UART

12.2.1 i.MX25 Internal Boot

The i.MX25 internal boot is selected by driving 0'b00 on the BMOD[1:0] pins during the device power-up. In this mode, the core boots from internal ROM. The boot code performs hardware initialization, application image validation using the HAB library and then jumps to an address derived from the application image. If any error occurs during the internal boot, the boot code jumps to the UART/USB secure download. Internal boot mode is the only mode in which a secure boot is possible.

The internal boot supports the following boot Flash devices:

- NOR Flash with WEIM Interface, located on CS0, bus width of 16 bits
- OneNAND

- MLC NAND and SLC NAND Flash with NFC interface. Page sizes of 512 byte, 2 Kbyte, or 4 Kbyte and bus width of 8 or 16 bits
- SD/MMC through eSDHC interface supporting high capacity cards
- EPROM boot through the SPI (serial Flash) and I^2C (through CSPI and I^2C modules respectively)

The boot ROM determines the boot device by reading BT_MEM_CTL[1:0] bits on the eFuse as shown in Table 17.

Table 17. i.MX25 Internal Boot Memory Control Type

BT_MEM_CTL [1:0]	Boot Memory Control Type (Memory Device)
00	WEIM
01	NAND Flash
10	Reserved
11	Expansion Device (SD/MMC/MoviNAND, supports high storage, EEPROMs)

12.2.2 i.MX25 External Boot

External boot is supported on the i.MX25 only from the WEIM interface. It is selected by driving 0'b10 on the BMOD[1:0] pins during the device power-up, provided the fuse DIR_BT_DIS is not burnt. In this mode, the core directly boots from the external memory, and it supports muxed or non-muxed address data boot from the WEIM interface. This mode is a nonsecure boot mode.

12.2.3 i.MX25 UART/USB Bootloader

The UART/USB bootloader is selected by driving 0'b11 on the BMOD[1:0] pins during the device power-up. The bootable UART is selected by the BT_UART_SRC[2:0] fuses. Selection between the UART and USB download boot device is determined by polling the UART and the USB controllers. The device that shows activity first is selected.

For the UART, the activity is detected by the Receive Data Ready (RDR) flag, which shows that at least one character is read into the FIFO. The bootable UART (UART 1–5) is selected by BT_UART_SRC[2:0] fuses.

For the USB, either of the integrated on-chip PHYs can be used. An external PHY, the ULPI interface can also be used. For typical application board usage, the internal PHY option is recommended. The external PHY option depends on the availability of the pins. Therefore, the external PHY option is not recommended. The activity is detected by the setup endpoint status register, which shows that the setup transaction is received. Booting from the OTG port is not possible in the current silicon revision due to an errata in the USB OTG VBus pin.

12.2.4 i.MX28 Boot Modes

The boot modes supported by the i.MX28 ROM is shown in Table 18. The boot mode can be selected by using the external resistors or through OTP eFuse bit programming.

Table 18. Boot Modes Supported by the i.MX28 ROM

PORT	BOOT MODE
USB	Encrypted/unencrypted USB slave boot mode
I^2C	Encrypted/unencrypted I^2C0 master—boots from 1.8 V and 3.3 V EEPROM
SPI2	Encrypted/unencrypted SPI2 master from SSP2—boots from 1.8 V and 3.3 V Flash memory
SPI3	Encrypted/unencrypted SPI3 master from SSP3—boots from 1.8 V and 3.3 V Flash and EEPROM
SSP0	Encrypted/unencrypted SD/MMC master from SSP1—boots from 1.8 V and 3.3 V 1-bit, 4-bit, and 8-bit SD/MMC/eSD/eMMC cards
SSP1	Encrypted/unencrypted SD/MMC master from SSP2—boots from 1.8 V and 3.3 V 1-bit, 4-bit, and 8-bit SD/MMC/eSD/eMMC cards
GPMI	Encrypted/unencrypted NAND, 1.8 V and 3.3 V, 8-bit wide, BCH2 to BCH20
JTAG	Wait JTAG connection

The boot pins on the i.MX28 are located on LCD_RS, LCD_DATA[3:0] and LCD_RS is pulled-up to enable the boot mode selection from the LCD data pins. The ROM probles the LCD_RS pin and it is pulled-up. The boot ROM decodes the boot mode vector from the data pins. If LCD_RS is pulled-down, the boot mode is determined by the OTP eFuse bits. In either case, the ROM code selects the boot mode according to the selection map illustrated in Table 19.

Table 19 shows the selection map for the i.MX28 boot mode.

Table 19. i.MX28 Boot Mode Selection Map

VOLTAGE SELECT OR/ LCD_DATA [4]	BM3/ LCD_DATA [3]	BM2/ LCD_DATA [2]	BM1/ LCD_DATA [1]	BM0/ LCD_DATA [0]	PORT	BOOT MODE
x	0	0	0	0	USB0	USB (unencrypted versus encrypted is under OTP control)
0	0	0	0	1	I^2C0	I^2C0 master, 3.3 V
1	0	0	0	1	I^2C0	I^2C0 master, 1.8 V
0	0	0	1	0	SPI2	SPI master SSP2 boot from Flash, 3.3 V
1	0	0	1	0	SPI2	SPI master SSP2 boot from Flash, 1.8 V
0	0	0	1	1	SPI3	SPI master SSP3 boot from Flash, 3.3 V
1	0	0	1	1	SPI3	SPI master SSP2 boot from Flash, 1.8 V

Table 19. i.MX28 Boot Mode Selection Map (continued)

VOLTAGE SELECT OR/ LCD_DATA [4]	BM3/ LCD_DATA [3]	BM2/ LCD_DATA [2]	BM1/ LCD_DATA [1]	BM0/ LCD_DATA [0]	PORT	BOOT MODE
0	0	1	0	0	GPMI	NAND, 3.3 V
1	0	1	0	0	GPMI	NAND, 1.8 V
0	0	1	0	1	—	Reserved
0	0	1	1	0	JTAG	Wait JTAG connection mode
0	0	1	1	1	—	Reserved
0	1	0	0	0	SPI3	SPI master SSP3 boot from EEPROM, 3.3 V
1	1	0	0	0	SPI3	SPI master SSP3 boot from EEPROM, 1.8 V
0	1	0	0	1	SSP0	SD/MMC master on SSP0, 3.3 V
1	1	0	0	1	SSP0	SD/MMC master on SSP0, 1.8 V
0	1	0	1	0	SSP1	SD/MMC master on SSP1, 3.3 V
1	1	0	1	0	SSP1	SD/MMC master on SSP1, 1.8 V
0	1	0	1	1	—	Reserved
0	1	1	0	0	—	Reserved
0	1	1	0	1	—	Reserved
0	1	1	1	0	—	Reserved
0	1	1	1	1	—	Manufacturing Test Mode

13 Revision History

Table 20 provides a revision history for this application note.

Table 20. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	09/2010	Initial release

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