Freescale Semiconductor
Application Note

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Interfacing and Configuring the i.MX25 Flash Devices

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This application note explains the various Flash devices that can interface with the i.MX25. It also explains how to interface and configure the Flash devices.

Contents

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1 Boot Mode and Memory Interfaces

The i.MX25 can boot from an external device. It can also download from the Flash memory using the serial full-speed Universal Serial Bus (USB), USB On-The-Go (OTG), or Universal Asynchronous Receiver/Transmitter (UART) connection. See *i.MX25 Boot Options* (AN3684), for information on the boot modes and eFUSEs.

The i.MX25 can interface to the following memories:

- NAND FLASH by the Near Field Communication (NFC)
- NOR FLASH / PSRAM by the WEIM
- SD / MCC by eSDHC
- EEPROM / Serial FLASH by the SPI interface
- EEPROM by the I^2C Interface

Before customizing the Advanced Tool Kit (ATK), check if the hardware support is available in the latest ATK tool release. See the *ATK User Guide Standard Version* document for a list of supported i.MX platforms and hardwares.

2 Flash Devices and Connection Diagrams

The various Flash devices and their connection diagrams are described in the following sections.

2.1 NAND Flash

The i.MX25 supports single-level cell (SLC) and multi-level cell (MLC) NAND Flash products of up to 64 Kbyte blocks.

- SLC—512 bytes per page, 16 Kbytes per block and memory size up to 8 Gbits
- SLC—2 Kbytes per page, 128 Kbytes per block and memory size up to 64 Gbits
- MLC— 4 Kbytes per page, 512 Kbytes per block and memory size up to 256 Gbits

The size of spare bytes for the 4 Kbytes page size NAND can be 128 or 218 bytes for booting. The NAND bus can be 8 or 16-bits. Also, the i.MX25 supports Open NAND Flash Interface (ONFI) 1.0 devices.

The i.MX25 PDK implementation uses an SLC or MLC with an 8-bit data bus. By default, PDK uses the SLC K9LAG08UOM-2 Gbyte Samsung device. If MLC is to be used, when the PDK is connected to the signals for that option, then a level shifter or a transceiver is required for the clock enable (CE) signals to meet the voltage level of the memory. The CE1, CE2, and CE3 signals belong to a different power rail from the DATA and command signals from the NFC that are listed below:

- NVCC_NFC: 3.3 V
- NVCC_EM1: 1.8 V

Figure 1 shows the NAND interface connection diagram.

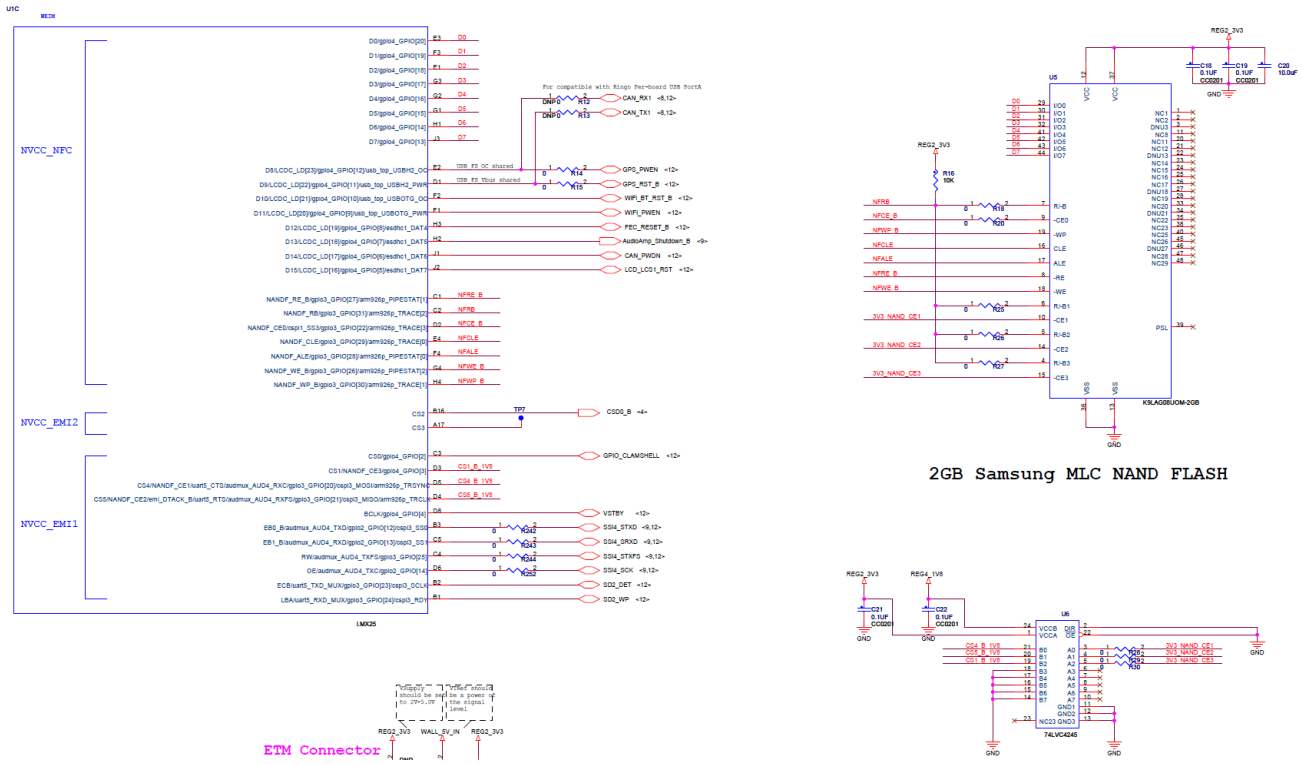

Figure 1. NAND Interface

2.2 I²C EEPROM

The I²C interface operates at a speed of up to 400 kbps, but it depends on the pin loading and the timing characteristics. See *Philips I2C Bus Specification, Version 2.1*, for pin requirement details.

The i.MX25 has three I²C ports that can be used for booting. The i.MX25 boot ROM code uses the 2-Address bytes protocol for accessing. Other types of I²C devices are not supported. Using the 2-Address words, defines the size of 512 ≤ Size ≤ 64 Kbytes (2^{16}).

Figure 2 shows the I²C EEPROM interface diagram.

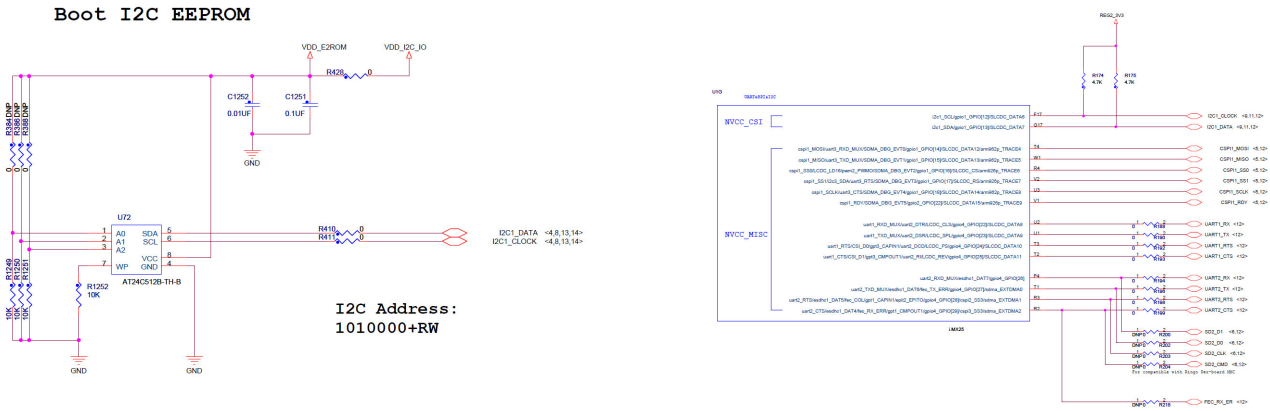

Figure 2. I²C EEPROM Interface

The I²C interface from the i.MX25 can operate at 3.3 V and 1.8 V.

The PDK device AT24C512B, has 3.3 V option. The SDA and SCL signals require external pull-up resistors. The PDK design uses a 4.7 KΩ resistor on the CPU board. The I²C bus specification provides the maximum and minimum values of pull-up resistors.

Also, it is important to configure the address for the I²C EEPROM. The design has pull-up and pull-down option resistors to set the address. By default, the signals for A0 to A2 are connected to the ground.

Table 1 gives the default address during the boot up operation.

Table 1. Default Address

Access: Read/Write

Bits	7	6	5	4	3	2	1	0
Device Select Code	1	0	1	0	0	0	0	0
	Device Type Identifier				Chip Enabled Address[1]			

[1] These address bits should be configured in the memory device to match the 000 value.

If the device address has to be changed because the design is not using the boot mode, then change the I²C address register.

Figure 3 shows the I²C address register.

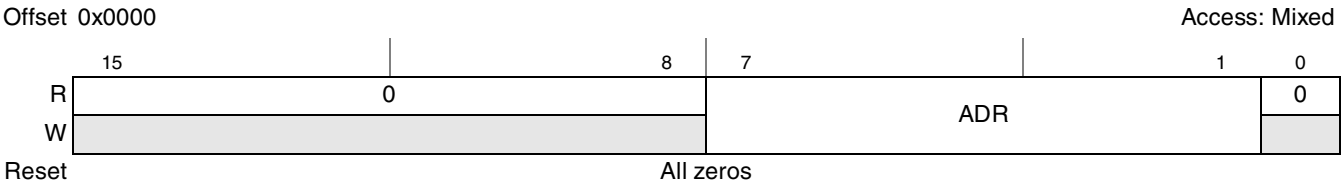

Figure 3. I²C Address Register

Table 2 gives the field descriptions for the I²C address register.

Table 2. Memory Initialization File Format

Field Description	Description
15–8	Reserved
7–1 ADR	Slave address. These fields contains the specific slave address to be used by the I²C module. Slave mode is the default I²C mode for an address match on the bus. **Note:** The IADR holds the address. The I²C responds when it is addressed as a slave. The slave address is not sent on the bus during the address transfer. The register is not reset by a software reset.
0	Reserved

2.3 SPI Flash

The i.MX25 has three configurable serial peripheral interface (CSPI) ports. The CSPI module is a full-duplex, synchronous, four-wire serial communication module. It contains an 8×32 receive buffer (RXFIFO) and an 8×32 transmit buffer (TXFIFO).

Any CSPI module can be used for booting. These modules can read the data from devices in 2 or 3 byte addressing and the burst length is 32 bytes. The Serial ROM should reside on Chip Select #1 of the CSPI module. The serial device is connected as SPI slave interface.

According to the i.MX25 datasheet, the maximum speed for the Master/slave SPI clock is 16.6 MHz. The PDK application uses the CSPI1 and the voltage is 3.3 V as the power rail is NVCC_MISC. If the SPI modules are to be used, then ensure that the correct voltage is used for the memory, because the voltage is supplied by another power rail and a level shifter has to be added.

Figure 4 shows the SPI interface diagram.

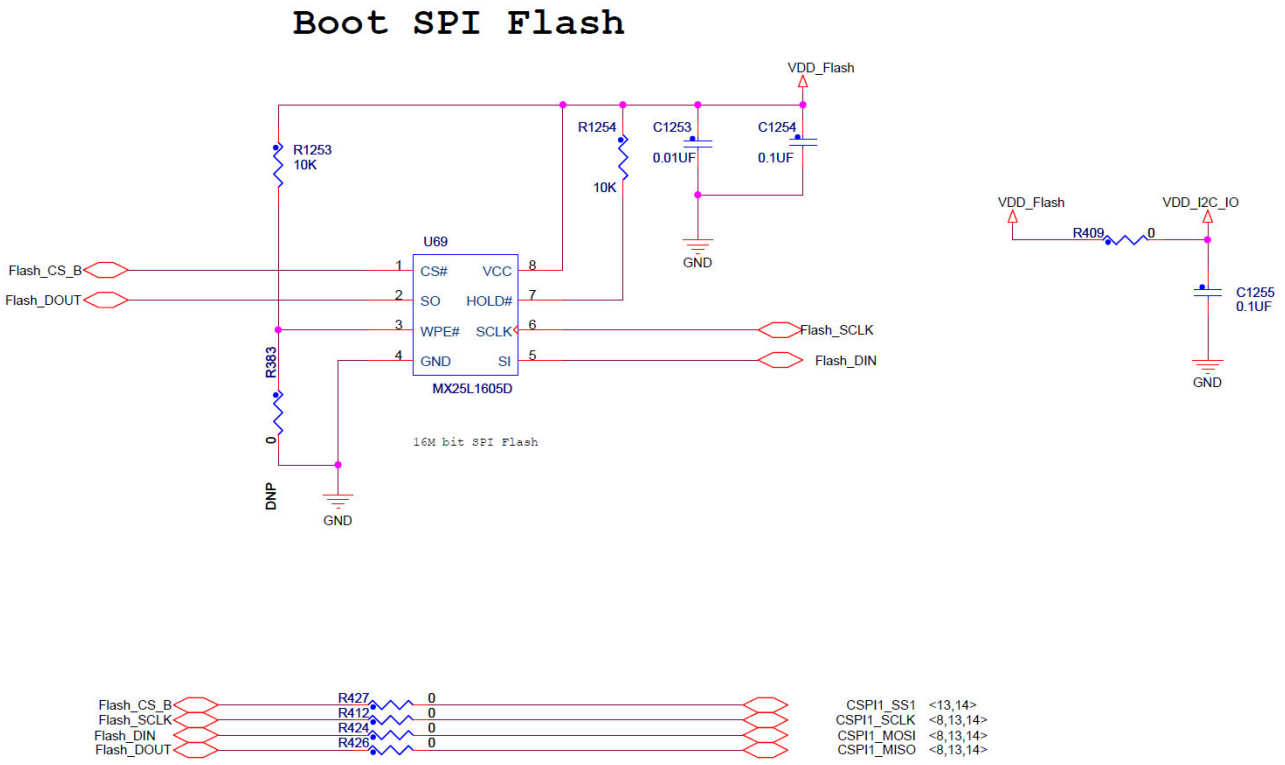

Figure 4. SPI Interface

2.4 SD/MMC Card

The i.MX25 has two enhanced security digital host controller (eSDHC) interfaces and supports the following:

- High capacity SD, eSD (Embedded SD, versions 2.0 and 2.1 Draft Rev. 0.3)
- MMC/eMMC (version 4.3 (MoviNAND), JEDSD84-A43) cards

The SD/MMC interface can operate with low voltage devices. On the PDK board, the interface is connected at 3.3 V power rail and it is supplied by the HDD_3V3 or VDD_SD1_IO voltages. VDD_SD1_IO is the default option.

Also, the PDK has resistor options for two signals: SD1_DET and SD_WP. These are connected to 1.8 V, because they are part of the NVVC_EMI power rail and they are general purpose input/output (GPIO) used for Write Protection (WP) and Detection (DET) functions.

Figure 5 shows the SD Card interface diagram.

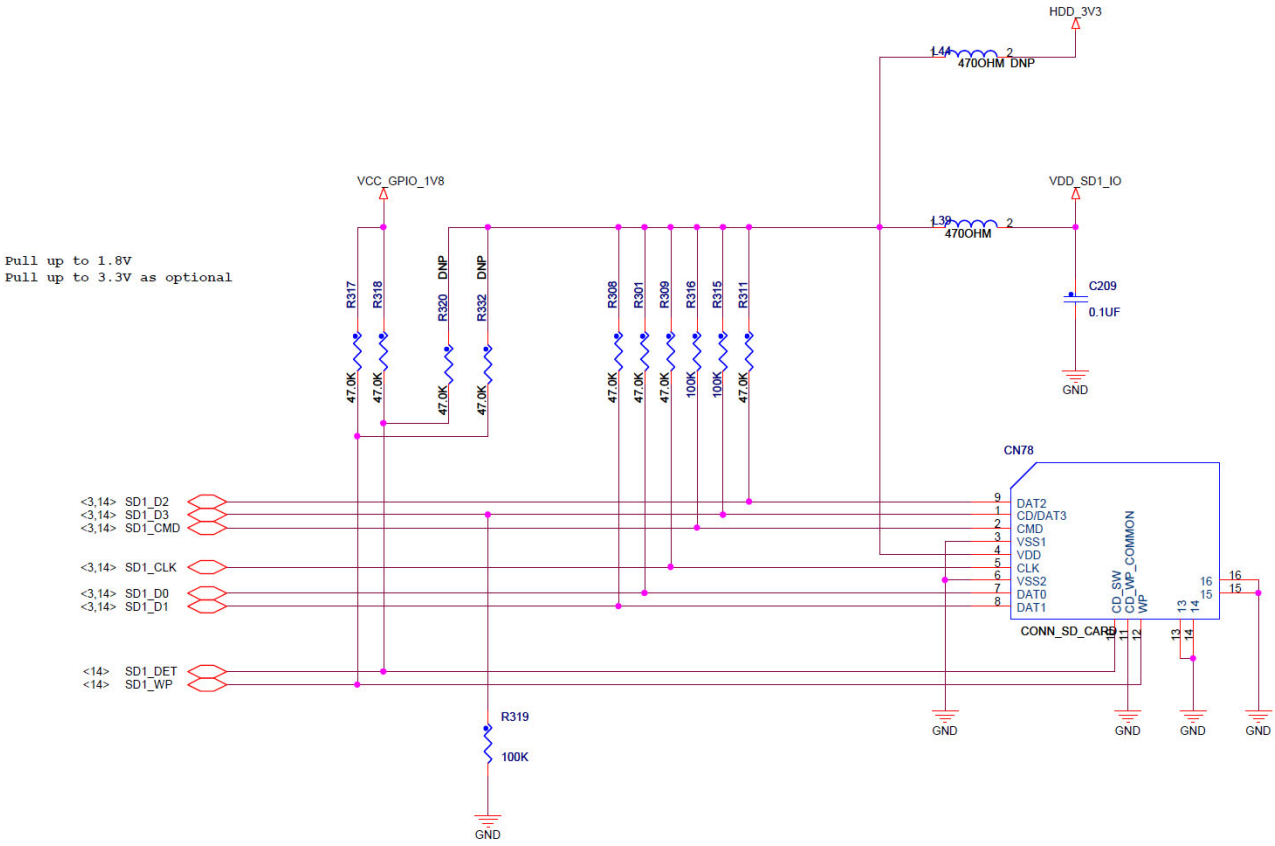

Figure 5. SD Card Interface

2.5 NOR Flash

The i.MX25 microprocessor interfaces NOR Flash and OneNAND devices through the WEIM. For NOR Flash booting, use the chip select 0 (CS0). The NOR Flash interface operates in asynchronous mode, and supports 16-bit muxed Address/Data and non-muxed schemes, based on the fuse settings. Also the 24-bit address option is available for booting. The OneNAND Flash devices are available only with 16-bit interface. By default, the Input/Output Multiplexer (IOMUX) settings at power-on reset (POR) supports NOR boot.

By default, the PDK does not show the NOR Flash implementation. It has the option in the Debug Board.

Figure 6 shows NOR Flash interface with the i.MX25. The interface connects the Address signals that are shared with the double data rate (DDR) interface. The data bus is shared with the NFC and the control signals of the WEIM as follows:

- Address bus: A0–A21
- Data Bus: D0–D15
- Control Signals: WEIM_CS0,WEIM_RW,WEIM_OE# and WEIM_RY/BY#

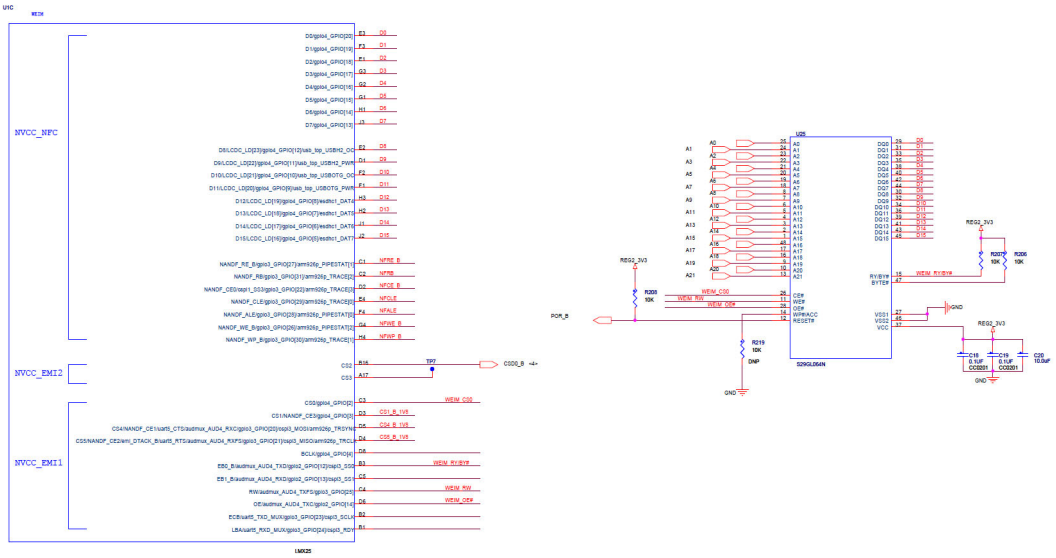

Figure 6. NOR Interface

The device is S29GL064N and the operating voltage is 3.3 V. Ensure that data signals are part of the NVCC_NFC voltage rail and the address bus is attached to the NVCC_EMI. So, if a DDR is used at 1.8 V, then a buffer or a level shifter is required to change the NOR Flash voltage.

The Registers required to configure the WEIM are CSCR0U, CSCR0L, CSCR0A, and WCR. The values after reset are as follows:

- CSCR0U: 0x0000_1E00
- CSCR0L: 0xA000_0841
- CSCR0A: 0x0000_5000
- WCR: 0x0000_0100

3 Revision History

Table 3 provides a revision history for this application note.

Table 3. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	03/2010	Initial release.

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