Freescale Semiconductor
Application Note

Document Number: AN3999
Rev. 0, 03/2010

i.MX27 to i.MX25 Porting Guide

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The i.MX family has a few ARM 9 microprocessors. Among them, the most widely used is the i.MX27 processor and, one of the latest is the i.MX25 processor. This application note describes both these i.MX microprocessors in detail and also provides some recommendations to port an application from i.MX27 to i.MX25.

Contents

1 i.MX27 Overview

The i.MX27 has two versions to choose from: the i.MX27 and i.MX27L. The difference between the two is that the i.MX27 does not include the following features:

- ATA-6 HDD interface
- Memory Stick Pro
- VPU: (MPEG-4/.263/H.264 HW encoder/decoder)
- eMMA (PrP processing, CSC, deblock, dering)

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Figure 1 shows the block diagram of the i.MX27 processor.

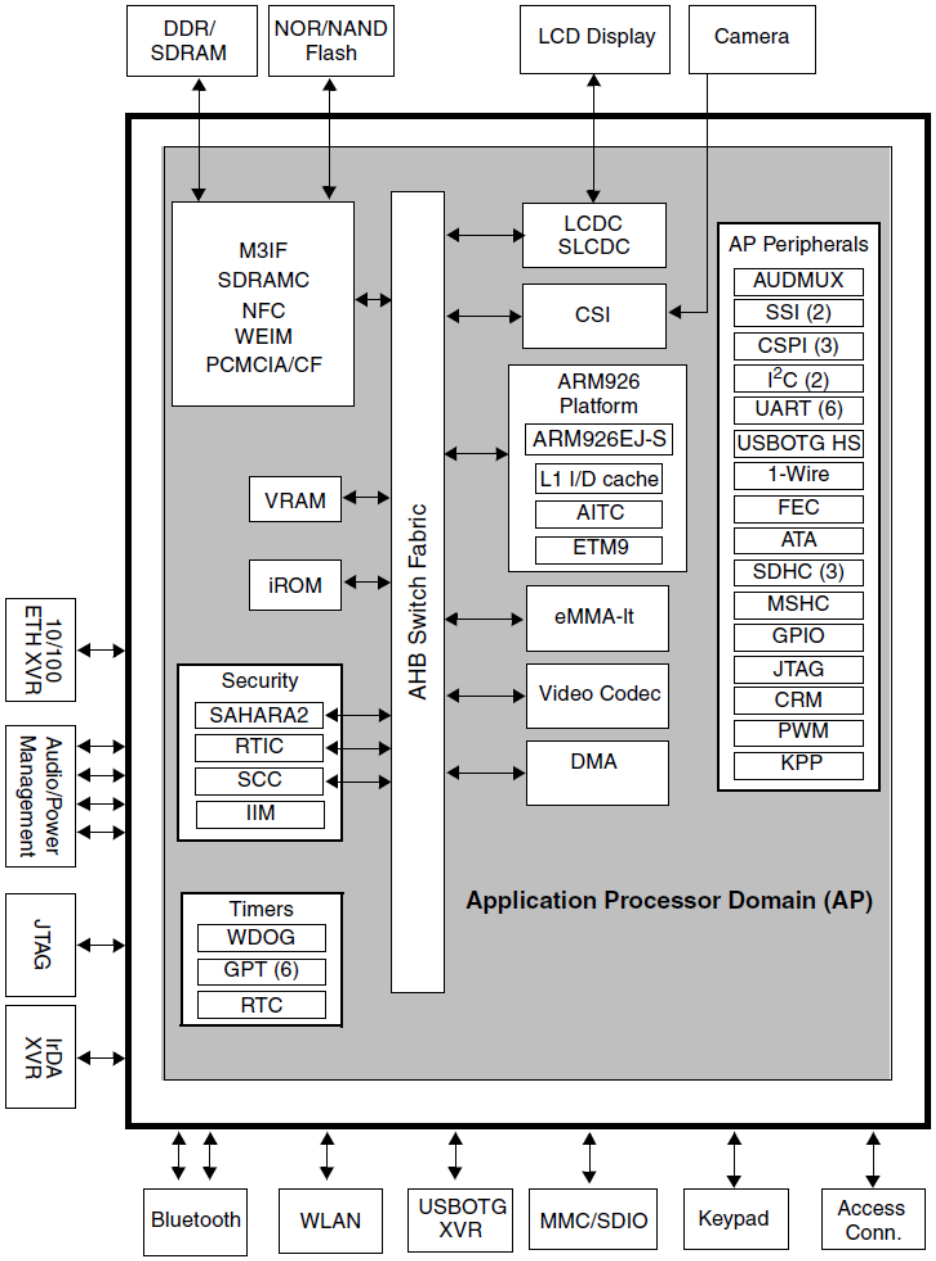

Figure 1. i.MX27 Block Diagram

The features of the i.MX27 processor are as follows:

1-Wire®	1-Wire Interface
AIPI	AHB-Lite IP Interface Module
AITC	ARM9EJ-S Interrupt Controller
AUDMUX	Digital Audio Multiplexer
CRM	Clock and Reset Module

CSI	CMOS Sensor Interface
CSPI	Configurable Serial Peripheral Interface (x3)
DMAC	Direct Memory Access Controller
EMI	External Memory Interface
ESDRAMC	Enhanced SDRAM Controller
FEC	Fast Ethernet Controller
GPIO	General Purpose I/O Module
GPT	General Purpose Timer
I^2C	Inter IC Communication
IIM	IC Identification Module
JTAGC	JTAG Controller
KPP	Keypad Port
LCDC	Liquid Crystal Display Controller
M3IF	Multi-Master Memory Interface
MAX	Multi-Layer AHB Crossbar Switch
NFC	NAND Flash Controller
PCMCIA	Personal Computer Memory Card International Association
PLL	Phase Lock Loop
PWM	Pulse Width Modulator
RTC	Real Time Clock
RTIC	Run-Time Integrity Checkers
SAHARA2	Symmetric/Asymmetric Hashing and Random Accelerator
SCC	Security Controller Module
SDHC	Secured Digital Host Controller
SLCDC	Smart Liquid Crystal Display Controller
SSI	Synchronous Serial Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus 2 Host Controllers and 1 OTG (On-the-Go)
WDOG	Watchdog Timer Module
WEIM	Wireless External Interface Module

The i.MX27 processor is used in two different platforms: the ADS and the PDK and these are used as reference designs.

2 i.MX25 Overview

The i.MX25 processor has five different versions with the modules available on each part number. The available versions are the i.MX251, i.MX253, i.MX255, i.MX257, and i.MX258.

Figure 2 shows the block diagram of the i.MX25 processor.

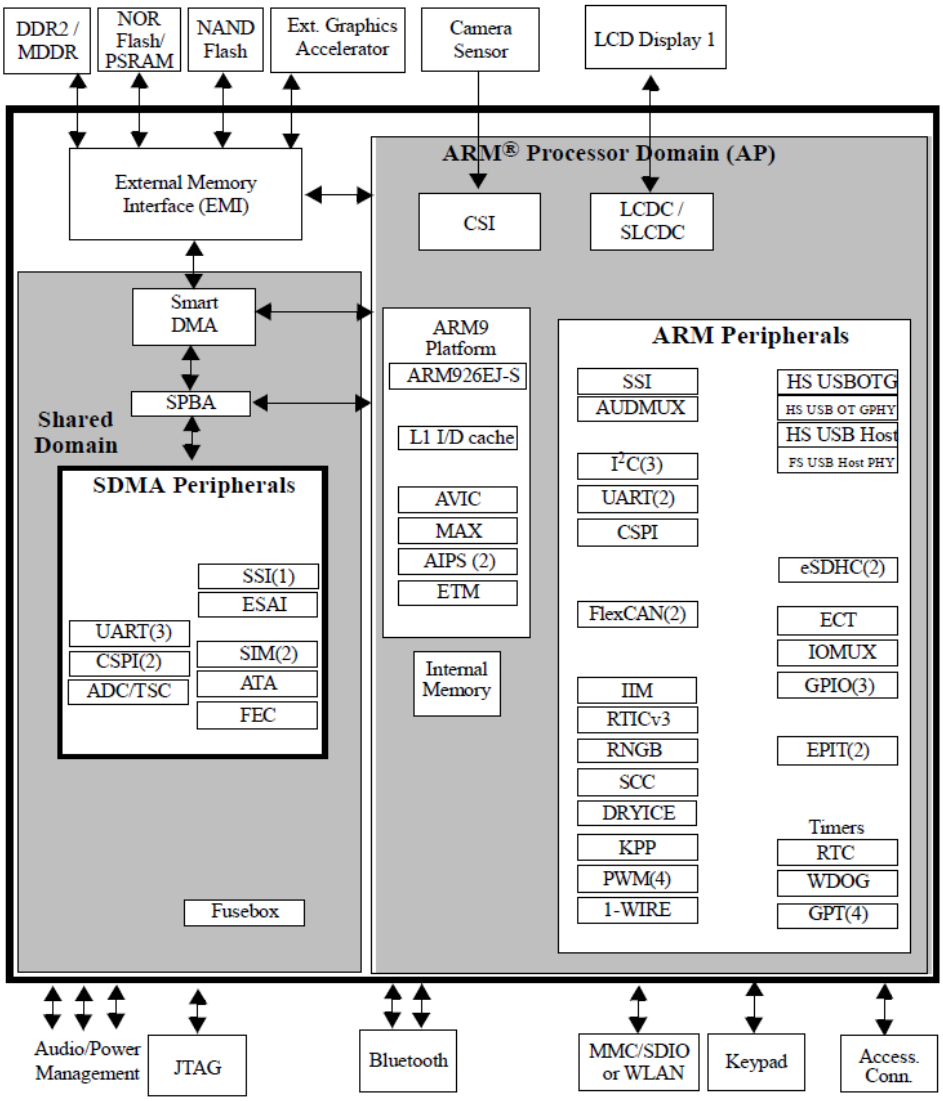

Figure 2. i.MX25 Block Diagram

The features of the i.MX25 processor are as follows:

1-Wire	1-Wire Interface
ATA	Advanced Technology Attachment
AUDMUX	Digital Audio Multiplexer
CCM	Clock Control Module

CSPI	Configurable Serial Peripheral Interface
DRYICE	Security Module
EMI	External Memory Interface
EPIT	Enhanced Periodic Interrupt Timer
ESAI	Enhanced Serial Audio Interface
eSDHC	Enhanced Secure Digital Host Controller
FEC	Fast Ethernet Controller
FlexCAN	Controller Area Network
GPIO	General Purpose I/O Module
GPT	General Purpose Timer
I^2C	Inter IC Communication
IIM	IC Identification Module
IOMUX	I/O Multiplexer
KKP	Keypad Port
LCDC	LCD Controller
PWM	Pulse Width Modulator
SDMA	Smart Direct Memory Access
SIM	Subscriber Identification Module
SJC	Secure JTAG Controller
SLCD	Smart LCD Controller
SSI	Synchronous Serial Interface
TSC (and ADC)	Touch Screen Controller (and A/D Converter)
UART	Universal Asynchronous Receiver/Transmitter
USBOTG/USBHOST	High Speed USB On-The-Go

The i.MX25 processor is used in the PDK platform and this is used as a reference design.

3 i.MX27 versus i.MX25

A better view of the differences between the two processors is highlighted in the table below.

Table 1 shows the differences between the i.MX25 and i.MX27 processors.

Table 1. Differences Between the i.MX25 and i.MX27

ITEM	i.MX25	i.MX27
CPU Frequency	400 MHz/133 MHz	400 MHz/133 MHz
I-Cache/D-Cache	16 KB/16 KB	16 KB/16 KB
DMA	32 channels	16 channels

Table 1. Differences Between the i.MX25 and i.MX27 (continued)

ITEM	i.MX25	i.MX27
Embedded SRAM	128 KB	45 KB
Memory Support	16-bit SDRAM 16-bit mobile DDR 16-bit DDR2	16/32-bit SDRAM 16/32-bit mobile DDR
Touch Controller ADC	Resistive Solution and 3 ADC channels	—
ESAI	Full-duplex serial port	—
USB	1 x OTG v2.0 HS with HS PHY 1 x Host v2.0 HS with FS PHY	1 x OTG v2.0 HS 2 x Host v2.0 (1 FS, 1 HS)
PCMCIA	—	PCMCIA 2.1 standard
UART	5	6
SPI	3	3
I2C	3	2
SD/MMC	2	3
CE-ATA	ATA-6 standard	—
Keypad	8x8	8x8
SIM	2	—
SSI/I2S	2	2
CAN	2	—
TIMER	4	6
Watchdog	1	1
PWM	4	1
Real-time Clock	—	1
Security	Security Controller, IC Identification module, Run-Time Integrity Checker, DryIce module, and Random Number generator	Security Controller, SAHARA2, Run-Time Integrity Checker, and the IC Identification module
Package	17x17 mm, 0.8 mm pitch, 400 MAPBGA	17x17 mm, 0.65 mm pitch, 404-pin MAPBGA 19x19 mm, 0.8 mm pitch, 473-pin MAPBGA package
Temperature	- 20°C to + 70°C, - 40°C to + 85°C	- 20°C to + 85°C; - 40°C to + 85°C
Core Voltage	1.15-1.52 V	1.2-1.52 V
# Power Supplies	22 VDD 9 VSS	24 VDD 9 VSS

Table 1. Differences Between the i.MX25 and i.MX27 (continued)

ITEM	i.MX25	i.MX27
Boot Modes	Boot Mode. These devices has two bits to select the boot mode and the configuration is completed by using eFUSEs or sampling the pins. 00 Internal Boot 01 Reserved 10 External (Direct) Boot 11 USB/UART Serial Boot The supported devices are: • NOR Flash • OneNAND • MLC NAND and SLC NAND Flash with NFC interface. Page sizes of 512 bytes, 2 KB or 4 KB, bus width of 8-bit or 16-bit • SD/MMC/eSD/eMMC via all eSDHC Interface, supporting all types of cards. • eSD FAST BOOT and eMMC Boot Mode (FAST BOOT) are supported via all the eSDHC ports • EEPROM boot via SPI (serial flash) and I2C (via CSPI and I2C modules respectively)	Boot Mode. These are 4-bit system boot mode for the i.MX27 device. 0000 Bootstrap from UART/USB 0001 Reserved 0010 8-bit NAND Flash (2 Kbyte per page) 0011 16-bit NAND Flash (2 Kbyte per page) 0100 16-bit NAND Flash (512 bytes per page) 0101 16-bit CS0 0110 32-bit CS0 0111 8-bit NAND Flash
UART Boot option	All UARTs are bootable	UART1 is bootable
CSI	Embedded DMA controller	No DMA
WEIM	16-bit muxed/non muxed mode 32-bit muxed/mode	16/32-bit muxed/non muxed mode
NAND Flash support	MLC NAND and SLC NAND Flash with NFC interface. Page sizes of 512 bytes, 2 KB or 4 KB, bus width of 8-bit or 16-bit	Only SLC NAND Flash. Page sizes of 512 bytes, 2 KB
Power Modes	Low power boot support (from USB power supply)	—
SDMA	Yes, with seperate RISC core	Yes
External Interfaces	3.3 V Compatible	Fast I/O - 1.75-2.8 V Slow I/O - 1.75-3.05 V DDR - 1.75-1.9 V
SD/MMC protocol support	Full support SD 2.0	SD 1.01

4 Porting an Application

4.1 Hardware Concepts

The hardware concepts to consider when porting an application are as follows:

- Verify whether the same interfaces are being used for the design.
- Check if the PMIC can be reused in the two microprocessors, LCD resolution, and the functionality.
- Verify that the same memory capacity is being used.

- Verify the boot mode configuration.

The i.MX25 processor has an ESDRAM interface with a 16-bit data bus. Therefore, the addressable space limit is 1GBit 4bank DDR devices.

The BATT_VDD is one of the supplies which must be applied to i.MX25 in RTC mode. For the i.MX27 processor - RTCVDD, OSCVDD (may be tied together), and NVDD13 is supplied.

4.2 Software Concepts

The software concepts to consider when porting an application are as follows:

- Modify the registers according to the i.MX25 processor, for all the interfaces.
- Modify the parameters and initialization code for the SDRAM memory.
- Modify the DMA code used in i.MX27 processor according to the i.MX25 SDMA requirements.

5 Revision History

Table 2 provides a revision history for this application note.

Table 2. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	03/2010	Initial release

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Document Number: AN3999
Rev. 0
03/2010