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Application Note

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Interfacing DDR Memories with the i.MX31

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This application note describes the different considerations and methods to route the double data rate (DDR) interface memory with the i.MX31. This application note also gives a few examples for stackup configurations, placement, and routing.

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1 i.MX31 Synchronous Dynamic Random Access Memory (SDRAM) Controller

The following sections discuss the i.MX31 SDRAM controller.

1.1 Bus Signals

The SDRAM controller can be interfaced with single data rate (SDR)-SDRAM and mobile DDR-SDRAM memories. The i.MX31 DDR controller interfaces the following signals with the memories:

- Data bus and corresponding buffer controlling signals
  — SD0-SD31
  — DQS0-DQS3

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  - DQM0-DQM3
- Address bus and corresponding bank controlling signals
  - A0-A9, A11-A12
  - SDBA0-SDBA1
  - MA10
- Control
  - RAS
  - CAS
  - SDCKE0
  - SDWE
  - CDS0
- Clock
  - SDCLK
  - SDCLK_B

1.2 i.MX31 PDK Memory Interface

The i.MX31 PDK interfaces with mobile DDR memory, using 32-bit data. The following memories are tested with the i.MX31:

- Qimonda
  - 128 Mbyte HYB18M1G320BF-7.5
    HYB18M512160AF
  - Used on the i.MX31 PDK
- Hynix
  - 128 Mbyte H5MS1222EFP
  - 256 Mbyte HY5MS5B2ALFP
  - 1 Gbyte H5MS1G22MFP
- Micron
  - 1 Gbyte MT46H32M32LF
  - Requires a change in the initialization code

Figure 1 shows the schematic representation of the memory interface with the mobile DDR memory.

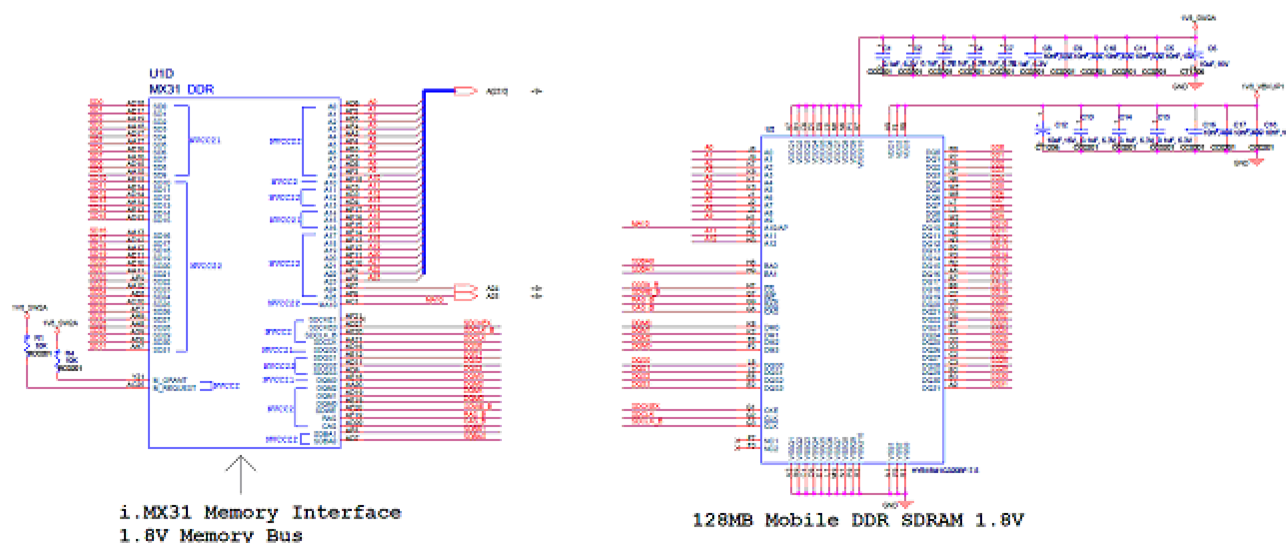

Figure 1. Schematic Representation of Memory Interface with Mobile DDR Memory

According to Figure 1, the total number of signals required to connect to the interface are as follows:

- 60 singled ended
- 2 signals as differential pair
- 3 power signals

1.3 Calculating the Characteristic Impedance

The characteristic impedance, Zo, for the signals should be calculated according to the drive strength of the i.MX31 and the memory.

Equation 1 calculates the driver's output impedance:

$$Zo = (V_{CC} - V_{IOH})/I_{out} \qquad \textit{Eqn. 1}$$

Table 1. Operating Ranges and Parameters

Symbol	Parameter	Test Conditions	Min	Max	Typ	Units
NVCC2 NVCC21, NVCC22	I/O Supply voltage, DDR only	—	1.75	1.95	—	V
I_{OH}	High-level output current	V_{OH} = 0.8*NVCC Std drive High drive Max drive DDR drive	 –3.6 –7.2 –10.8 –14.4	—	—	mA

Using the information provided in Table 1, the following impedances can be obtained.

Equation 2 shows the impedances for standard drive:

$$Zo = (1.8 - (0.8 \times 1.8))/3.6\ m = 100\ \Omega \quad \text{Eqn. 2}$$

Equation 3 shows the impedances for high drive

$$Zo = (1.8 - (0.8 \times 1.8))/7.2\ m = 50\ \Omega \quad \text{Eqn. 3}$$

Equation 4 shows the impedances for maximum drive

$$Zo = (1.8 - (0.8 \times 1.8))/10.8\ m = 33\ \Omega \quad \text{Eqn. 4}$$

Equation 5 shows the impedances for DDR drive

$$Zo = (1.8 - (0.8 \times 1.8))/14.4\ m = 24.5\ \Omega \quad \text{Eqn. 5}$$

According to datasheets of the mDDR memories, the drive strength should be selected based on the expected loading of the memory bus. The settings supported for output drivers can be 25 Ω, 37 Ω, 55 Ω, and 80 Ω which are full, three-quarter, one-half, and one-quarter drive strengths, respectively.

Therefore, the micron DDR memory and the i.MX31 should have the same impendence. It is recommended to route the connection between the i.MX31 and DDR memory with the following characteristic impedance:

- 50 Ω—Single ended
- 100 Ω—Differential pair

Figure 2 shows the connection between the i.MX31 and the DDR memory according to the type of the signals.

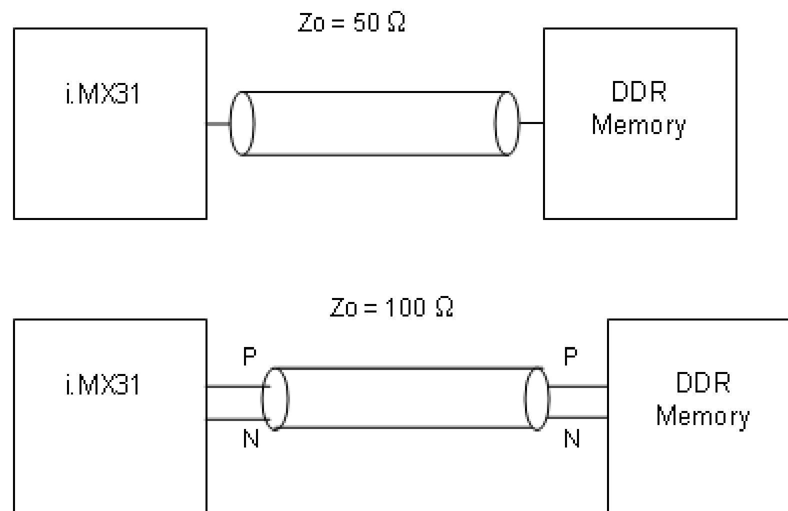

Figure 2. Connection between i.MX31 and DDR Memory

2 Stackup

The previous sections discussed the impedances for the DDR bus. The impedance for the i.MX31 is considered as a high speed bus. Therefore, a good stackup for routing is required and it allows the user to have the impedance control and meet the DDR topology.

The recommended configurations for six layer, eight layer, and ten layer stackup are shown in Figure 3, Figure 4, and Figure 5 respectively.

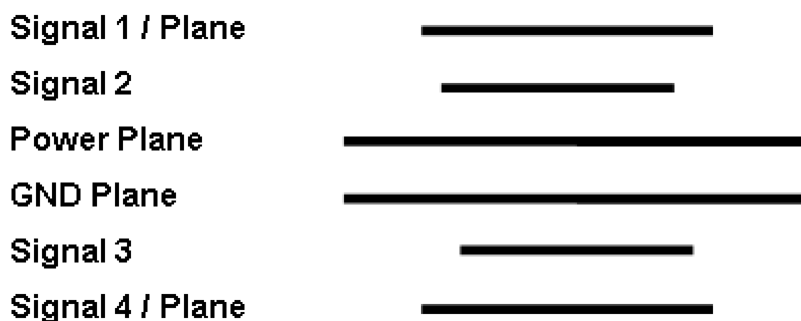

Figure 3. Six Layer Stackup

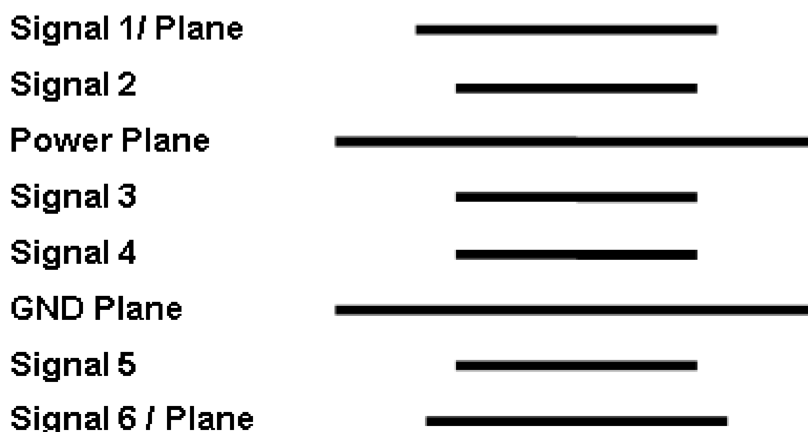

Figure 4. Eight Layer Stackup

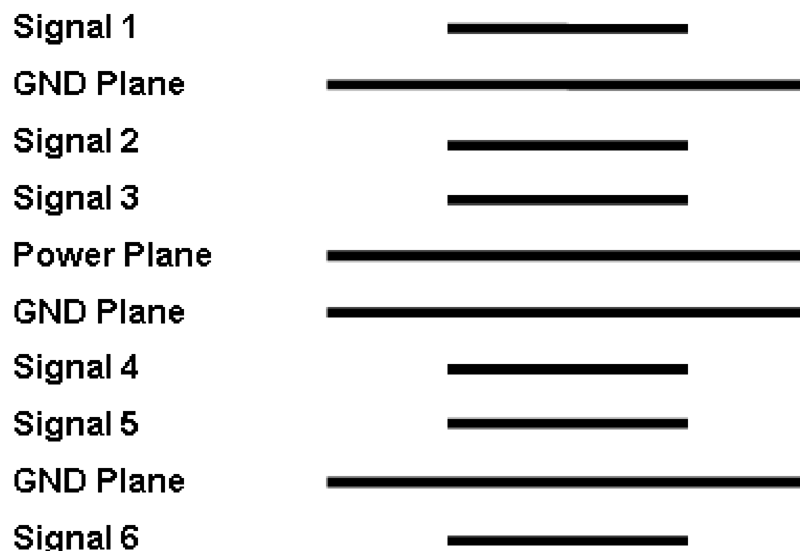

Figure 5. Ten Layer Stackup

These stackups may have different configurations which depends on the critical routing, number of components, and the signals that are shielded by ground (GND) planes. It is very important to ask the PCB manufacturer for the stackup before starting the routing. The stackup gives the next considerations such as, the trace width and the trace geometry. The stackup also allows the user to choose the type of vias and etch spacing.

3 DDR Topology

The applications with the i.MX31 need a small or reduced board with a high density of components. Therefore, it is important to follow the topology to get a better signal integrity.

The point to point topology is intended to have only one trace coming from fanout of the IC. The signals should always have a return path plane. If the design has the power plane as reference, the signals should not have cross or split planes.

Figure 6 shows the point to point connection between the i.MX31 and the DDR memory.

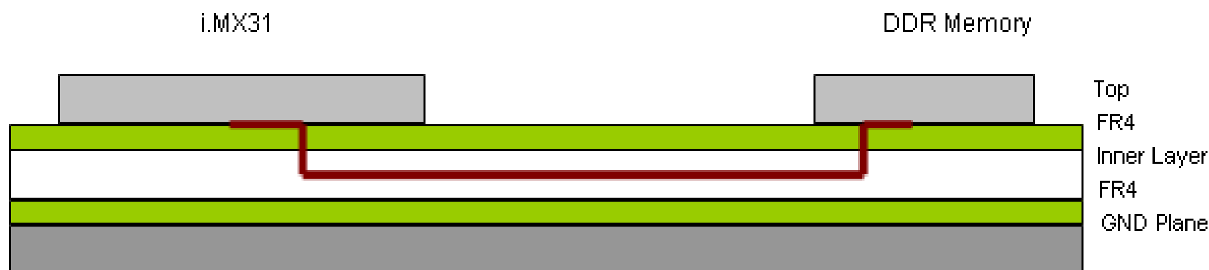

Figure 6. Point to Point Connection between the i.MX31 and DDR Memory

The topology shown in Figure 6 could be modified by placing a series resistors as shown in Figure 7, in order to compensate or improve the signal waveform in different temperature environments or memory configurations.

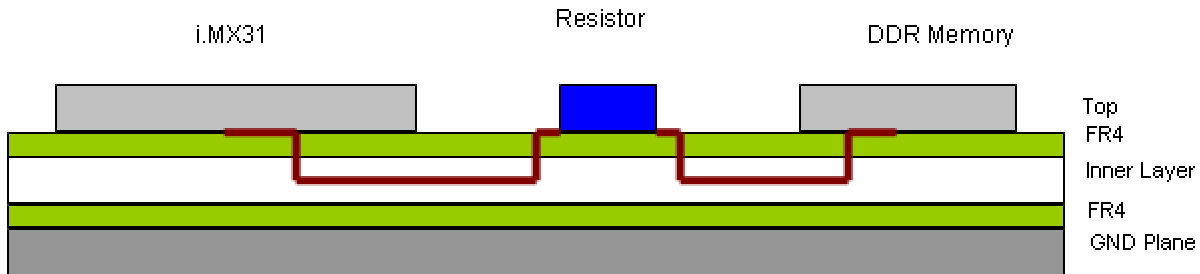

Figure 7. Point to Point Connection between i.MX31, Series Resistor, and DDR Memory

3.1 Maximum Length

The maximum length is critical for the DDR signals and it should be taken into account during the placement. The platforms are routed from 1 to 3 inches as the maximum length for the i.MX31-DDR interface. Note that the routing depends on the stackup and it is recommended to perform few tests in order to verify the quality of the signals.

4 Placement

The following sections discuss the placement of the i.MX31 and DDR memory.

4.1 i.MX31—DDR

The placement of the i.MX31 and DDR memory is important, because it helps to control the total etch of the signal traces. The placement also reduces or increases the difficulty of the routing. In addition, the manufacturing rules for rework should be taken into account to have the necessary spacing for ball-grid array (BGA) handling.

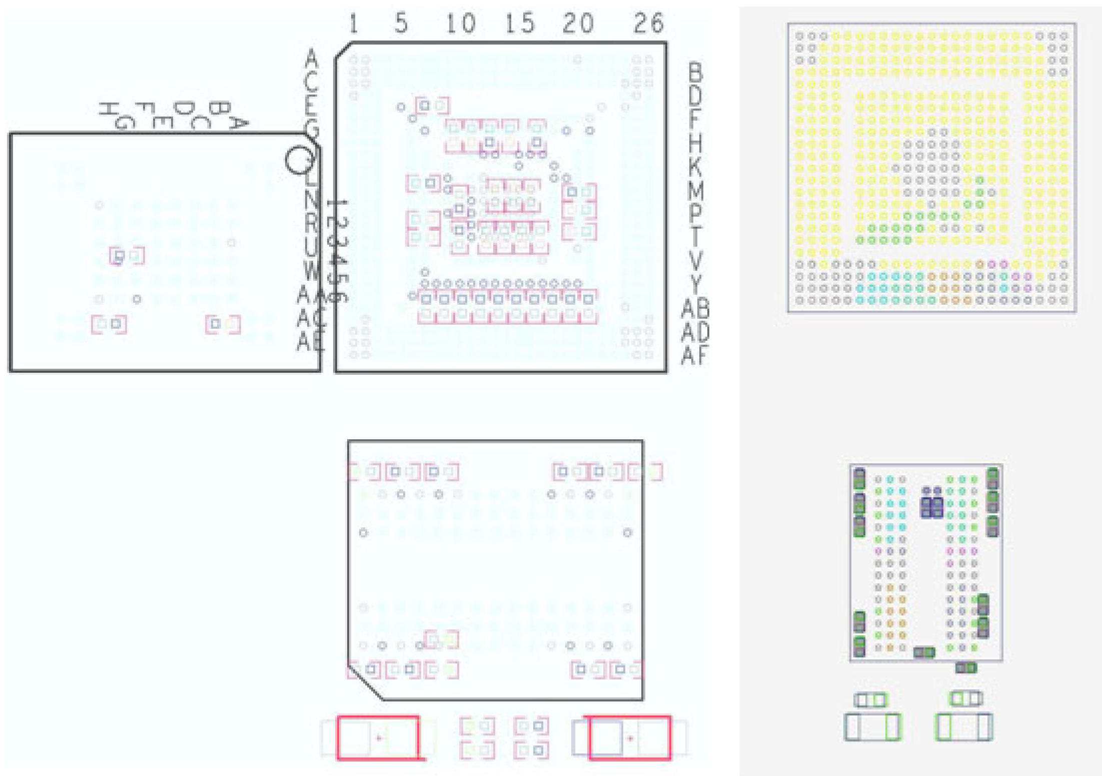

Figure 8. Placement of i.MX31 and DDR Memory

The left side of Figure 8 shows the i.MX31 0.5 mm package and the memory placed with an air gap of 107.421 mils from assembly package drawings. The right side of Figure 8 shows the i.MX31, 0.8 mm package with 400 mils air gap.

4.2 Decoupling Capacitors

The capacitors should be placed as near as possible to the pin. For BGAs, it is recommended to place the capacitors at bottom with a single via and a wide trace.

Figure 9 shows one way to place the decoupling and bulk capacitors and to use the vias from the fanout. It also shows how the bulk capacitors are placed in the opposite side of the routing, which helps to have a routing space without vias.

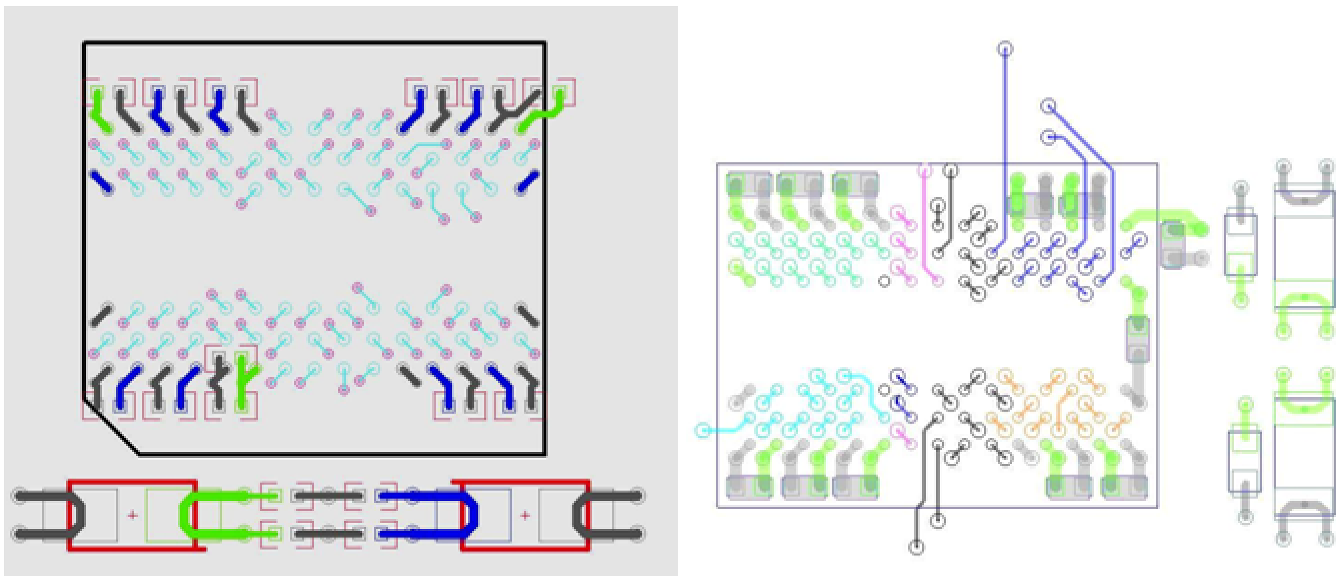

Figure 9. Decoupling Capacitors

5 DDR Routing Rules

The DDR routing can be accomplished by two ways. The first is routing all the signals at the same length and the second one is routing the signals by byte group. Table 2 shows the guidelines to route all the signals at the same length.

Table 2. Rules to Route Signals at Same Length

Signals	Length	Considerations
Address and Bank	≤ Clock length	Match the signals ± 20 mils
Data and Buffer	≤ Clock length	
Control signals	≤ Clock length	
Clock	≤ $L_{critical}$	Match the signals of clocks signals ± 5 mils

Routing all signals at the same length could be more difficult but it is the better way and easy for analysis.

Table 3 shows the guidelines to route the signals by byte group.

Table 3. Rules to Route Signals by Byte Group

Signals	Lengths	Considerations
Address and Bank	Clock length	Match the signals 20 mils

Table 3. Rules to Route Signals by Byte Group (continued)

Signals	Lengths	Considerations
Byte Group 1 DQ0-DQ7,DQS0,DQM0	The Max byte Group 1 length ≤ Clock length	Match the signals of each byte group ± 20 mils The difference between the byte groups should be ± 50 mils
Byte Group 2 DQ8-DQ15,DQS1,DQM1	The Max byte Group 2 length ≤ Clock length	
Byte Group 3 DQ16-DQ23,DQS2,DQM2	The Max byte Group 3 length ≤ Clock length	
Byte Group 4 DQ24-DQ31,DQS3,DQM3	The Max byte Group 4 length ≤ Clock length	
Control signals	≤ Clock length	Match the signals ± 20 mils
Clock	$\leq L_{critical}$	Match the signals of clocks signals ± 5 mils

Routing by byte group requires a better control of the signals of each group, which is more difficult for analysis and constraints settings.

6 i.MX31 0.5 mm—DDR Memory

The i.MX31 0.5 mm package has fine pitch and it is necessary to use via in pad and different types of vias such as, blind, buried or stacked via.

6.1 Design Considerations

The design considerations for the i.MX31 0.5 mm and DDR memory are as follows:

- Stacked via—10 mils pad/5 mils drill
- BGA Spacing—3 mils gap/3 mils width/3 mils gap
- Trace width—3 mils for DDR routing

Using these configuration the fanout shown in Figure 10 is obtained and the signals come out of the BGA.

Figure 10 shows the fanout of the 0.5 mm package.

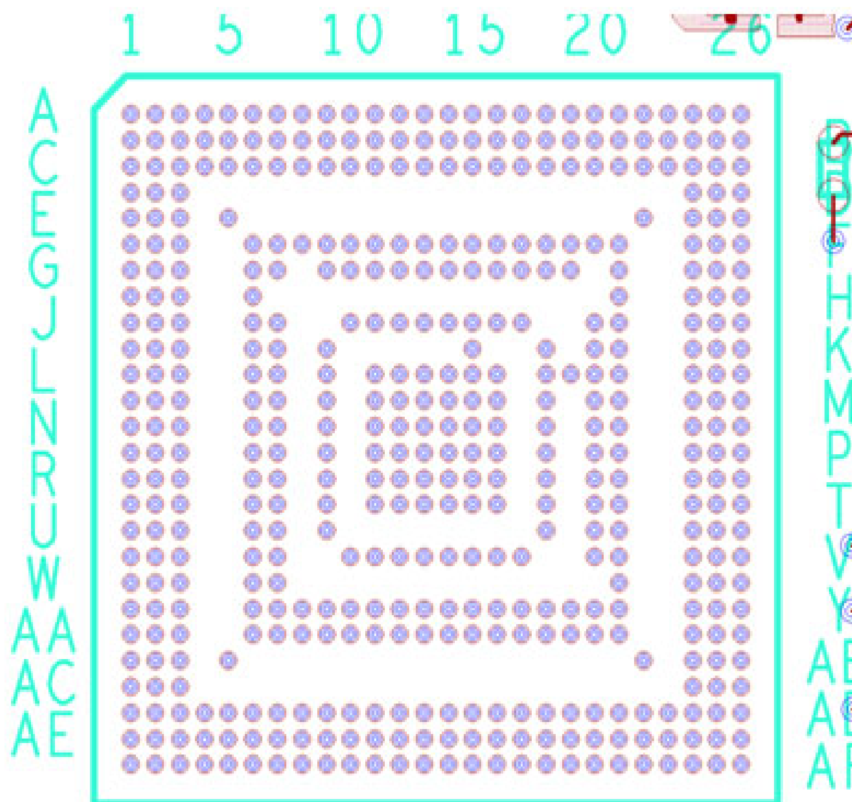

Figure 10. Fanout of 0.5 mm Package

6.2 Routing Example

This section shows few examples of routing for layer 1, layer 2, and layer 3.

Figure 11 shows an example of DDR routing for layer 1.

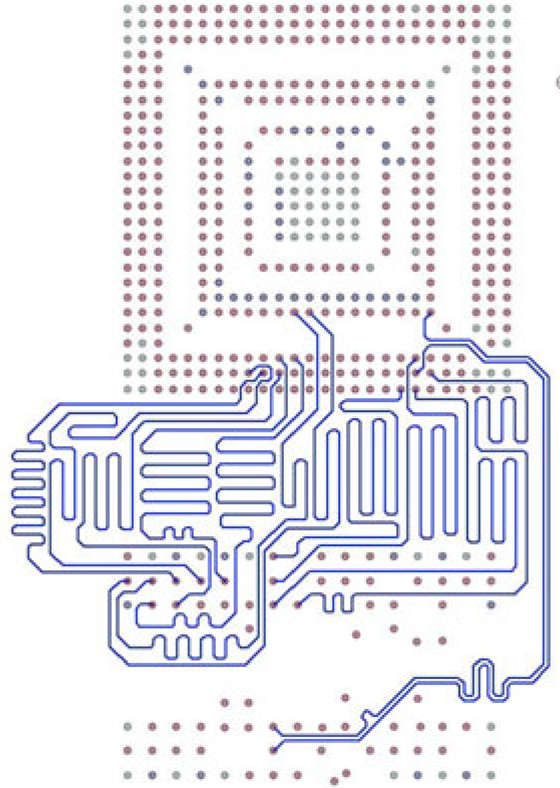

Figure 11. DDR Routing for Layer 1

The clock routing in the right side is kept away from other signals as much as possible. Also, some vias were removed to create the space for the clock routing. The clock was routed in an inner layer and it does not have series resistors.

Figure 12 shows an example of DDR routing for layer 2.

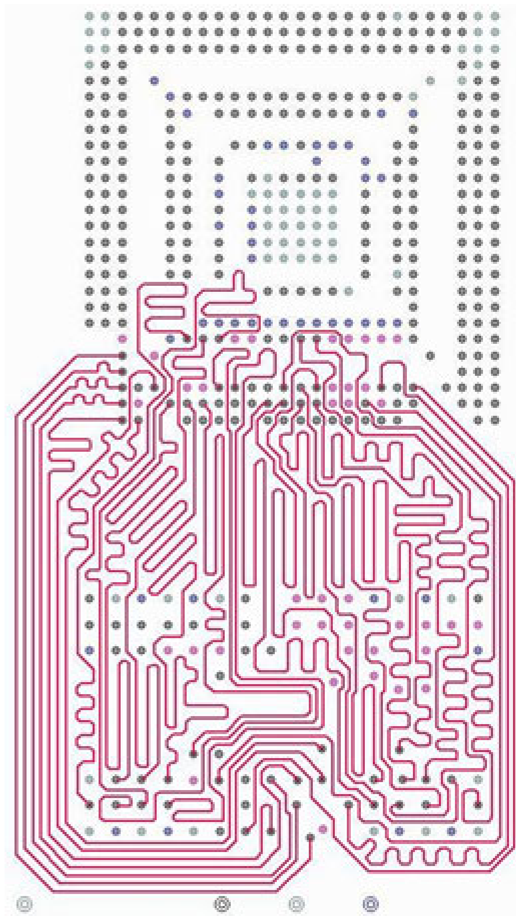

Figure 12. DDR Routing for Layer 2

The vias of the left bottom corner of the i.MX31 were removed in order to create the space for the tuning and routing. Also, some vias from the right side were removed for the same reason.

Figure 13 shows an example of DDR routing for layer 3.

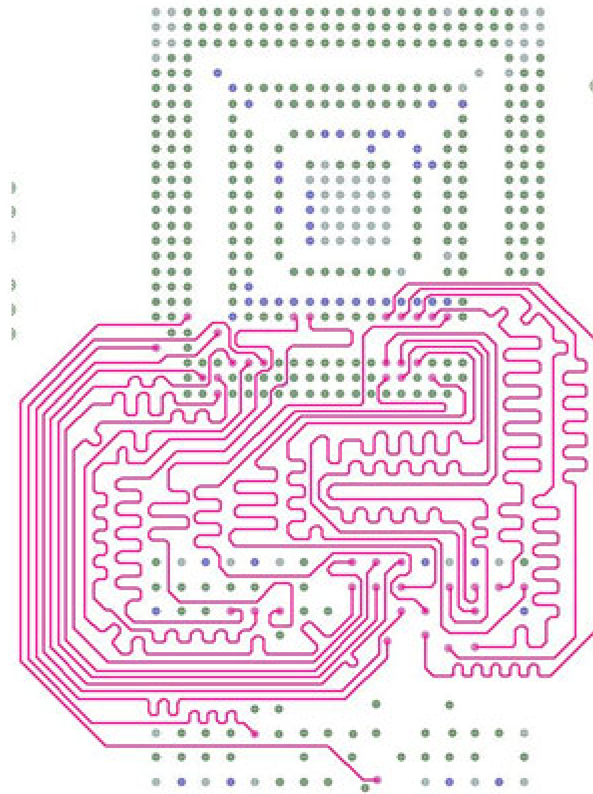

Figure 13. DDR Routing for Layer 3

The last layer for the DDR routing has less vias on the right bottom corner. This is because, the signals of the pins were connected to previous layers.

The routing can be improved, because it has stacked vias and if the signals are connected in one layer, the same net does not have a via. Removing the vias which are not used in the layers increases the space for the routing.

6.3 Total Etch Analysis

The following analysis is intended to show the length of the traces from the DDR routing discussed in Section 6.2, "Routing Example," that was routed at the same length for all signals.

Table 4 shows the total etch analysis of the address signals.

Table 4. Total Etch Analysis of Address Signals

Signal	Min (mils)	Actual (mils)	Max (mils)
A0	1125	1125.599	1135
A1	1125	1130.895	1135
A2	1125	1133.44	1135

Table 4. Total Etch Analysis of Address Signals (continued)

Signal	Min (mils)	Actual (mils)	Max (mils)
A3	1125	1132.663	1135
A4	1125	1134.952	1135
A5	1125	1127.451	1135
A6	1125	1133.241	1135
A7	1125	1132.273	1135
A8	1125	1128.488	1135
A9	1125	1125.14	1135
A11	1125	1128.266	1135
A12	1125	1132.794	1135
MA10	1125	1125.993	1135
SDBA0	1125	1132.072	1135
SDBA1	1125	1130.557	1135

Table 5 shows the total etch analysis of the control and clock signals.

Table 5. Total Etch Analysis of Control and Clock Signals

Signal	Min (mils)	Actual (mils)	Max (mils)
RAS_B	1125	1128.875	1135
CAS_B	1125	1130.91	1135
CSDX_B	1125	1130.955	1135
SDCKEX	1125	1132.719	1135
SDWE_B	1125	1125.987	1135
SDCLK	1125	1129.005	1135
SDCLK_B	1125	1128.999	1135

Table 6 shows the total etch analysis of the data signals.

Table 6. Total Etch Analysis of Data Signals

Signal	Min (mils)	Actual (mils)	Max (mils)
SD0	1125	1125.92	1135
SD1	1125	1130.892	1135
SD2	1125	1126.472	1135
SD3	1125	1129.708	1135
SD4	1125	1126.688	1135
SD5	1125	1126.191	1135

Table 6. Total Etch Analysis of Data Signals (continued)

Signal	Min (mils)	Actual (mils)	Max (mils)
SD6	1125	1133.69	1135
SD7	1125	1127.934	1135
SD8	1125	1127.29	1135
SD9	1125	1125.431	1135
SD10	1125	1125.59	1135
SD11	1125	1125.958	1135
SD12	1125	1132.761	1135
SD13	1125	1126.747	1135
SD14	1125	1125.987	1135
SD15	1125	1132.802	1135
SD16	1125	1127.316	1135
SD17	1125	1132.954	1135
SD18	1125	1125.915	1135
SD19	1125	1125.187	1135
SD20	1125	1133.673	1135
SD21	1125	1127.571	1135
SD22	1125	1126.908	1135
SD23	1125	1134.236	1135
SD24	1125	1125.762	1135
SD25	1125	1125.302	1135
SD26	1125	1132.632	1135
SD27	1125	1131.693	1135
SD28	1125	1134.534	1135
SD29	1125	1127.73	1135
SD30	1125	1131.322	1135
SD31	1125	1131.328	1135
DQM0	1125	1126.138	1135
DQM1	1125	1130.172	1135
DQM2	1125	1125.256	1135
DQM3	1125	1127.26	1135
DQS0	1125	1127.595	1135
DQS1	1125	1127.309	1135

Table 6. Total Etch Analysis of Data Signals (continued)

Signal	Min (mils)	Actual (mils)	Max (mils)
DQS2	1125	1126.44	1135
DQS3	1125	1128.896	1135

The target for the length was 1130 ± 5 mils. According to the DDR routing rules, the length of the signals should be ± 20 mils, but reducing the tolerance is more accurate.

7 i.MX31 0.8 mm—DDR Memory

The i.MX31 0.8 mm package is not considered as a fine pitch component. Therefore, the best way to implement the fanout is by using through hole (TH) vias.

7.1 Design Considerations

The design considerations for the i.MX31 0.8 mm and DDR memory are as follows:

- TH vias—18 mils pad/10 mils drill
- BGA spacing—4 mils gap/4 mils width/4 mils gap
- Trace width—4 mils for DDR routing

Using these configuration the fanout shown in Figure 14 is obtained and the signals come out of the BGA. It also creates some routing channels, where routing is done for more than one trace.

Figure 14 shows the fanout of the 0.8 mm package.

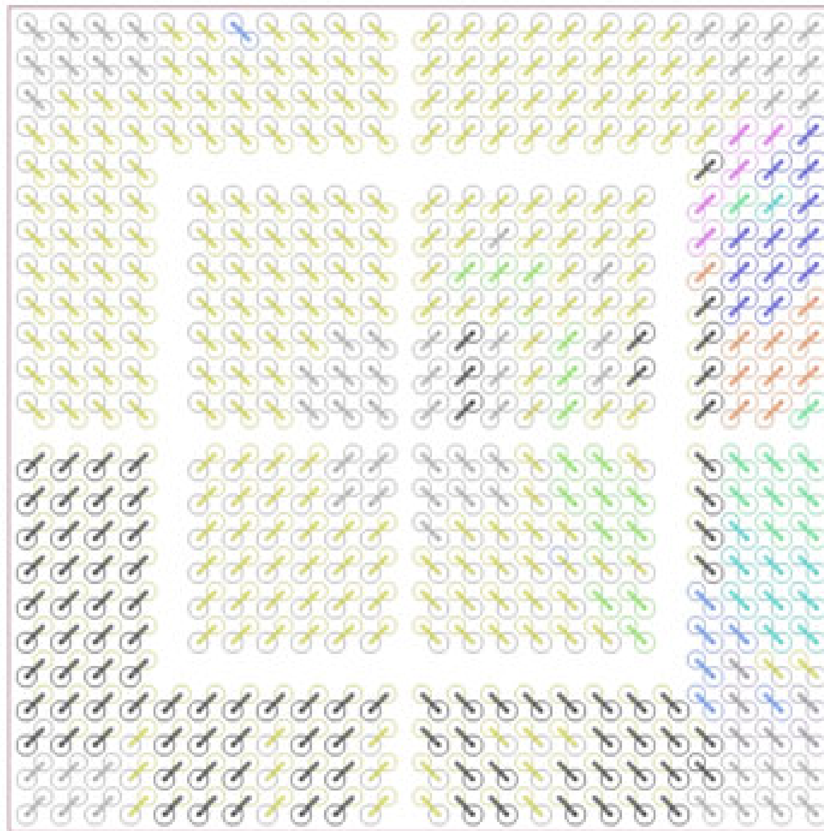

Figure 14. Fanout of 0.8 mm Package

7.2 Routing Example

This section shows few examples of DDR routing for layer 1, layer 2, and layer 3.

Figure 15 shows an example of DDR routing for layer 1.

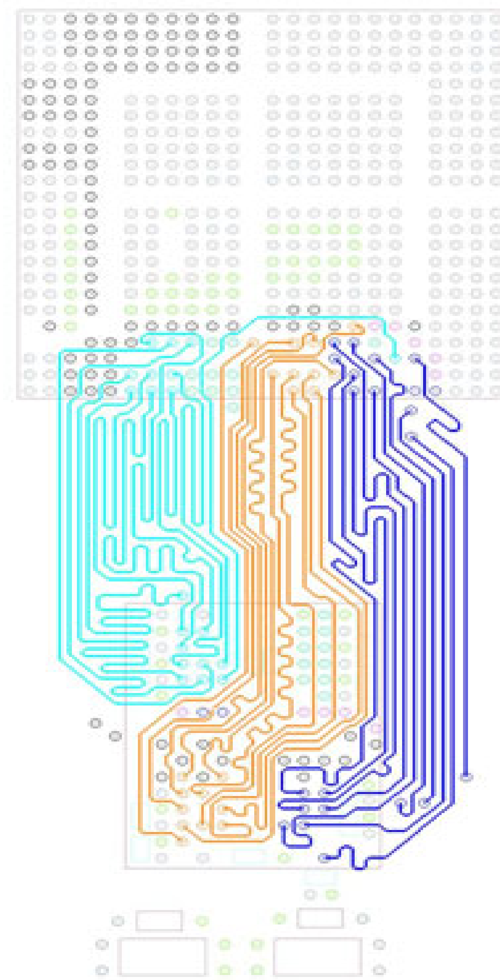

Figure 15. DDR Routing for Layer 1

The fan out is modified to have all signals of each byte group on the same layer. Each color is a byte group with 10 signals.

Figure 16 shows an example of DDR routing for layer 2.

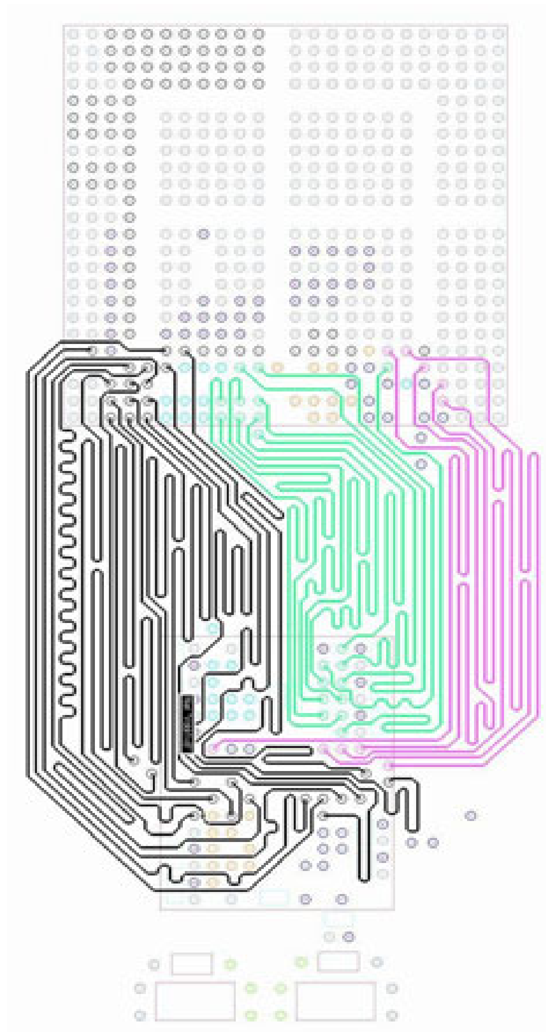

Figure 16. DDR Routing for Layer 2

This second layer contains the routing of one byte group and the address and control signals. The black signals are the address signals and the green signals are the control signals.

Figure 17 shows an example of DDR routing for layer 3.

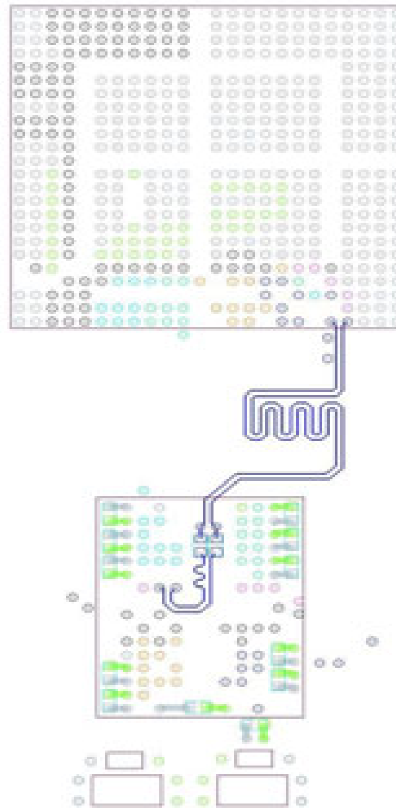

Figure 17. DDR Routing for Layer 3

The clock routing is not in an inner layer; therefore, was routed on bottom, because it has series resistors. Also, it helps to keep it way from other signals.

Finally, this routing can be improved if another inner layer for the routing is used, because there are two layers with two byte groups and a third one for the address and control signals. It may allow reducing the length of the signals. The same effect could be reached if the placement of the DDR memory is closer to the i.MX31.

7.3 Total Etch Analysis

The following analysis shows the length of the traces by byte group from the DDR routing discussed in Section 7.2, "Routing Example."

Table 7 shows the total etch analysis of the address signals.

Table 7. Total Etch Analysis of Address Signals

Signal	Min (mils)	Actual (mils)	Max (mils)
A0	1755	1764.47	1765
A1	1755	1762.23	1765

Table 7. Total Etch Analysis of Address Signals (continued)

Signal	Min (mils)	Actual (mils)	Max (mils)
A2	1755	1757.94	1765
A3	1755	1760.85	1765
A4	1755	1762.26	1765
A5	1755	1757.56	1765
A6	1755	1759.25	1765
A7	1755	1756.42	1765
A8	1755	1761.93	1765
A9	1755	1760.91	1765
MA10	1755	1763.11	1765
A11	1755	1764.26	1765
A12	1755	1759.34	1765
SDBA0	1755	1760.11	1765
SDBA1	1755	1757	1765

Table 8 shows the total etch analysis of the control signals.

Table 8. Total Etch Analysis of Control Signals

Signal	Min (mils)	Actual (mils)	Max (mils)
CAS_B	1755	1764.34	1765
SDCKEX	1755	1755.02	1765
CSDX_B	1755	1755.66	1765
RAS_B	1755	1759.85	1765
WE_B	1755	1762.23	1765

Table 9 shows the total etch analysis of byte group 0.

Table 9. Total Etch Analysis of Byte Group 0

Signal	Min (mils)	Actual (mils)	Max (mils)
SD0	1195	1197.73	1205
SD1	1195	1203.21	1205
SD2	1195	1198.89	1205
SD3	1195	1196.71	1205
SD4	1195	1200.39	1205
SD5	1195	1200.76	1205
SD6	1195	1197.87	1205

Table 9. Total Etch Analysis of Byte Group 0 (continued)

Signal	Min (mils)	Actual (mils)	Max (mils)
SD7	1195	1199.72	1205
DQM0	1195	1199.54	1205
DQS0	1195	1203.8	1205

Table 10 shows the total etch analysis of byte group 1.

Table 10. Total Etch Analysis of Byte Group 1

Signal	Min (mils)	Actual (mils)	Max (mils)
SD8	1195	1198.53	1205
SD9	1195	1198.35	1205
SD10	1195	1200.82	1205
SD11	1195	1197.3	1205
SD12	1195	1196.45	1205
SD13	1195	1196.09	1205
SD14	1195	1197.14	1205
SD15	1195	1199.16	1205
DQM1	1195	1198.32	1205
DQS1	1195	1195.57	1205

Table 11 shows the total etch analysis of byte group 2.

Table 11. Total Etch Analysis of Byte Group 2

Signal	Min (mils)	Actual (mils)	Max (mils)
SD16	1155	1164.34	1165
SD17	1155	1161.16	1165
SD18	1155	1158.11	1165
SD19	1155	1157.45	1165
SD20	1155	1161.28	1165
SD21	1155	1160.34	1165
SD22	1155	1159.1	1165
SD23	1155	1159.3	1165
DQM2	1155	1157.84	1165
DQS2	1155	1161.66	1165

Table 12 shows the total etch analysis of byte group 3.

Table 12. Total Etch Analysis of Byte Group 3

Signal	Min (mils)	Actual (mils)	Max (mils)
SD24	1155	1157.3	1165
SD25	1155	1161.8	1165
SD26	1155	1159.61	1165
SD27	1155	1159.75	1165
SD28	1155	1160.15	1165
SD29	1155	1161.89	1165
SD30	1155	1157.19	1165
SD31	1155	1165.59	1165
DQM3	1155	1162.09	1165
DQS3	1155	1159.99	1165

Table 13 shows the total etch analysis of the clock.

Table 13. Total Etch Analysis of Clock

Signal	Min (mils)	Before Resistors	After Resistors	Actual (mils)	Max (mils)
SDCLK+	1760	1468.76	295.93	1764.69	1770
SDCLK-	1760	1468.44	297.06	1765.5	1770

The target for the length was 1160 ± 5 mils for byte groups 0 and 1, and 1200 ± 5 mils for byte groups 2 and 3. The difference between the groups is 40 mils and the clock routing is 1765 ± 5 mils. The address and control signals were routed at 1760 ± 5 mils. Checking the lengths of the signals against the DDR routing rules, meets the constraints and the tolerance is reduced from ± 20 mils to ± 5.

8 Revision History

Table 14 provides a revision history for this application note.

Table 14. Document Revision History

Rev. Number	Date	Substantive Change(s
0	03/2010	Initial Release

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